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# ST92F124xx/ST92F150Cxx/ ST92F150JDV1/ST92F250CV2

8/16-bit single voltage Flash MCU family with RAM,  
E<sup>3</sup>™ (emulated EEPROM), CAN 2.0B and J1850 BLPD

Datasheet – production data

## Features

- Memories
    - Internal memory: Single Voltage Flash up to 256 Kbytes, RAM up to 8 Kbytes, 1 Kbyte E<sup>3</sup>™ (Emulated EEPROM)
    - In-Application Programming (IAP)
    - 224 general purpose registers (register file) available as RAM, accumulators or index pointers
  - Clock, reset and supply management
    - Register-oriented 8/16 bit CORE with RUN, WFI, SLOW, HALT and STOP modes
    - 0-24 MHz Operation (Int. Clock), 4.5-5.5 V range
    - PLL Clock Generator (3-5 MHz crystal)
    - Minimum instruction time: 83 ns (24 MHz int. clock)
  - Up to 80 I/O pins
  - Interrupt management
    - 4 external fast interrupts + 1 NMI
    - Up to 16 pins programmable as wake-up or additional external interrupt with multi-level interrupt handler
  - DMA controller for reduced processor overhead
  - Timers
    - 16-bit Timer with 8-bit Prescaler, and Watchdog Timer (activated by software or by hardware)
    - 16-bit Standard Timer that can be used to generate a time base independent of PLL Clock Generator
    - Two 16-bit independent Extended Function Timers (EFTs) with Prescaler, up to two Input Captures and up to two Output Compares
    - Two 16-bit Multifunction Timers, with Prescaler, up to two Input Captures and up to two Output Compares
  - Communication interfaces
    - Serial Peripheral Interface (SPI) with selectable Master/Slave mode
- One Multiprotocol Serial Communications Interface with asynchronous and synchronous capabilities
  - One asynchronous Serial Communications Interface with 13-bit LIN Synch Break generation capability
  - J1850 Byte Level Protocol Decoder (JBLPD)
  - Up to two full I<sup>2</sup>C multiple Master/Slave Interfaces supporting Access Bus
  - Up to two CAN 2.0B Active interfaces
- Analog peripheral (low current coupling)
  - 10-bit A/D Converter with up to 16 robust input channels
- Development tools
  - Free High performance development environment (IDE) based on Visual Debugger, Assembler, Linker, and C-Compiler; Real Time Operating System (OSEK OS, CMX) and CAN drivers
  - Hardware emulator and Flash programming board for development and ISP Flasher for production

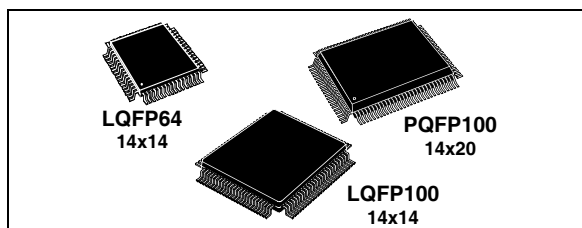


Table 1. Device summary

Reference	Part number
ST92F124xx	ST92F124R1, ST92F124R9, ST92F124V1
ST92F150Cxx	ST92F150CR1, ST92F150CR9, ST92F150CV1, ST92F150CV9
ST92F150JDxx	ST92F150JDV1
ST92F250Cxx	ST92F250CV2

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**Table 2. Detailed device summary <sup>(1)</sup>**

Features	ST92F124xx		ST92F150Cxx		ST92F150JDV 1	ST92F250CV 2
	ST92F124R1 ST92F124R9	ST92F124V1	ST92F150CR1 ST92F150CR9	ST92F150CV1 ST92F150CV9		
FLASH - bytes	64 Kbytes/ 128 Kbytes	128 Kbytes	64Kbytes/ 128 Kbytes	64 Kbytes/ 128 Kbytes	128 Kbytes	256 Kbytes
RAM - bytes	2 Kbytes/ 4 Kbytes	4 Kbytes	2 Kbytes/4 Kbytes	2 Kbytes/ 4 Kbytes	6 Kbytes	8 Kbytes
E <sup>3</sup> ™ - bytes	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte
Timers and Serial Interface	2 MFT, 2 EFT, STIM, WD, SCI, SPI, I <sup>2</sup> C	2 MFT, 2 EFT, STIM, WD, 2 SCI, SPI, I <sup>2</sup> C	2 MFT, 2 EFT, STIM, WD, SCI, SPI, I <sup>2</sup> C	2 MFT, 2 EFT, STIM, WD, 2 SCI, SPI, I <sup>2</sup> C	2 MFT, 2 EFT, STIM, WD, 2 SCI, SPI, I <sup>2</sup> C	2 MFT, 2 EFT, STIM, WD, 2 SCI, SPI, 2 I <sup>2</sup> C <sup>(2)</sup>
ADC	16 x 10 bits	16 x 10 bits	16 x 10 bits	16 x 10 bits	16 x 10 bits	16 x 10 bits
Network Interface	-	LIN Master	CAN	CAN, LIN Master	2 CAN, J1850, LIN Master	CAN, LIN Master
Packages	LQFP64	P/LQFP100	LQFP64	P/LQFP100	P/LQFP100	

1. see [Table 137: Supported part numbers on page 498](#) for the list of supported part numbers.
2. see [Section 16.4 on page 500](#) for important information.

# 1 Description

The ST92F124/F150/F250 microcontroller is developed and manufactured by STMicroelectronics using a proprietary n-well HCMOS process. Its performance derives from the use of a flexible 256-register programming model for ultra-fast context switching and real-time event response. The intelligent on-chip peripherals offload the ST9 core from I/O and data management processing tasks allowing critical application tasks to get the maximum use of core resources. The new-generation ST9 MCU devices now also support low power consumption and low voltage operation for power-efficient and low-cost embedded systems.

## ST9+ core

The advanced Core consists of the Central Processing Unit (CPU), the Register File, the Interrupt and DMA controller, and the Memory Management Unit. The MMU allows a single linear address space of up to 4 Mbytes.

Four independent buses are controlled by the Core: a 22-bit memory bus, an 8-bit register data bus, an 8-bit register address bus and a 6-bit interrupt/DMA bus which connects the interrupt and DMA controllers in the on-chip peripherals with the core.

This multiple bus architecture makes the ST9 family devices highly efficient for accessing on and off-chip memory and fast exchange of data with the on-chip peripherals.

The general-purpose registers can be used as accumulators, index registers, or address pointers. Adjacent register pairs make up 16-bit registers for addressing or 16-bit processing. Although the ST9 has an 8-bit ALU, the chip handles 16-bit operations, including arithmetic, loads/stores, and memory/register and memory/memory exchanges.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST92F150/F124 with 48 (64-pin devices) or 77 (100-pin devices) I/O lines dedicated to digital Input/Output and with 80 I/O lines by the ST92F250. These lines are grouped into up to ten 8-bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing to the external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O. Two memory spaces are available to support this wide range of configurations: a combined Program/Data Memory Space and the internal Register File, which includes the control and status registers of the on-chip peripherals.

## External memory interface

100-pin devices have a 22-bit external address bus allowing them to address up to 4 Mbytes of external memory.

## On-chip peripherals

Two 16-bit Multifunction Timers, each with an 8 bit Prescaler and 12 operating modes, allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

Two Extended Function Timers provide further timing and signal generation capabilities.

A Standard Timer can be used to generate a stable time base independent from the PLL.

An I<sup>2</sup>C interface (two in the ST92F250 device) provides fast I<sup>2</sup>C and Access Bus support.

The SPI is a synchronous serial interface for Master and Slave device communication. It supports single master and multimaster systems.

A J1850 Byte Level Protocol Decoder is available (ST92F150JDV1 device only) for communicating with a J1850 network.

The bxCAN (basic extended) interface (two in the ST92F150JDV1 device) supports 2.0B Active protocol. It has 3 transmit mailboxes, 2 independent receive FIFOs and 8 filters.

In addition, there is a 16 channel Analog to Digital Converter with integral sample and hold, fast conversion time and 10-bit resolution.

There is one Multiprotocol Serial Communications Interface with an integral generator, asynchronous and synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

On 100-pin devices, there is an additional asynchronous Serial Communications interface with 13-bit LIN Synch Break generation capability.

Finally, a programmable PLL Clock Generator allows the usage of standard 3 to 5 MHz crystals to obtain a large range of internal frequencies up to 24 MHz. Low power Run (SLOW), Wait For Interrupt, low power Wait For Interrupt, STOP and HALT modes are also available.

Figure 1. ST92F124R9: Architectural block diagram

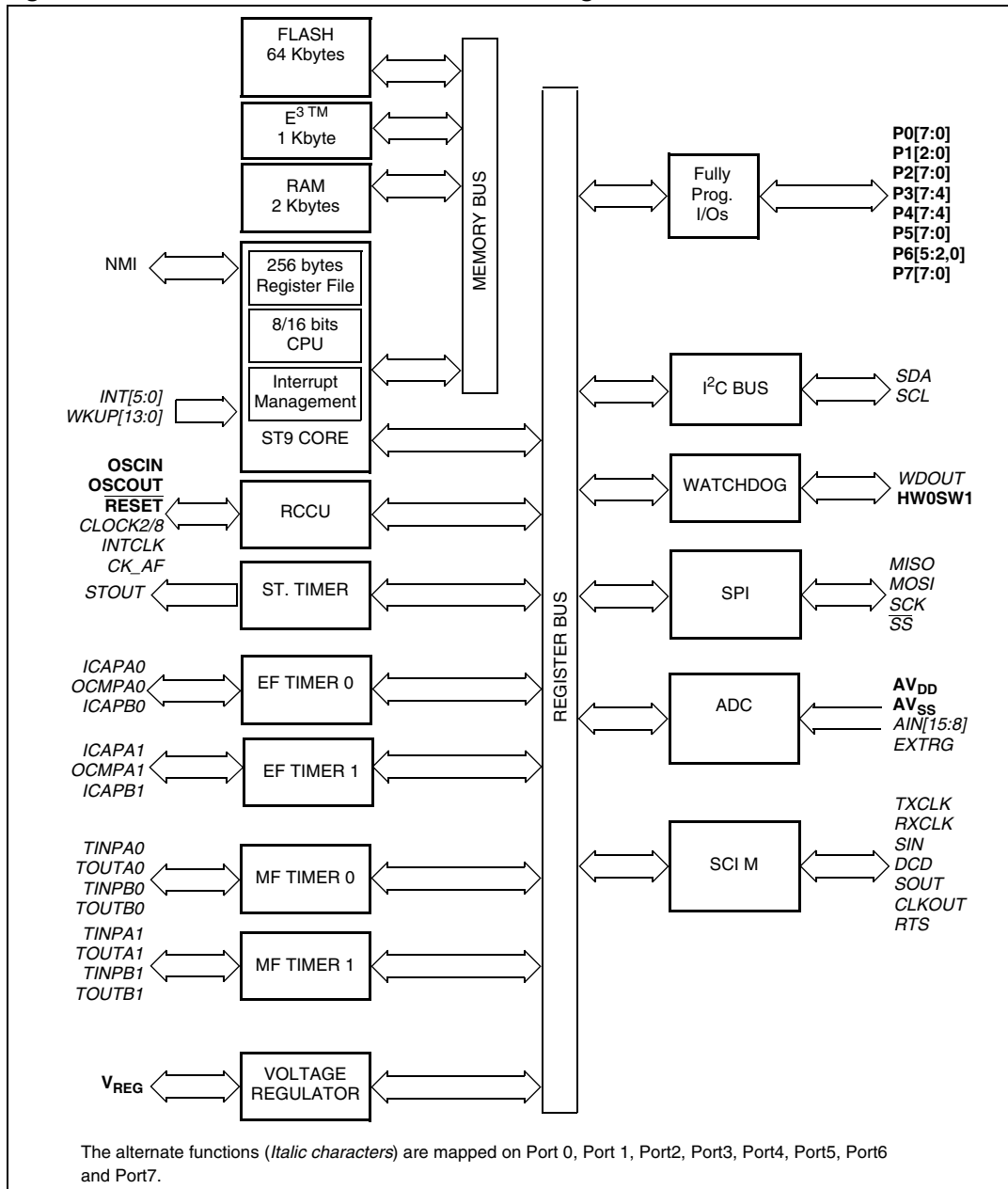


Figure 2. ST92F124V1: Architectural block diagram

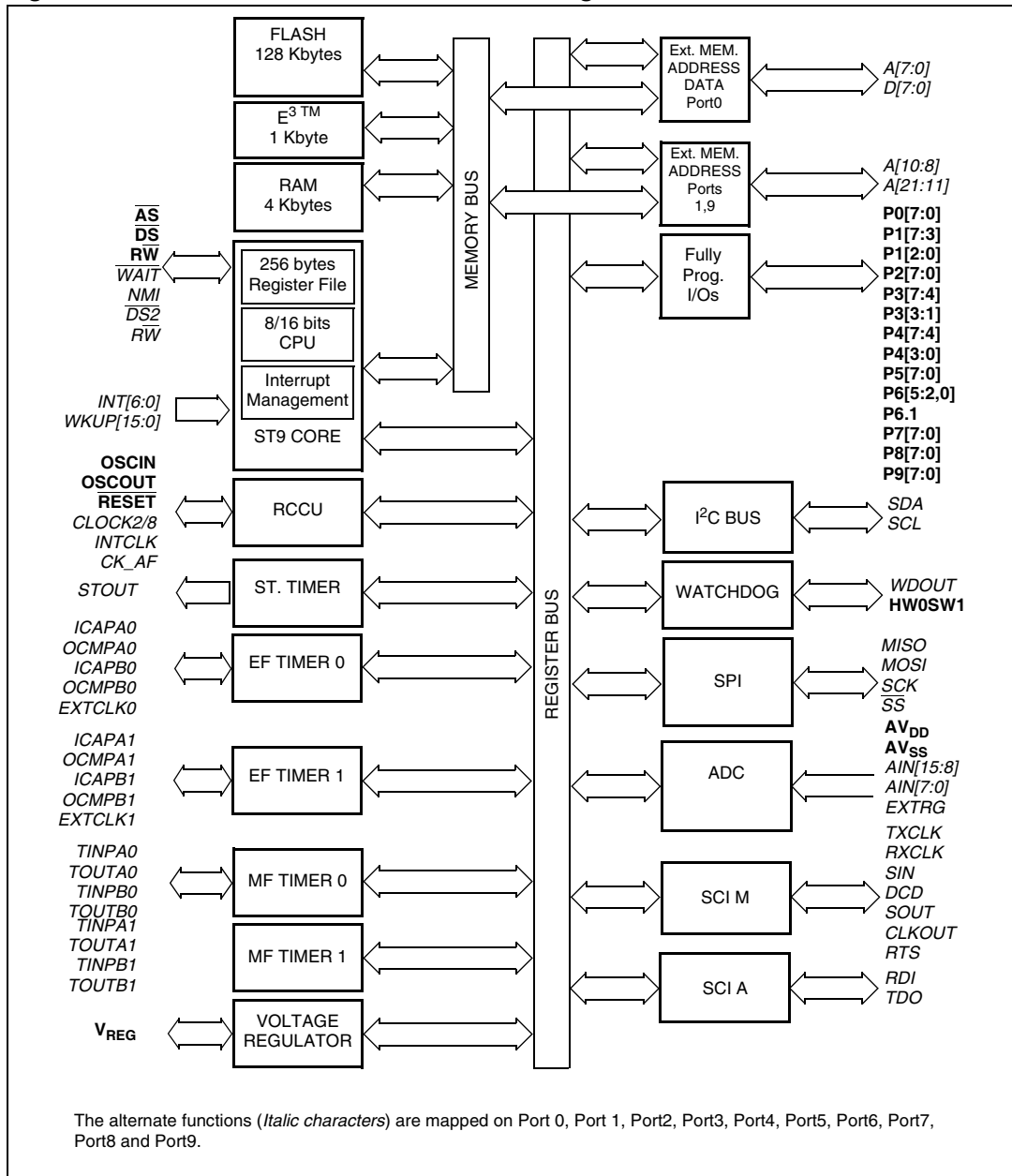


Figure 3. ST92F150C(R/V)1/9: Architectural block diagram

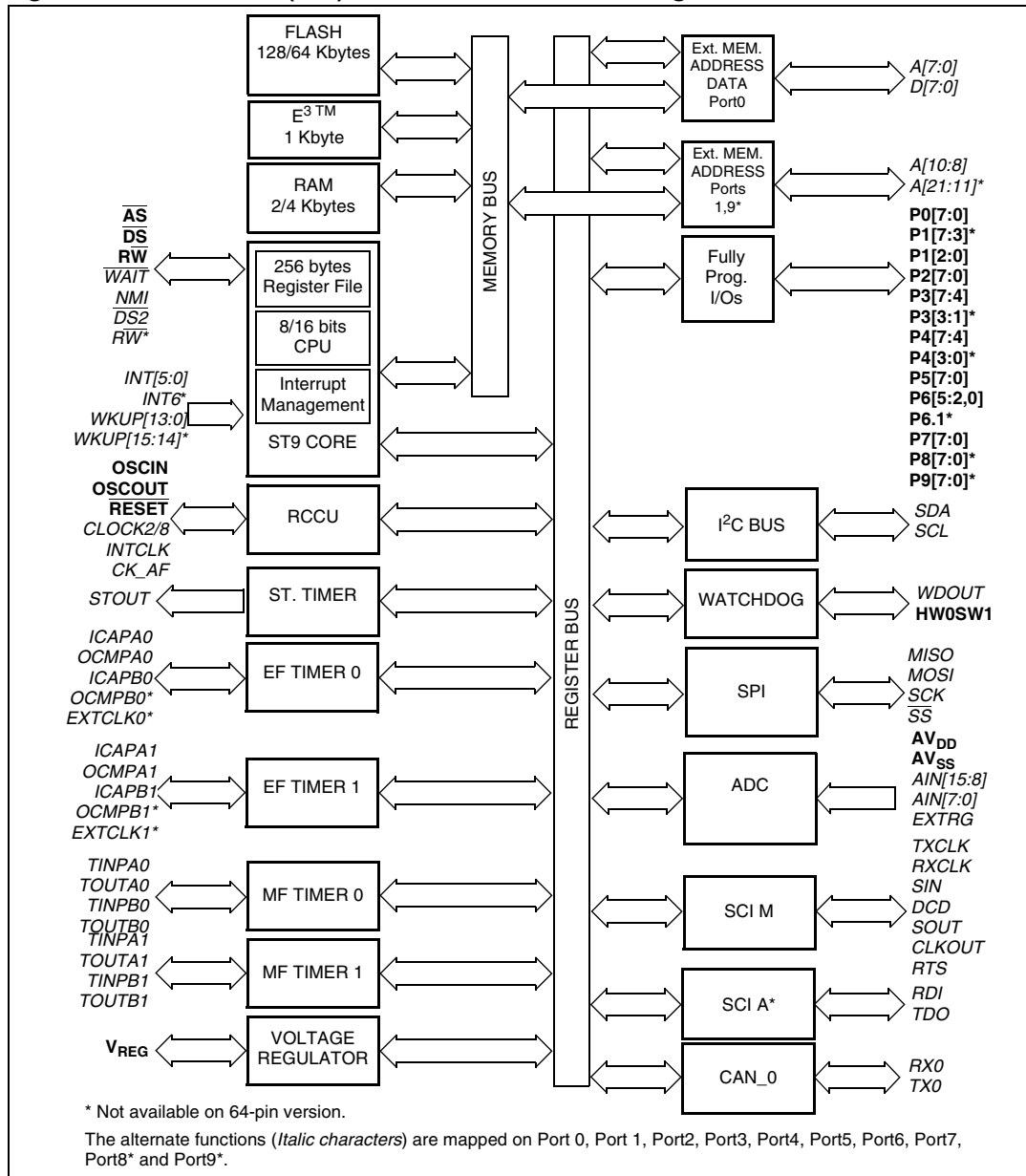


Figure 4. ST92F150JDV1: Architectural block diagram

