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## MPEG 2.5 LAYER III AUDIO DECODER SUPPORTING CD-ROM CAPABILITY

PRODUCT PREVIEW

### 1 FEATURES

- SINGLE CHIP MPEG LAYER 3 DECODER SUPPORTING:
  - All features specified for Layer III in ISO/IEC 11172-3 (MPEG 1 Audio)
  - All features specified for Layer III in ISO/IEC 13818-3.2 (MPEG 2 Audio)
  - Lower sampling frequencies syntax extension, (not specified by ISO) called MPEG 2.5
- DECODES LAYER III STEREO CHANNELS, DUAL CHANNEL, SINGLE CHANNEL (MONO)
- SUPPORTING ALL THE MPEG 1 & 2 SAMPLING FREQUENCIES AND THE EXTENSION TO MPEG 2.5:48, 44.1,32, 24,22.05, 16, 12,11.025, 8 KHz
- ACCEPTS MPEG 2.5 LAYER III ELEMENTARY COMPRESSED BITSTREAM WITH DATA RATE FROM 8 Kbit/s UP TO 320 Kbit/s
- BYPASS MODE FOR EXTERNAL AUXILIARY AUDIO SOURCE
- EMBEDDED ISO9660 LAYER FOR FILE-SYSTEM DECODING (JOLIET)
- EMBEDDED CD-ROM DECODER BLOCKS INCLUDING ECC/EDC CAPABILITY
- FLEXIBLE I<sup>2</sup>S INPUT INTERFACE FOR EASY CONNECTION WITH MOST CD-SERVO DEVICES
- EMBEDDED BROWSING COMMAND INTERPRETER FOR EASY FILE-SYSTEM BROWSING
- CUE-SHEET CAPABILITY UP TO 100 ENTRIES
- BROWSER COMMAND INTERPRETER (BCI)
  - Parent Dir
  - Enter Dir
  - Previous Entry
  - Next Entry
  - Get Record Infos
- EASY PROGRAMMABLE GPSO INTERFACE (MONO/STEREO) FOR ENCODED DATA UP TO 5Mbit/s
- DIGITAL VOLUME

STA016A/STA016AA

Figure 1. Package

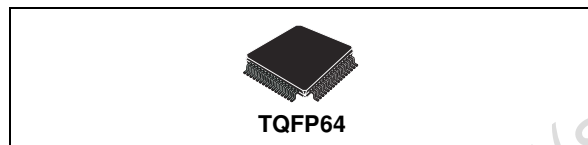


Table 1. Order Codes

Part Number	Package
STA016A	TQFP64

- BASS & TREBLE CONTROL
- SERIAL BITSTREAM INPUT INTERFACE
- EASY PROGRAMMABLE ADC INPUT INTERFACE
- SERIAL PCM OUTPUT INTERFACE (I<sup>2</sup>S AND OTHER FORMATS)
- PLL FOR INTERNAL CLOCK AND FOR OUTPUT PCM CLOCK GENERATION
- CRC CHECK AND SYNCHRONISATION ERROR DETECTION WITH SOFTWARE INDICATORS
- I<sup>2</sup>C CONTROL BUS
- LOW POWER 2.4V CMOS TECHNOLOGY WITH 3.3V TOLERANT AND CAPABLE I/O
- FAST FORWARD AND PAUSE CAPABILITIES
- ADDITIONAL FEATURES AVAILABLE VIA SOFTWARE
  - MMC and SD card: read and format via SPI
  - MMC and SD cards: write
  - Sample Rate Converter for MPEG streams: from general input frequency to internal 44.1kHz
  - Generic features
  - Faster browsing, feed forward and rewind capabilities
  - long file name support

### 1.1 APPLICATIONS

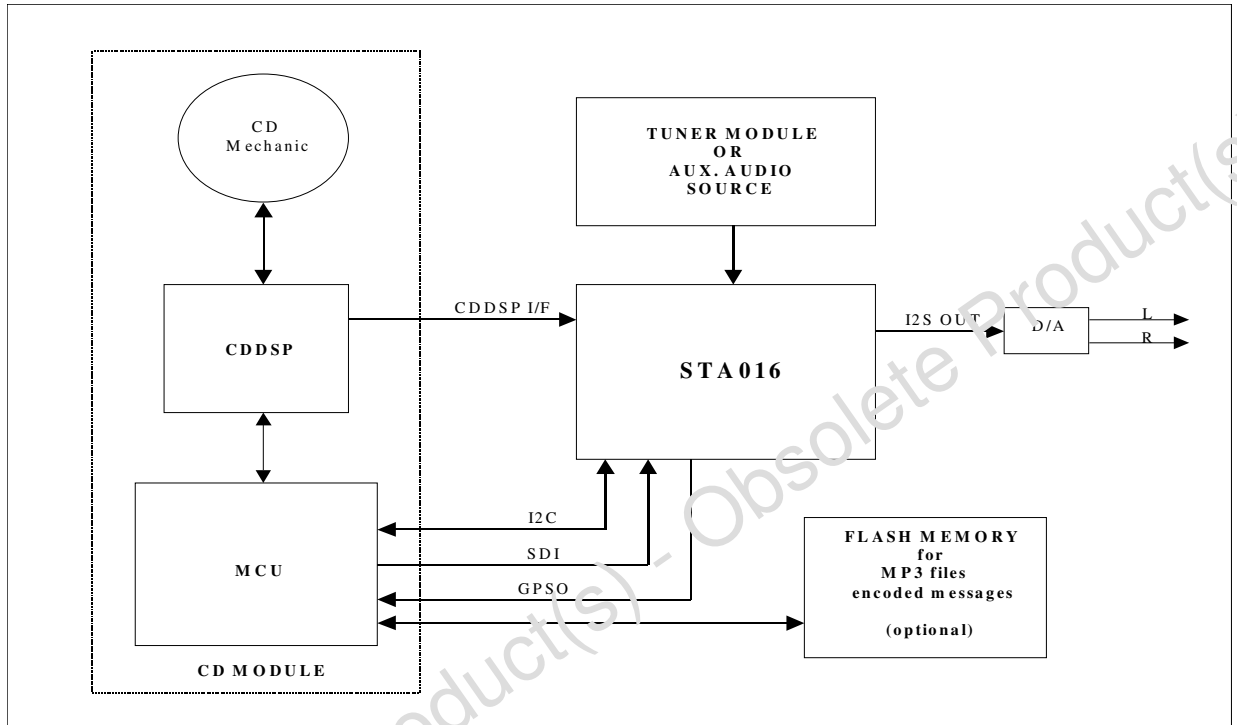
- AUDIO CD PLAYERS
- MULTIMEDIA PLAYERS
- CD-ROM PLAYERS
- CAR RADIO PLAYERS

## 2 DESCRIPTION

The STA016A is a single chip MPEG 1, 2 and 2.5 Layer III audio decoder with embedded CDDSP decoding capability. It can be easily connected to most existing CDDSP devices via a software configurable serial link. A typical application block diagram is shown in Figure 1. The audio sources, for instance could be an external flash memory.

A useful bypass mode allows using this device also as an audio processor for volume and tone controls.

**Figure 2. Typical CD-Player application**



**Table 2. ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	Digital Power Supply at 2.5V (nominal)	-0.5 to 3.3	V
V <sub>CC</sub>	Digital Power Supply at 3.3V (nominal)	-0.5 to 4	V
V <sub>L-V<sub>CC</sub></sub>	Analog Supply Voltage at 2.5V (nominal)	-0.5 to 3.3	V
V <sub>IH/VIL</sub>	Voltage on input pins (3.3V pads)	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>stg</sub>	Storage Temperature	-40 to +150	°C
T <sub>op</sub>	Operative ambient temp	-40 to +85(*)	°C
T <sub>j</sub>	Operating Junction Temperature	-40 to 125	°C

(\*) guarantee by design

**Table 3. THERMAL DATA**

Symbol	Parameter	Value	Unit
R <sub>th j-amb</sub>	Thermal resistance Junction to Ambient	85	°C/W

### 3 OVERVIEW

The device can decode/process data coming from three possible sources, as showed in Figure 2:

- **CDDSP serial link:** using this input interface, besides MP3 encoded data CD, it's possible to playback also standard Audio CD using the available volume and tone equalizer features of the device and allowing the use of only one D/A converter with no external analog switch.
- **SDI input interface:** through this input interface it's possible to decode any MP3 bitstream coming, for instance, from an external flash memory.
- **I<sup>2</sup>S input interface:** this interface can be used to process an external audio source (tuner, for instance) through the DSP based volume and tone controls: this BYPASS mode can avoid the use of additional D/A converters or postprocessing units.

#### 3.1 MP3 decoder engine

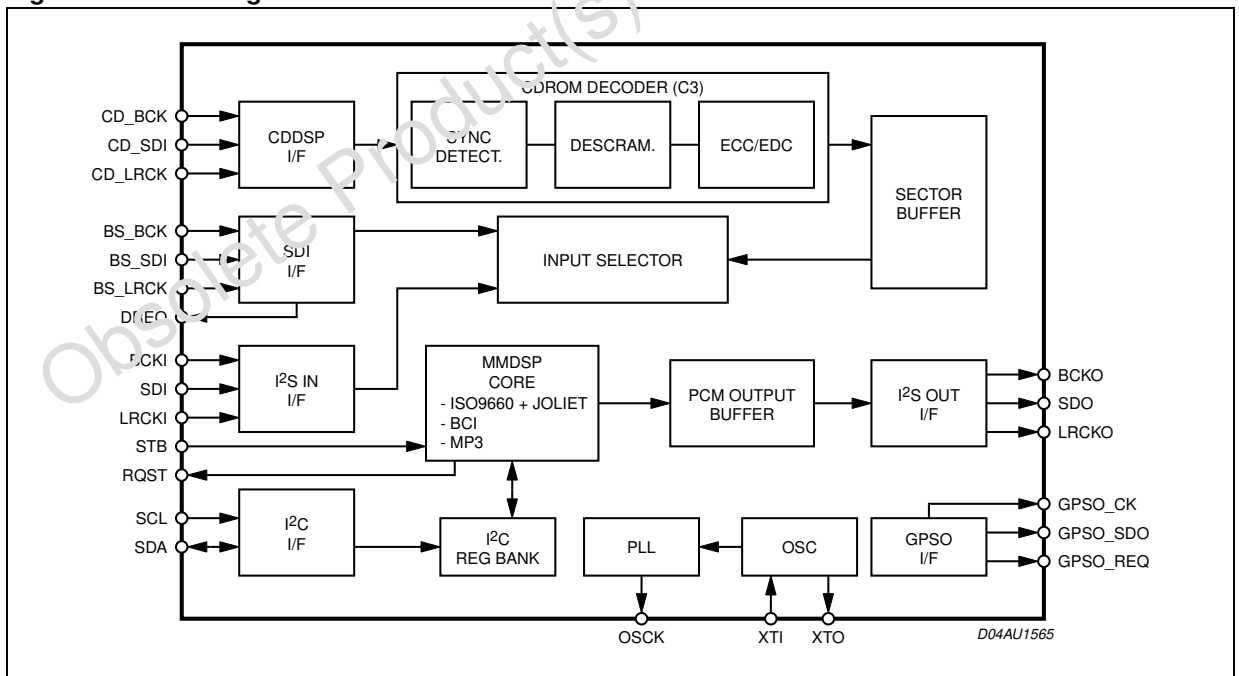
The MP3 decoder engine is able to decode any Layer III compliant bitstream: MPEG1, MPEG2 and MPEG 2.5 streams are supported.

Decoded audio data goes through a software volume control and a two-band equalizer blocks before feeding the output I<sup>2</sup>S interface. This results in no need for an external audio processor.

**Table 4. MPEG Sampling Rates (KHz)**

MPEG 1	MPEG 2	MPEG 2.5
48	24	12
44.1	22.05	11.025
32	16	8

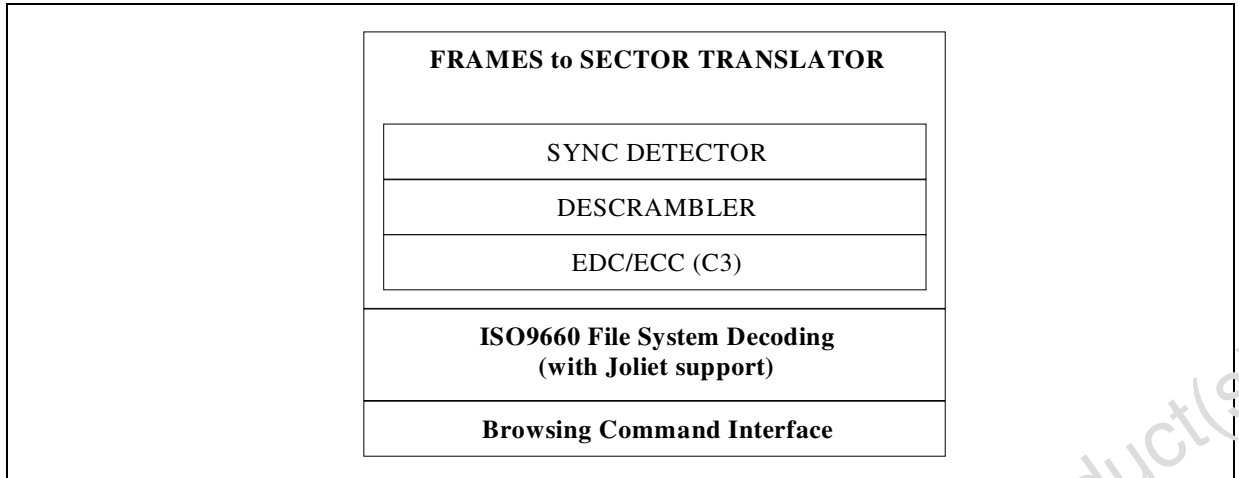
**Figure 3. Block Diagram**



The basic functions of the device can be fully operated via the I<sup>2</sup>C bus. Besides that the GPSO interface can be used to move huge amount of data this fast and flexible interface can achieve transfer rates up to 5 Mbit/s.

The embedded DSP firmware implements all the layers required to decode a standard data CD, as shown in the Figure 4:

Figure 4. Layers performed by embedded DSP firmware



The whole CDROM and file-system decoding task is performed by embedded firmware. The application MCU, basically, must manage CDDSP device according to STA016A requests. Three basic command flows exist:

- MCU -> STA016A: commands used to handle decoder operation and to ask for specific information like filename, filelength, sector raw data, etc. This flow will use I<sup>2</sup>C (GPSC for special operations) interface.
- STA016A -> MCU: this channel is used to retrieve inquired information and to inform MCU that a CDDSP specific operation must be performed (like pick-up repositioning). This flow is based on I<sup>2</sup>C link plus an additional interrupt signal in order to avoid time consuming polling techniques.
- MCU -> CDDSP: the CDDSP management is fully up to the application MCU. This architecture allows maximum flexibility and easy migration from existing CDPlayers to MP3 CDPlayers.

Figure 5. PIN CONNECTION

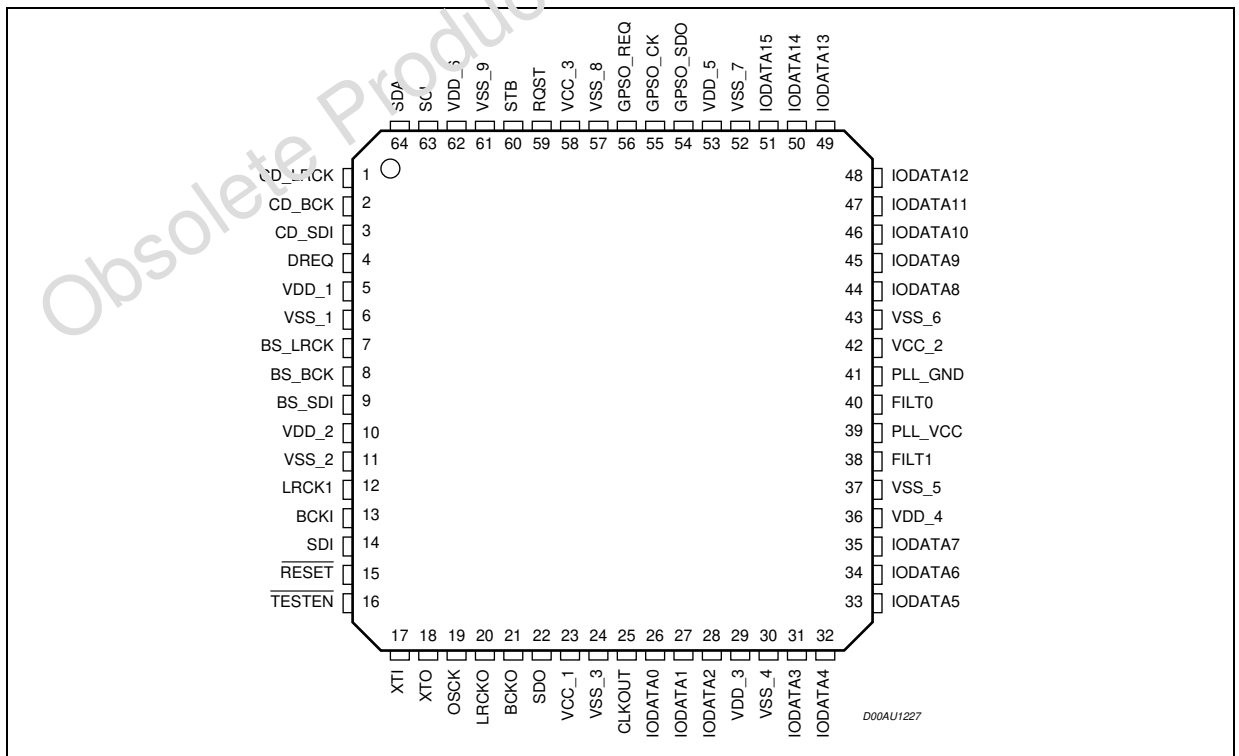


Table 5. PIN DESCRIPTION

PIN	Pin Name	Type	Description	Source/Dest
<b>CDDSP interface</b>				
1	CD_LRCK	I	DSP Interface left/right Clock	From DSP
3	CD_SDI	I	DSP interface serial data	From DSP
2	CD_BCK	I	DSP interface bit clock	From DSP
<b>SDI interface</b>				
9	BS_SDI	I	Bitstream interface serial data	From MCU
7	BS_LRCK	I	Bitstream interface left/right Clock	From MCU
8	BS_BCK	I	Bitstream interface clock	From MCU
4	DREQ	O	Bitstream data request	To MCU
<b>PCM IN interface</b>				
13	BCKI	I	ADC bit clock	From ADC
14	SDI	I	ADC serial data	From ADC
12	LRCKI	I	ADC left/right Clock	From ADC
<b>PCM OUT interface</b>				
20	LRCKO	O	DAC Interface left/right Clock	To DAC
22	SDO	O	DAC serial data	To DAC
21	BCKO	O	DAC bit clock	To DAC
19	OSCK	O	DAC oversampling clock	To DAC/ADC
<b>GPSO interface</b>				
55	GPSO_CK	I	GPSO bit clock	From MCU
54	GPSO_SDO	O	GPSO serial data	To MCU
56	GPSO_REQ	O	GPSO request signal	To MCU
<b>GPIO interface</b>				
26	IODATA0	I/O	GPIO DATA0	
27	IODATA1	I/O	GPIO DATA1	
28	IODATA2	I/O	GPIO DATA2	
31	IODATA3	I/O	GPIO DATA3	
32	IODATA4	I/O	GPIO DATA4	
33	IODATA5	I/O	GPIO DATA5	
34	IODATA6	I/O	GPIO DATA6	
35	IODATA7	I/O	GPIO DATA7	
44	IODATA8	I/O	GPIO DATA8	
45	IODATA9	I/O	GPIO DATA9	
46	IODATA10	I/O	GPIO DATA10	
47	IODATA11	I/O	GPIO DATA11	
48	IODATA12	I/O	GPIO DATA12	
49	IODATA13	I/O	GPIO DATA13	
50	IODATA14	I/O	GPIO DATA14	
51	IODATA15	I/O	GPIO DATA15	

Table 5. PIN DESCRIPTION (continued)

PIN	Pin Name	Type	Description	Source/Dest
<b>HANDSHAKE SIGNALS</b>				
60	STB	I	Strobe signal	From MCU
59	RQST	O	I2C data signal	To MCU
<b>I<sup>2</sup>C LINK</b>				
63	SCL	I	I2C clock signal	From MCU
64	SDA	I/O	I2C data signal	To MCU
<b>MISCELLANEOUS</b>				
17	XTI	I	Oscillator input	
18	XTO	O	Oscillator output	
25	CLKOUT	O	Buffered output clock	
15	-RESET	I	Reset	
16	-TESTEN	I	Reserved for test purpose	
40	FILT0	I	PLL external filter	
38	FILT1		PLL external filter	
<b>POWER SUPPLY</b>				
39	PLL_VCC		Digital supply (2.5V Power Supply)	
41	PLL_GND		Ground	
5	VDD_1		Digital supply (2.5V Power Supply)	
10	VDD_2		Digital supply (2.5V Power Supply)	
29	VDD_3		Digital supply (2.5V Power Supply)	
36	VDD_4		Digital supply (2.5V Power Supply)	
53	VDD_5		Digital supply (2.5V Power Supply)	
62	VDD_6		Digital supply (2.5V Power Supply)	
23	VCC_1		Digital supply (3.3V Power Supply)	
42	VCC_2		Digital supply (3.3V Power Supply)	
58	VCC_3		Digital supply (3.3V Power Supply)	
6	VSS_1		Ground	
11	VSS_2		Ground	
24	VSS_3		Ground	
30	VSS_4		Ground	
37	VSS_5		Ground	
43	VSS_6		Ground	
52	VSS_7		Ground	
57	VSS_8		Ground	
61	VSS_9		Ground	

## 4 ELECTRICAL CHARACTERISTICS

( $T_{amb} = 25^{\circ}\text{C}$ ;  $R_g = 50\Omega$  unless otherwise specified)

**Table 6. DC OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Power Supply Voltage	$2.5 \pm 0.25$	V
$V_{CC}$	Power Supply Voltage	$3.3 \pm 0.3$	V
PLL_ $V_{CC}$	Power Supply Voltage	$2.5 \pm 0.25$	V

**Table 7. GENERAL INTERFACE ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
$I_{IL}$	Low Level Input Current Without pull-up device	$V_i = 0\text{V}$	-10		10	$\mu\text{A}$	1
$I_{IH}$	High Level Input Current Without pull-up device	$V_i = V_{DD}$	-10		10	$\mu\text{A}$	1
$V_{esd}$	Electrostatic Protection	Leakage $< 1\mu\text{A}$	2000			V	2

**Note 1:** The leakage currents are generally very small,  $< 1\text{nA}$ . The value given here is a maximum that can occur after an electrostatic stress on the pin.

**Note 2:** Human Body Model.

**Table 8. DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
$V_{IL}$	Low Level Input Voltage				$0.2 \cdot V_{CC}$	V	
$V_{IH}$	High Level Input Voltage		$0.8 \cdot V_{CC}$			V	
$V_{OL}$	Low Level Output Voltage	$I_{ol} = X\text{ma}$			0.4V	V	1, 2
$V_{OH}$	High Level Output Voltage		$0.85 \cdot V_{CC}$			V	1, 2

**Note1:** Takes into account 200mV voltage drop in both supply lines.

**Note 2:** X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

**Table 9.**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
$I_{pu}$	Pull-up current	$V_i = 0\text{V}$ ; pin numbers 7, 24 and 26	-25	-66	-125	$\mu\text{A}$	1
$R_{pu}$	Equivalent Pull-up Resistance			50		$\text{k}\Omega$	

Note 1: Min. condition:  $V_{DD} = 2.7\text{V}$ ,  $125^{\circ}\text{C}$  Min process Max. condition:  $V_{DD} = 3.6\text{V}$ ,  $-20^{\circ}\text{C}$  Max.

**Table 10. POWER DISSIPATION**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
$P_D$	Power Dissipation@ $V_{DD} = 2.4\text{V}$	Sampling_freq $\leq 24\text{ kHz}$		t.b.d.		mW	
		Sampling_freq $\leq 32\text{ kHz}$		t.b.d.		mW	
		Sampling_freq $\leq 48\text{ kHz}$		t.b.d.		mW	



## 5 HOST REGISTERS

The following table gives a description of STA016A register list.

The STA016A device includes 256 I<sup>2</sup>C registers. In this document, only the user-oriented registers are described. The undocumented registers are reserved or unused. These registers must never be accessed (in Read or in Write mode). The Read-Only registers must never be written

We can split the data flux in different time periods (see following diagram) meanwhile host registers can be read or written :

- DWT : During Whole Time (at any time during process).
- DEC : During External Config (period between RUN=2 and RUN=1).
- DBO : During Boot (period between RUN=0 and RUN=2).
- ABO : After B0ot (period after RUN=1).
- AEC : After External Config (period after RUN=2).
- EDF : Every Decoded Frame (each time a frame has been decoded).
- EDB : Every Decoded Block (each time a block has been decoded).

Figure 6.

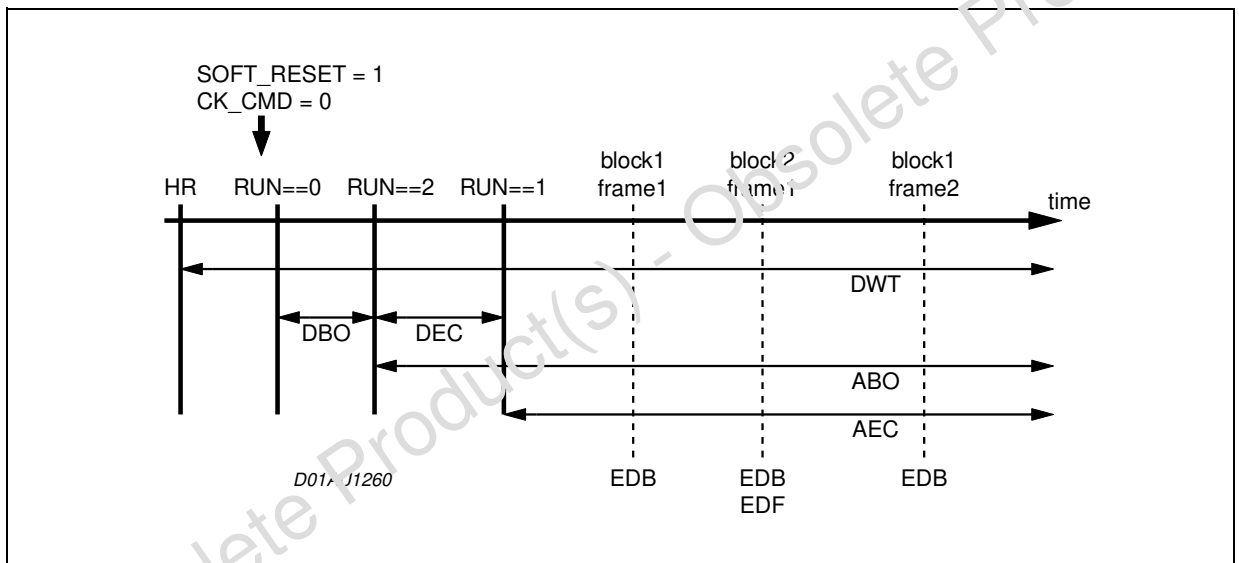


Table 11. REGISTER MAP BY FUNCTION

Register function	Hex	Dec	Name	Type	When
VERSION	0x00	0	VERSION	RO	DWT
	0x01	1	IDENT	RO	DWT
	0xD3	211	SOFT_VERSION	RO	DWT
PLL_AUDIO_CONFIGURATION	0xDC	220	PLL_AUDIO_PEL_192	RW	DEC
	0xDD	221	PLL_AUDIO_PEH_192	RW	DEC
	0xDE	222	PLL_AUDIO_NDIV_192	RW	DEC
	0xDF	223	PLL_AUDIO_XDIV_192	RW	DEC
	0xE0	224	PLL_AUDIO_MDIV_192	RW	DEC
	0xE1	225	PLL_AUDIO_PEL_176	RW	DEC
	0xE2	226	PLL_AUDIO_PEH_176	RW	DEC
	0xE3	227	PLL_AUDIO_NDIV_176	RW	DEC
	0xE4	228	PLL_AUDIO_XDIV_176	RW	DEC
	0xE5	229	PLL_AUDIO_MDIV_176	RW	DEC
PLL_SYSTEM_CONFIGURATION	0xE6	230	PLL_SYSTEM_PEL_50	RW	DEC
	0xE7	231	PLL_SYSTEM_PEH_50	RW	DEC
	0xE8	232	PLL_SYSTEM_NDIV_50	RW	DEC
	0xE9	233	PLL_SYSTEM_XDIV_50	RW	DEC
	0xEA	234	PLL_SYSTEM_MDIV_50	RW	DEC
	0xEB	235	PLL_SYSTEM_PEL_42_5	RW	DEC
	0xEC	236	PLL_SYSTEM_PEH_42_5	RW	DEC
	0xED	237	PLL_SYSTEM_NDIV_42_5	RW	DEC
	0xEE	238	PLL_SYSTEM_XDIV_42_5	RW	DEC
	0xEF	239	PLL_SYSTEM_MDIV_42_5	RW	DEC
I2Sout_CONFIGURATION	0x66	102	OUTPUT_CONF	RW	DEC
	0x67	103	PCM_DIV	RW	DEC
	0x68	104	PCM_CONF	RW	DEC
	0x69	105	PCM_CROSS	RW	DEC
GPSO_CONFIGURATION	0x66	102	OUTPUT_CONF	RW	DEC
	0x6A	106	GPSO_CONF	RW	DEC
I2Sin_CONFIGURATION	0x5A	90	INPUT_CONF	RW	DEC
	0x5B	91	I_AUDIO_CONFIG_1	RW	DEC
	0x5C	92	I_AUDIO_CONFIG_2	RW	DEC
	0x5D	93	I_AUDIO_CONFIG_3	RW	DEC

Register function	Hex	Dec	Name	Type	When
CDBSA_CONFIGURATION	0x5A	90	INPUT_CONF	RW	DEC
	0x5B	91	I_AUDIO_CONFIG_1	RW	DEC
	0x5C	92	I_AUDIO_CONFIG_2	RW	DEC
	0x5D	93	I_AUDIO_CONFIG_3	RW	DEC
	0x5E	94	I_AUDIO_CONFIG_4	RW	DEC
	0x5F	95	I_AUDIO_CONFIG_5	RW	DEC
	0x60	96	I_AUDIO_CONFIG_6	RW	DEC
	0x61	97	I_AUDIO_CONFIG_7	RW	DEC
	0x62	98	I_AUDIO_CONFIG_8	RW	DEC
	0x63	99	I_AUDIO_CONFIG_9	RW	DEC
	0x64	100	I_AUDIO_CONFIG_10	RW	DEC
	0x65	101	I_AUDIO_CONFIG_11	RW	DEC
BSB_CONFIGURATION	0x59	89	POL_REQ	RW	DEC
	0x5A	90	INPUT_CONF	RW	DEC
	0x5B	91	I_AUDIO_CONFIG_1	RW	DEC
CD_CONFIGURATION	0x40	64	BASIC_COMMAND	WO	AEC
	0x41	65	FAST_FUNCTION_VAL	RW	ABO
	0x42	66	REQUIRED_TRACK	RW	ABO
	0x43	67	REQUIRED_DIR	RW	ABO
	0x44	68	PLAY_MODE	RW	ABO
	0x46	70	TYPE_CD_EXT_REQ	RO	AEC
	0x47	71	MINUTE_REQ	RO	AEC
	0x48	72	SECOND_REQ	RO	AEC
	0x49	73	SECTOR_REQ	RO	AEC
	0x4A	74	MINUTE_SPENT	RO	AEC
	0x4B	75	SECOND_SPENT	RO	AEC
	0x4C	76	SCANNING_TIME	RW	ABO
	0x4D	77	PLAY_LIST_INDEX	RW	ABO
	0x4E	78	PLAY_LIST_VALUE	RW	ABO

Register function	Hex	Dec	Name	Type	When
	0x86	134	CD_SONG_INFO_C1	RO	AEC
	0x87	135	CD_SONG_INFO_C2	RO	AEC
	0x88	136	CD_SONG_INFO_C3	RO	AEC
	0x89	137	CD_SONG_INFO_C4	RO	AEC
	0x8A	138	CD_SONG_INFO_C5	RO	AEC
	0x8B	139	CD_SONG_INFO_C6	RO	AEC
	0x8C	140	CD_SONG_INFO_C7	RO	AEC
	0x8D	141	CD_SONG_INFO_C8	RO	AEC
	0x8E	142	CD_SONG_INFO_C9	RO	AEC
	0x8F	143	CD_SONG_INFO_C10	RO	AEC
	0x90	144	CD_SONG_INFO_C11	RO	AEC
	0x91	145	CD_SONG_INFO_C12	RO	AEC
	0x92	146	CD_SONG_INFO_C13	RO	AEC
	0x93	147	CD_SONG_INFO_C14	RO	AEC
	0x94	148	CD_SONG_INFO_C15	RO	AEC
	0x95	149	CD_SONG_INFO_C16	RO	AEC
	0x96	150	CD_SONG_INFO_C17	RO	AEC
	0x97	151	CD_SONG_INFO_C18	RO	AEC
	0x98	152	CD_SONG_INFO_C19	RO	AEC
	0x99	153	CD_SONG_INFO_C20	RO	AEC
	0x9A	154	CD_SONG_INFO_C21	RO	AEC
	0x9B	155	CD_SONG_INFO_C22	RO	AEC
	0x9C	156	CD_SONG_INFO_C23	RO	AEC
	0x9D	157	CD_SONG_INFO_C24	RO	AEC
	0x9E	158	CD_SONG_INFO_C25	RO	AEC
	0x9F	159	CD_SONG_INFO_C26	RO	AEC
	0xA0	160	CD_SONG_INFO_C27	RO	AEC
	0xA1	161	CD_SONG_INFO_C28	RO	AEC
	0xA2	162	CD_SONG_INFO_C29	RO	AEC
	0xA3	163	CD_SONG_INFO_C30	RO	AEC
	0xA4	164	CD_SONG_INFO_C31	RO	AEC
	0xA5	165	CD_SONG_INFO_C32	RO	AEC
	0xA6	166	CD_SONG_TYPE_INFO	RO	AEC

Register function	Hex	Dec	Name	Type	When
	0xA7	167	NB_OF_CUR_TRACK	RO	AEC
	0xA8	168	NB_OF_CUR_DIR	RO	AEC
	0xA9	169	CD_CUR_STATUS	RO	AEC
	0xAA	170	CD_TRACK_FORMAT	RO	AEC
	0xAB	171	CD_NB_OF_SUB_DIR	RO	AEC
	0xAC	172	CD_NB_OF_SUB_FILE	RO	AEC
	0xAD	173	DIRECTORY_LEVEL	RO	AEC
	0xAE	174	DIR_IDENTIFIER_B1	RO	AEC
	0xAF	175	DIR_IDENTIFIER_B2	RO	AEC
	0xB0	176	DIR_IDENTIFIER_B3	RO	AEC
	0xB1	177	DIR_IDENTIFIER_B4	RO	AEC
	0xB2	178	VOL_IDENTIFIER_B1	RO	AEC
	0xB3	179	VOL_IDENTIFIER_B2	RO	AEC
	0xB4	180	VOL_IDENTIFIER_B3	RO	AEC
	0xB5	181	VOL_IDENTIFIER_B4	RO	AEC
	0xB6	182	EXTRACT_BYTE_IDX_B1	RW	ABO
	0xB7	183	EXTRACT_BYTE_IDX_B2	RW	ABO
	0xB8	184	EXTRACT_BYTE_IDX_B3	RW	ABO
	0xB9	185	EXTRACT_BYTE_IDX_B4	RW	ABO
	0xBA	186	EXTRACT_ADR_MODE	RW	ABO
	0xBC	188	CONFIG_MODULE	RW	DEC
COMMAND	0x10	16	SOFT_RESET	WO	DWT
	0x3A	58	CK_CMD	WO	DBO
	0x55	85	DEC_SEL	RW	DEC
	0x56	86	RUN	RW	DEC
	0x52	82	CRC_IGNORE	RW	ABO
	0x53	83	MUTE	RW	ABO
	0x57	87	SKIP	RW	ABO
	0x58	88	PAUSE	RW	ABO

Register function	Hex	Dec	Name	Type	When
STATUS	0xCC	204	STATUS_MODE	RO	EDF
	0xCD	205	STATUS_CHAN_NB	RO	EDF
	0xCE	206	STATUS_SF	RO	EDF
	0x6F	111	STATUS_FE	RO	EDF
	0xD4	212	HEADER_1	RO	EDF
	0xD5	213	HEADER_2	RO	EDF
	0xD6	214	HEADER_3	RO	EDF
	0xD7	215	HEADER_4	RO	EDF
	0xD8	216	HEADER_5	RO	EDF
	0xD9	217	HEADER_6	RO	EDF
BYPASSA_CONFIGURATION	0x70	112	CHAN_NB	RW	DEC
	0x71	113	SAMPLING_FREQ	RW	DEC
	0xCB	203	PCMCLK_INPUT	RW	DEC
MP3_CONFIGURATION	0x52	82	CRC_IGNORE	RW	ABO
	0x6B	107	ERR_DEC_LEVEL	RO	EDB
	0x6C	108	ERR_DEC_NB_1	RO	EDB
	0x6D	109	ERR_DEC_NB_2	RO	EDB
RESERVED	0x70	112	RESERVED		
	0x71	113	RESERVED		
	0x72	114	RESERVED		
	0x73	115	RESERVED		
	0x74	116	RESERVED		
MIX_CONFIGURATION	0x75	117	MIX_MODE	RW	ABO
	0x76	118	MIX_DLA	RW	ABO
	0x77	119	MIX_DLB	RW	ABO
	0x78	120	MIX_DRA	RW	ABO
	0x79	121	MIX_DRB	RW	ABO
TCNE_CONFIGURATION	0x7A	122	TONE_ON	RW	ABO
	0x7B	123	TONE_FCUTH	RW	ABO
	0x7C	124	TONE_FCUTL	RW	ABO
	0x7D	125	TONE_GAINH	RW	ABO
	0x7E	126	TONE_GAINL	RW	ABO
	0x7F	127	TONE_GAIN_ATTEN	RW	ABO

## 6 REGISTER DESCRIPTION

### 6.1 VERSION registers description

#### 6.1.1 VERSION :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0x00 (0)

Type : RO - DWT

Software Reset : 0x10

Hardware Reset : 0x10

Description :

The VERSION register is Read-only and it is used to identify the IC on the application board.

#### 6.1.2 IDENT :

b7	b6	b5	b4	b3	b2	b1	b0
1	0	1	0	1	1	0	0

Address : 0x01 (1)

Type : RO - DWT

Software Reset : 0xAC

Hardware Reset : 0xAC

Description :

IDENT is a read-only register and it is used to identify the IC on an application board. IDENT always has the value 0xAC.

#### 6.1.3 SOFT\_VERSION :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xD3 (211)

Type : RO - DWT

Software Reset : X

Description :

The SOFT\_VERSION register is Read-only and it is used to identify the software running on the IC.

### 6.2 PLL\_AUDIO\_CONFIGURATION registers description

#### 6.2.1 PLL\_AUDIO\_PEL\_192 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xDC (220)

Type : RW - DEC

Software Reset : 58

Description :

This register must contain a PEL value that enables the audio PLL to generate a frequency of  $ofact \cdot 192$  kHz for the PCMCK. See table 1, 2 & 3.

ofact is the oversampling factor needed by the DAC (ofact==246 or ofact==384).

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

#### 6.2.2 PLL\_AUDIO\_PEH\_192 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xDD (221)

Type : RW - DEC

Software Reset : 187

Description :

This register must contain a PEH value that enables the audio PLL to generate a frequency of  $ofact \cdot 192$  kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

#### 6.2.3 PLL\_AUDIO\_NDIV\_192 :

b7	b6	b5	b4	b3	b2	b1	b0

Address : 0xDE (222)

Type : RW - DEC

Software Reset : 0

**Description :**

This register must contain a NDIV value that enables the audio PLL to generate a frequency of ofact\*192 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

**6.2.4 PLL\_AUDIO\_XDIV\_192 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xDF (223)

Type : RW - DEC

Software Reset : 3

**Description :**

This register must contain a XDIV value that enables the audio PLL to generate a frequency of ofact\*192 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

**6.2.5 PLL\_AUDIO\_MDIV\_192 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE0 (224)

Type : RW - DEC

Software Reset : 12

**Description :**

This register must contain a MDIV value that enables the audio PLL to generate a frequency of ofact\*192 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

**6.2.6 PLL\_AUDIO\_PEL\_176 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE1 (225)

Type : RW - DEC

Software Reset : 54

**Description :**

This register must contain a PEL value that enables the audio PLL to generate a frequency of ofact\*176 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- fact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

**6.2.7 PLL\_AUDIO\_PEH\_176 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE2 (226)

Type : RW - DEC

Software Reset : 118

**Description :**

This register must contain a PEH value that enables the audio PLL to generate a frequency of ofact\*176 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz

**6.2.8 PLL\_AUDIO\_NDIV\_176 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE3 (227)

Type : RW - DEC

Software Reset : 0

**Description :**

This register must contain a NDIV value that enables the audio PLL to generate a frequency of ofact\*176 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :

- ofact == 256
- external crystal provide a CRYCK running at 14.31818 MHz



**6.2.9 PLL\_AUDIO\_XDIV\_176 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE4 (228)  
 Type : RW - DEC  
 Software Reset : 2

**Description :**

This register must contain a XDIV value that enables the audio PLL to generate a frequency of ofact\*176 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :  
 - ofact == 256  
 - external crystal provide a CRYCK running at 14.31818 MHz

**6.2.10 PLL\_AUDIO\_MDIV\_176 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE5 (229)  
 Type : RW - DEC  
 Software Reset : 8

**Description :**

This register must contain a MDIV value that enables the audio PLL to generate a frequency of ofact\*176 kHz for the PCMCK. See table 1, 2 & 3.

Default value at soft reset assume :  
 - ofact == 256  
 - external crystal provide a CRYCK running at 14.31818 MHz

**6.3 PLL\_SYSTEM\_CONFIGURATION registers description**

**6.3.1 PLL\_SYSTEM\_PEL\_50 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE6 (230)  
 Type : RW - DEC  
 Software Reset : 0

**Description :**

This register must contain a PEL value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :  
 - external crystal provide a CRYCK running at 14.31818 MHz

**6.3.2 PLL\_SYSTEM\_PEH\_50 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE7 (231)  
 Type : RW - DEC  
 Software Reset : 0

**Description :**

This register must contain a PEH value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :  
 - external crystal provide a CRYCK running at 14.31818 MHz

**6.3.3 PLL\_SYSTEM\_NDIV\_50 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE8 (232)  
 Type : RW - DEC  
 Software Reset : 0

**Description :**

This register must contain a NDIV value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :  
 - external crystal provide a CRYCK running at 14.31818 MHz

**6.3.4 PLL\_SYSTEM\_XDIV\_50 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE9 (233)  
 Type : RW - DEC  
 Software Reset : 1

Description :

This register must contain a XDIV value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**6.3.5 PLL\_SYSTEM\_MDIV\_50 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xEA (234)

Type : RW - DEC

Software Reset : 13

Description :

This register must contain a MDIV value that enables the system PLL to generate a frequency of 50 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**6.3.6 PLL\_SYSTEM\_PEL\_42\_5**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE6 (230)

Type : RW - DEC

Software Reset : 126

Description :

This register must contain a PEL value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**6.3.7 PLL\_SYSTEM\_PEH\_42\_5 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE7 (231)

Type : RW - DEC

Software Reset : 223

Description :

This register must contain a PEH value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**6.3.8**

**6.3.9 PLL\_SYSTEM\_NDIV\_42\_5 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE8 (232)

Type : RW - DEC

Software Reset : 0

Description :

This register must contain a NDIV value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**6.3.10 PLL\_SYSTEM\_XDIV\_42\_5 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xE9 (233)

Type : RW - DEC

Software Reset : 1

Description :

This register must contain a XDIV value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**6.3.11 PLL\_SYSTEM\_MDIV\_42\_5 :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0xEA (234)

Type : RW - DEC  
 Software Reset : 10

Description :

This register must contain a MDIV value that enables the system PLL to generate a frequency of 42.5 MHz for the SYSCK. See table 4.

Default value at soft reset assume :

- external crystal provide a CRYCK running at 14.31818 MHz

**6.4 I<sup>2</sup>Sout\_CONFIGURATION registers description**

**6.4.1 OUTPUT\_CONF :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x66 (102)

Type : RW - DEC

Software Reset : 0

Description :

If set to 1 enable the configurability of the PCM-BLOCK Output thanks to following registers, else disable this configurability and take embedded default configuration for PCM-BLOCK registers

Note that this embedded default configuration can be retrieved by user thanks to following setting :

- PCM\_DIV = 3;
- PCM\_CONF = 0;
- PCM\_CROSS = 0;

**6.4.2 PCM\_DIV :**

b7	b6	b5	b4	b3	b2	b1	b0
0	0	DV5	DV4	DV3	DV2	DV1	DV0

Address : 0x67 (103)

Type : RW - DEC

Software Reset : 0

Description :

If OUTPUT\_CONF == 1, configure the divider to generate the bit clock of the I2Sout interface, called BCK0, from PCMCK. according the following relation :  $BCK0 = PCMCK / 2 * (PCM\_DIV + 1)$

**6.4.3 PCM\_CONF :**

b7	b6	b5	b4	b3	b2	b1	b0
0	CO6	CO5	CO4	CO3	CO2	CO1	CO0

Address : 0x68 (104)

Type : RW - DEC

Software Reset : 0

Description :

If OUTPUT\_CONF == 1, configure the I2Sout interface according following table

**Table 12. .**

Bit fields	Comment
CO[1:0]	0 : 16 bits mode (16 slots transmitted). 1 : 18 bits mode (18 slots transmitted). 2 : 20 bits mode (20 slots transmitted). 3 : 24 bits mode (24 slots transmitted).
CO2	Polarity of BCKO : 0 : data are sent on the falling edge & stable on the rising). 1 : (data are sent on the rising edge & stable on the falling).
CO3	0 : I2S format is selected 1 : other format is selected
CO4	Polarity of LRCKO : 0 : low->right, high->left). 1 : low->left, high->right so compliant to I2S format ).
CO5	0 : data are in the last BCKO cycles of LRCKO (right aligned data). 1 : data are in the first BCKO cycles of LRCKO (left aligned data).
CO6	0 : the transmission is LS bit first. 1 : the transmission is MS bit first.

**6.4.4 PCM\_CROSS :**

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	CR1	CR0

Address : 0x69 (105)

Type : RW - DEC

Software Reset : 0

Description :

If OUTPUT\_CONF == 1, CR[1:0] is used to configure

the output crossbar according following table

Table 13. .

CR1	CR0	Comment
0	0	Left channel is mapped on the left output. Right channel is mapped on the right output.
0	1	Left channel is duplicated on both output channels.
1	0	Right channel is duplicated on both output channels.
1	1	Right and left channels are toggled.

## 6.5 GPSO\_CONFIGURATION registers description

### 6.5.1 OUTPUT\_CONF :

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	OC2	OC1	OC0

Address : 0x66 (102)

Type : RW - DEC

Software Reset : 0

Description

Table 14. :

Bit fields	Comment
OC0	Configuration of gpso : 0 : take embedded default configuration. 1 : configure gpso from register GPSO_CONF.
OC1	Use of block PCM to generate clocks (PCMCK, LRCK & BCK): 0 : no use. 1 : use it.
OC2	Configuration of PCM block: 0 : take embedded default configuration. 1 : configure PCM block from PCM_DIV & PCM_CONF registers.

Note that embedded default configuration for GPSO can be retrieved by user thanks to following setting :

- GPSO\_CONF = b00000011;

Note that embedded default configuration for PCM block is described at previous chapter.

### 6.5.2 GPSO\_CONF :

b7	b6	b5	b4	b3	b2	b1	b0
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0

Address : 0x6A (106)

Type : RW - DEC

Software Reset : 0

Description :

If OUTPUT\_CONF == 1, this register configure the GPSO interface

Table 15. .

Bit fields	Comment
CF0	Polarity of GPSO_CK : 0 : data provided on rising edge & stable on falling edge 1 : data provided on falling edge & stable on rising edge
CF1	Polarity of GPSO_REQ : 0 : data are valid when GPSO_REQ is high 1 : data are valid when GPSO_REQ is low
CF[7:2]	Reserved : to be set to 0.

## 6.6 I<sup>2</sup>Sin\_CONFIGURATION registers description

### 6.6.1 INPUT\_CONF :

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x5A (90)

Type : RW - DEC

Software Reset : 0

Description :

If set to 1 enable the configurability of the I2Sin Input thanks to following registers, else disable this configurability and take embedded default configuration for I2Sin registers.

Note that this embedded default configuration can be retrieved by user thanks to following setting :

- I\_AUDIO\_CONFIG\_1 = b00000110;
- I\_AUDIO\_CONFIG\_2 = b11100000;
- I\_AUDIO\_CONFIG\_3 = b00000001;

6.6.2 I\_AUDIO\_CONFIG\_1:

b7	b6	b5	b4	b3	b2	b1	b0
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0

Address : 0x5B (91)  
 Type : RW - DEC  
 Software Reset : 0

Description :  
 If INPUT\_CONF == 1, this register configure the I2Sin interface

Table 16. .

Bit fields	Comment
CF0	Relative synchro : 0 : synchro with first data bit 1 : synchro one bit before first data bit
CF1	Data reception configuration : 0 : LSB first 1 : MSB first
CF2	Polarity of bit clock BCK : 0 : data provided on falling edge & stable on rising edge. 1 : data provided on rising edge & stable on falling edge
CF3	Polarity of LR clock LRCK : 0 : negative 1 : positive
CF4	Start value of LRCK : combined with CF3, this bit enable user to determine left/right couple according to the following table.
CF[7:5]	Reserved : to be set to 0.

Table 17.

CF3	CF4	Left/Right couples
0	0	(data1/data2), (data3/data4),...
1	0	(data0/data1), (data2/data3),...
0	1	(data0/data1), (data2/data3),...
1	1	(data1/data2), (data3/data4),...

6.6.3 I\_AUDIO\_CONFIG\_2 :

b7	b6	b5	b4	b3	b2	b1	b0
LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0

Address : 0x5C (92)  
 Type : RW - DEC  
 Software Reset : 0

Description :  
 See I\_AUDIO\_CONFIG\_3 register description..

6.6.4 I\_AUDIO\_CONFIG\_3 :

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	LR9	LR8

Address : 0x5D (93)  
 Type : RW - DEC  
 Software Reset : 0

Description :  
 If INPUT\_CONF == 1, this register is used to configure the phase of the LRCK of the I<sup>2</sup>Sin.

Table 18.

Bit fields	Comment
LR[4:0]	Position of the data within the LRCK phase : - if CF1 = 0 (LSB), value must be set to [31 - SL[9:5] - bit position of the first bit of data within the LRCK phase]. - if CF1 = 1 (MSB), value must be set to bit position of the first bit of data within the LRCK phase. Note that range of value for this bit position is [0:31].
LR[9:5]	Length-1 of the data. Max value is 31.
LR[15:10]	Reserved : to be set to 0

## 6.7 CDBSA\_CONFIGURATION registers description

### 6.7.1 INPUT\_CONF :

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x5A (90)

Type : RW - DEC

Software Reset : 0

Description :

If set to 1 enable the configurability of the CD & BS input interfaces in audio mode thanks to following registers, else disable this configurability and take embedded default configuration.

Note that this embedded default configuration can be retrieved by user thanks to following setting :

- I\_AUDIO\_CONFIG1 = b00010010;  
// clocks in input  
// & polarity negative
- I\_AUDIO\_CONFIG2 = b00110010;  
// synchro with first data bit  
// data unsigned, MSB first
- I\_AUDIO\_CONFIG3 = b11001111;  
// LRCK phase length is 1
- I\_AUDIO\_CONFIG4 = b00000011;  
// LRCK phase length is 16
- I\_AUDIO\_CONFIG5 = 0xFF;  
// received 16 bits
- I\_AUDIO\_CONFIG6 = 0xFF;  
// received 16 bits
- I\_AUDIO\_CONFIG7 = 0x00;  
// received 16 bits
- I\_AUDIO\_CONFIG8 = 0x00;  
// received 16 bits
- I\_AUDIO\_CONFIG9 = 16;  
// data size is 16
- I\_AUDIO\_CONFIG10 = 0x00;  
// no use because clock in input
- I\_AUDIO\_CONFIG11 = 0x00;  
// no use because clock in input

### 6.7.2 \_AUDIO\_CONFIG\_1 :

b7	b6	b5	b4	b3	b2	b1	b0
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0

Address : 0x5B (91)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, this register is used to configure CD & BS input interfaces in audio mode

Table 19.

Bit	Comment
CF0	Reserved : to be set to 0
CF1	Reserved : to be set to 1
CF2	Direction of bit clocks CD_BCK & BS_BCK : 0 : input 1 : output
CF3	Polarity of bit clocks CD_BCK & BS_BCK : 0 : data provided on falling edge & stable on rising edge 1 : data provided on rising edge & stable on falling edge
CF4	Reserved : to be set to 1
CF5	Direction of LR clocks CD_LRCK & BS_LRCK : 0 : input 1 : output
CF6	Polarity of LR clocks CD_LRCK & BS_LRCK : 0 : left sample corresponds to the low level phase of LRCK 1 : left sample corresponds to the high level phase of LRCK
CF7	Reserved : to be set to 0

### 6.7.3 I\_AUDIO\_CONFIG\_2 :

b7	b6	b5	b4	b3	b2	b1	b0
CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8

Address : 0x5C (92)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, this register is used to configure CD & BS input interfaces in audio mode

Table 20. .

Bit	Comment
CF8	Relative synchro : 0 : synchro with first data bit 1 : synchro one bit before first data bit
CF9	Data reception configuration : 0 : LSB first 1 : MSB first
CF10	Arithmetic type of the reception : 0 : unsigned data 1 : signed data
CF11	Bit to select the reference clock used to generate BCK if clocks are in output (CF2=1 & CF5=1). Otherwise this bit is useless. 0 : SYSCK 1 : PCMCK
CF12	Reserved : to be set to 1
CF13	Reserved : to be set to 1
CF14	Reserved : to be set to 0
CF15	Reserved : to be set to 0

6.7.4 I\_AUDIO\_CONFIG\_3 :

b7	b6	b5	b4	b3	b2	b1	b0
LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0

Address : 0x5D (93)

Type : RW - DEC

Software Reset : 0

Description :

See I\_AUDIO\_CONFIG\_4 register description..

6.7.5 I\_AUDIO\_CONFIG\_4 :

b7	b6	b5	b4	b3	b2	b1	b0
LR15	LR14	LR13	LR12	LR11	LR10	LR9	LR8

Address : 0x5E (94)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, this register is used to configure LR clocks (CD\_LRCK & BS\_LRCK) of CD & BS input interfaces in audio mode.

Table 21.

Bit fields	Comment
LR[5:0]	Length-1 of phase 1 of LR clocks CD_LRCK & BS_LRCK. Max value is 31.
LR[11:6]	Length-1 of phase 2 of LR clocks CD_LRCK & BS_LRCK. Max value is 31.
LR[15:12]	Reserved : to be set to 0

6.7.6 I\_AUDIO\_CONFIG\_5:

b7	b6	b5	b4	b3	b2	b1	b0
MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0

Address : 0x5F (95)

Type : RW - DEC

Software Reset : 0

Description :

See I\_AUDIO\_CONFIG\_8 register description.

6.7.7 I\_AUDIO\_CONFIG\_6 :

b7	b6	b5	b4	b3	b2	b1	b0
MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8

Address : 0x60 (96)

Type : RW - DEC

Software Reset : 0

Description :

See I\_AUDIO\_CONFIG\_8 register description..

6.7.8 I\_AUDIO\_CONFIG\_7 :

b7	b6	b5	b4	b3	b2	b1	b0
MA23	MA22	MA21	MA20	MA19	MA18	MA17	MA16

Address : 0x61 (97)

Type : RW - DEC

Software Reset : 0

Description :

See I\_AUDIO\_CONFIG\_8 register description..

**6.7.9 I\_AUDIO\_CONFIG\_8 :**

b7	b6	b5	b4	b3	b2	b1	b0
MA31	MA30	MA29	MA28	MA27	MA26	MA25	MA24

Address : 0x62 (98)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, those registers are used to configure the MASK to be applied to CD\_LRCK & BS\_LRCK phase 1 & 2.

- if MA<sub>i</sub> set to 0, then bit i of both phases is not received.
- if MA<sub>i</sub> set to 1, then bit i of both phases is received.

**6.7.10 I\_AUDIO\_CONFIG\_9 :**

b7	b6	b5	b4	b3	b2	b1	b0
DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0

Address : 0x63 (99)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, this register is used to configure the size of the data to be received by CD & BS input interfaces in audio mode. Max is 32.

**6.7.11 I\_AUDIO\_CONFIG\_10 :**

b7	b6	b5	b4	b3	b2	b1	b0
DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0

Address : 0x64 (100)

Type : RW - DEC

Software Reset : 0

Description :

See I\_AUDIO\_CONFIG\_11 register description.

**6.7.12 II\_AUDIO\_CONFIG\_11 :**

b7	b6	b5	b4	b3	b2	b1	b0
DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8

Address : 0x65 (101)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, those registers are used to create BCK if configured in output (so if CF2=1 & CF5=1): then value of DV[15:0] is the divider factor to be applied to the selected clock (CF11 select either SYSCLK or PCMCLK) to create BCK.

Note : value 0 & 1 correspond to a bypass of the dividers.

**6.8 BSB\_CONFIGURATION registers**

description

**6.8.1 POL\_REQ :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x59 (89)

Type : WO - DEC

Software Reset : 0

Description :

This register manage the polarity of the data REQ signal DREQ of the BS input interface.

If set to 0, data are requested when REQ = 0.

If set to 1, data are requested when REQ = 1.

**6.8.2 INPUT\_CONF :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x5A (90)

Type : RW - DEC

Software Reset : 0

Description :



If set to 1 enable the configurability of the BSB input interfaces in burst mode thanks to following register, else disable this configurability and take embedded default configuration.

Note that this embedded default configuration can be retrieved by user thanks to following setting :

- I\_AUDIO\_CONFIG1 = b00000000;// polarity choice

**6.8.3 I\_AUDIO\_CONFIG\_1 :**

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	CF0

Address : 0x5B (91)

Type : RW - DEC

Software Reset : 0

Description :

If INPUT\_CONF == 1, this register is used to configure BSB bit clock

**Table 22. .**

Bit	Comment
CF0	Polarity of bit clock BS_BCK : 0 : data provided on falling edge & stable on rising edge. 1 : data provided on rising edge & stable on falling edge

**6.9 CD\_CONFIGURATION registers description**

**BASIC\_COMMAND :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x40 (64)

Type : RW - AEC

Software Reset : 0

Description :

Used for giving to dsp basic cd-player commands

**Table 23. .**

Value	Command
1	stop playing music
2	pause
3	fast forward
4	fast rewind
5	track up
6	track down
9	directory down
10	directory up
11	play specified track
12	set a play-list index
13	edit play list
14	play current dir
15	play cd from beginning
112	start playing music
113	start searching bytes/mute navigation
124	ID3 name of song required
125	ID3 name of author required
126	ID3 name of album required
127	name of file required
128	name of directory required

**6.9.1 FAST\_FUNCTIONAL\_VAL :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x41 (65)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the volume of fast function. For the "fast forward function" it is a number between 1 and 20.

For the "fast rewind function" it is a number of second

**6.9.2 REQUIRED\_TRACK :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x42 (66)

Type : RW - ABO

Software Reset : 0

Description :

This specifies the number of track to play.

**6.9.3 REQUIRED\_DIR :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x43 (67)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the number of directory to play.

**6.9.4 PLAY\_MODE :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x44 (68)

Type : RW - ABO

Software Reset : 0

Description :

This register specifies the playing mode

**Table 24. .**

Bit	Mode
[1:0]	end of directory: 0: play next directory 1: replay same directory 2: make pause. other: reserved
[3:2]	end of track: 0: play next track. 1: replay same track. 2: make pause. other: reserved
4	next track choice: 0: linear mode. 1: random mode.
5	playing time for track: 0: until end of track. 1: scanning mode.
6	end of CD: 0: stop. 1: replay same CD..

**6.9.5 TYPE\_CD\_EXT\_REQ:**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x46 (70)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies the type of request sent to the cd module

**Table 25. .**

Value	Signification
10	application is in pause after EOT or EOD
18	request for a sector
20	begin of track reached
30	ready to receive a new command
35	cd sp ready to run
40	cd application stopped.
66	time spent on track available
112	request for root
120	song information available

**6.9.6 MINUTE\_REQ :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x47 (71)

Type : RO - AEC

Software Reset : 0

Description :

This register specifies to the CD module the minute location requested.

**6.9.7 SECOND\_REQ :**

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

Address : 0x48 (72)

Type : RO - AEC

Software Reset : 0