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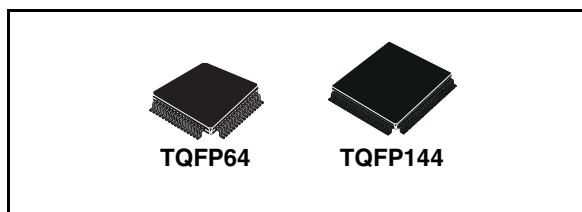


## 32-bit single chip baseband controller for GPS and telematic applications

Data Brief

### Features

- Suitable for automotive applications
  - ARM7TDMI 16/32 bit RISC CPU based host microcontroller.
  - Complete embedded memory system:
    - Flash 256 KB + 16 KB (100K erasing/programming cycles)
    - RAM 64 KB
  - External memory interface provides glueless support for up to four banks of external SRAM, Flash, ROM.
  - 12 channel GPS correlation DSP:
    - no TCXO required
    - RTCA-SC159 / WAAS / EGNOS support
  - GPS performance
    - accuracy: stand alone <30m; differential <1m; surveying <1cm
    - time to first fix: autonomous start 90s; cold start 45s; warm start 7s; obscuration 1s.
  - CMOS M8T (0.18  $\mu$ m) technology.
  - -40°C to 85°C operating temperature range.
  - Packaged in TQFP 64-pin or 144-pin
  - Power supply:
    - 2.7V to 3.6V operating supply range for input/output periphery
    - 3V to 3. V operating supply range for A/ D Converter reference
    - 1.8V operating supply range for core supply provided either by internal voltage regulator with external stabilization capacitor, or by external supply for higher power efficiency.
  - 0-66MHz internal clock frequency managed by a reset and clock control unit; the unitisable to provide low power modes (Wait, Slow, Stop, Standby) and to generate the internal clock from the external reference through integrated PLL.
  - 48 programmable general purpose I/O, each pin programmable independently as digital input or digital output; 40 (30 in TQFP64) are multiplexed with peripheral functions; 16 can generate an interrupt on input level/transition
  - Real time clock module with 3 2 kHz low power oscillator and separate power supply to continue running during stand-by mode.
- 16-bit watchdog timer with 8 bits prescaler for system reliability and integrity.
  - CAN module compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 Mbaud.
  - Four 16-bit programmable timers with 7 bit prescaler, up to two input capture/output compare, one pulse counter function, one PWM channel with selectable frequency each.
  - 4 channels 12-bit sigma-delta analog to digital converter, single channel or multi channel conversion modes, single-shot or continuous conversion modes, sample rate 1KHz (4 KHz when single channel), conversion range 0-2.5V.
  - Three serial communication interfaces (UART) allow full duplex, asynchronous, communications with external devices, independently programmable TX and RX baud rates up to 625K baud.
  - One UART adapted to suit smart card interface needs, for asynchronous SC as defined by ISO 7816-3; it includes SC clock generation..
  - Two serial peripheral interfaces (SPI) allow full duplex, synchronous communications with external devices, master or slave operation, max baud rate: 8Mb/s. One SPI may be used as multimedia card interface.
  - Two I<sup>2</sup>C interfaces provide multi-master and slave functions, support normal and fast I<sup>2</sup>C mode (400 kHz), 7/10 bit addressing modes. One I<sup>2</sup>C interface is multiplexed with one SPI, so either 2xSPI+1xI<sup>2</sup>C or 1xSPI+2xI<sup>2</sup>C may be used at a time.
  - USB unit V1.1 compliant, software configurable end point setting, USB Suspend/Resume support. (TQFP144 only)
  - High Level Data Link Controller (HDLC) unit supports full duplex operating mode, NRZ, NRZI, FM0 and MANCHESTER modes, internal 8bit Baud Rate Generator.



# 1 System block and pin connection diagrams

Figure 1. System block diagram

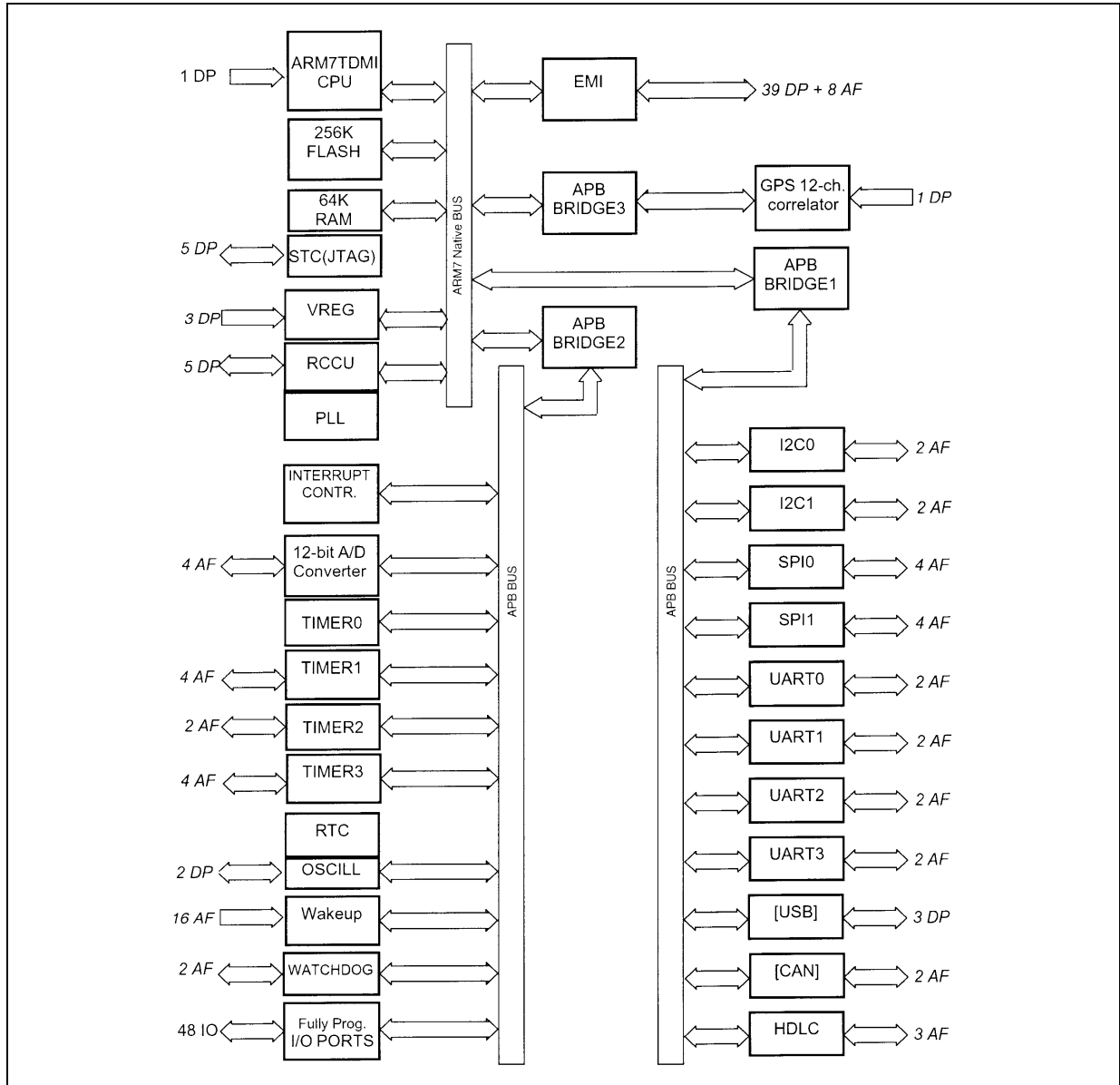




Figure 2. TQFP144 pin connection diagram (top view)

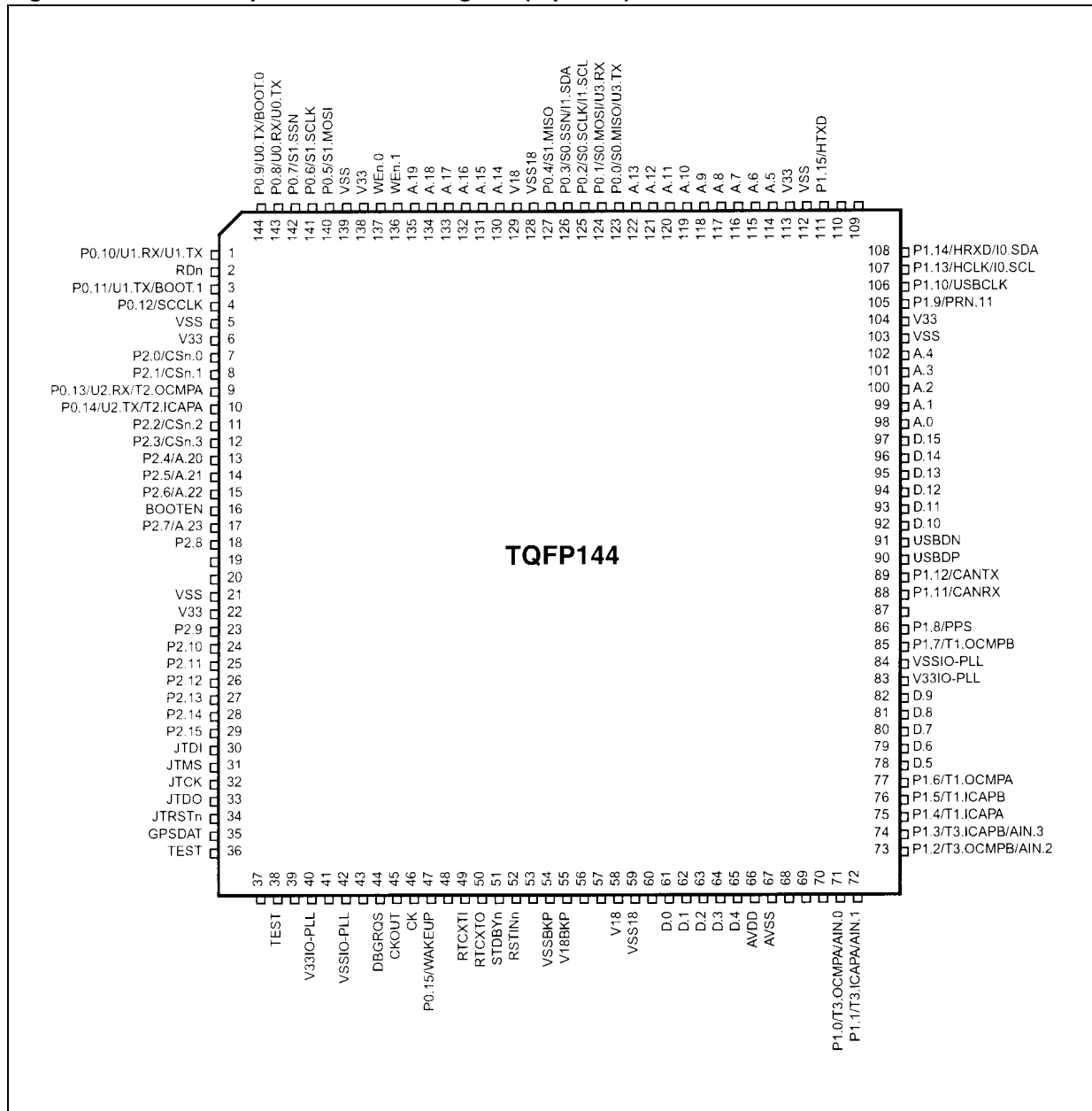
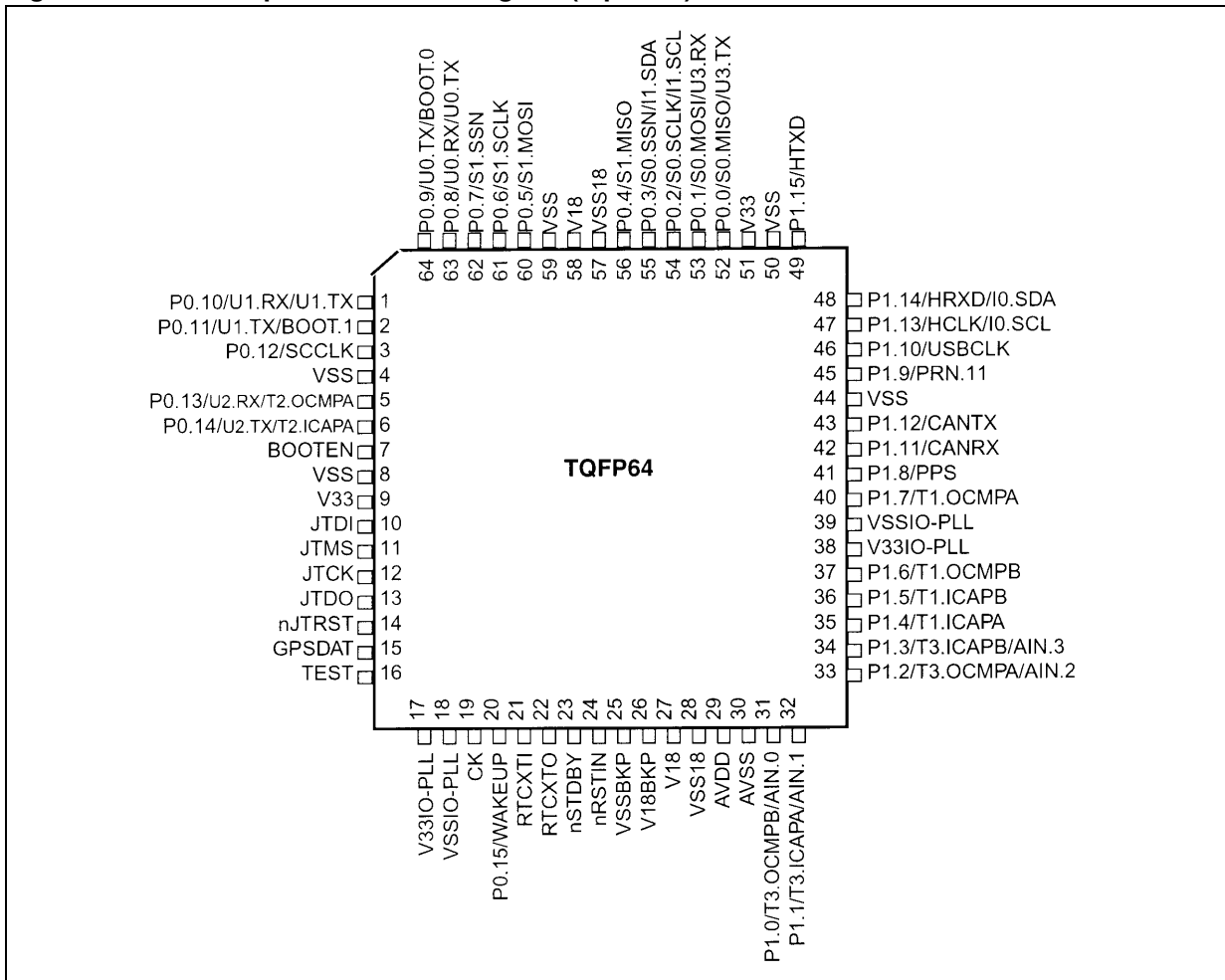


Figure 3. LQFP64 pin connection diagram (top view)



## 2 Ordering information

**Table 1. Device summary**

<b>Order code</b>	<b>Package</b>	<b>Packing</b>
STA2051	TQFP64	Tray
STA2051TR	TQFP64	Tape and reel
STA2051E	TQFP144	Tray
STA2051ETR	TQFP144	Tape and reel
E-STA2051	TQFP64	Tray
E-STA2051TR	TQFP64	Tape and reel

### 3 Revision history

**Table 2. Document revision history**

Date	Revision	Changes
24-Sep-1994	1	Initial release.
25-Jan-2004	2	Added a new feature (first bullet).
05-Dec-2008	3	Reformatted document. Updated <a href="#">Section 2: Ordering information</a> .

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