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Bluetooth™ V2.1 + EDR ("Lisbon") for automotive applications

Features

- Based on Ericsson technology licensing baseband core (EBC)
- Bluetooth™ specification compliance: V2.1 + EDR ("Lisbon")
 - Point-to-point, point-to-multipoint (up to 7 slaves) and scatternet capability
 - Support ACL and SCO links
 - Extended SCO (eSCO) links
 - Faster connection
- HW support for packet types
 - ACL: DM1, DM3, DM5, DH1, DH3, DH5, 2-DH1, 2-DH3, 2-DH5, 3-DH1, 3-DH3, 3-DH5
 - SCO: HV1, HV3 and DV
 - eSCO: EV3, EV4, EV5, 2-EV3, 2-EV5, 3-EV3, 3-EV5
- Adaptive frequency hopping (AFH)
- Channel quality driven data rate (CQDDR)
- "Lisbon" features
 - Encryption pause/resume (EPR)
 - Extended inquiry response (EIR)
 - Link supervision time out (LSTO)
 - Secure simple pairing
 - Sniff subrating
 - Quality of service (QoS)
Packet boundary flag
Erroneous data delivery
- Transmit power
 - Power class 2 and power class 1.5 (above 4 dBm)
 - Programmable output power
 - Power class 1 compatible
- HCI
 - HCI H4 and enhanced H4 transport layer
 - HCI proprietary commands (e.g. peripherals control)
 - Single HCI command for patch/upgrade download
 - eSCO over HCI supported
- Supports pitch-period error concealment (PPEC)
- Efficient and flexible support for WLAN coexistence scenarios

**LFBGA48 (6x6x1.4mm; 0.8mm Pitch)**

- Low power consumption
 - Ultra low power architecture with 3 different low-power levels
 - Deep sleep modes, including host-power saving feature
 - Dual wake-up mechanism: initiated by the host or by the Bluetooth device
- Communication interfaces
 - Fast UART up to 4 MHz
 - Flexible SPI interface up to 13 MHz
 - PCM interface
 - Up to 10 additional flexibly programmable GPIOs
 - External interrupts possible through the GPIOs
 - Fast I²C interface as master
- Clock support
 - System clock input (digital or sine wave) at 9.6, 10, 13, 16, 16.8, 19.2, 26, 33.6 or 38.4 MHz
 - Low power clock input at 3.2 kHz, 32 kHz and 32.768 kHz
- ARM7TDMI CPU
- Memory organization
 - On chip RAM, including provision for patches
 - On chip ROM, preloaded with SW up to HCI
- Ciphering support up to 128-bit key
- Single power supply with internal regulators for core voltage generation
- Supports 1.65 V to 2.85 V I/O systems
- Auto calibration (VCO, filters)

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1 Description

The STA2500D is a single chip Bluetooth solution that is fully optimized for automotive applications such as telematics, navigation and portable navigation. Power consumption levels are targeted at battery powered devices and single chip solution brings cost advantages. Manufacturers can easily and quickly integrate the STA2500D on their product to enable a rapid time to market.

STA2500D supports the Bluetooth specification V2.1 + EDR ("Lisbon") and is optimized in terms of RF performance and cost.

The STA2500D is a ROM-based solution targeted at applications requiring integration up to HCI level. Patch RAM is available, enabling multiple patches/upgrades and fast time to volume. The STA2500D's main interfaces are UART or SPI for HCI transport, PCM for voice and GPIOs for control purposes.

The radio has been designed specifically for single chip requirements, for low power consumption and minimum BOM count.

2 Quick reference data

BT_VIO_x means BT_VIO_A, BT_VIO_B.

BT_HVx means BT_HVA, BT_HVD.

(See also [Table 12.](#))

2.1 Absolute maximum ratings

The absolute maximum rating (AMR) corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown).

Table 1. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
BT_HVx	Core supply voltages	-0.3	4.0	V
BT_VIO_A	Supply voltage I/O	-0.3	4.0	V
BT_VIO_B	Supply voltage I/O (for the low power clock)	-0.3	4.0	V
BT_V _{in}	Input voltage of any digital pin	-0.3	4.0	V
V _{ssdiff}	Maximum voltage difference between different types of V _{ss} pins.	-0.3	0.3	V
T _{stg}	Storage temperature	- 65	+ 150	°C

2.2 Operating ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied.

Table 2. Operating ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
BT_T _{amb}	Operating ambient temperature	-40	25	+85	°C
BT_HVx	Core supply voltages	2.65	2.75	2.85	V
BT_VIO_A	I/O supply voltage	1.65	-	2.85	V
BT_VIO_B	I/O supply voltage (for the low power clock)	1.17	-	2.85	V

2.3 I/O specifications

The I/Os comply with the EIA/JEDEC standard JESD8-B.

Table 3. DC input specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL_BT}	Low level input voltage	-0.2	-	0.35 * BT_VIO_x	V
V_{IH_BT}	High level input voltage	0.65 * BT_VIO_x	-	(BT_VIO_x + 0.2) and (≤ 2.85)	V
C_{in_BT}	Input capacitance ⁽¹⁾	1	-	2.5	pF
R_{pu}	Pull-up equivalent resistance (with $V_{in} = 0$ V)	31	47	73	k Ω
R_{pd}	Pull-down equiv. resistance (with $V_{in} = BT_VIO_x$)	29	50	100	k Ω
V_{hyst}	Schmitt trigger hysteresis (at BT_VIO_A = 1.8 V) except for BT_CONFIG1-3, BT_RESETN, BT_WAKEUP	0.4	0.5	0.6	V
V_{hyst}	Schmitt trigger hysteresis (at BT_VIO_x = 1.8 V) for BT_CONFIG1-3, BT_RESETN, BT_WAKEUP, BT_LP_CLK	0.223	-	0.314	V
V_{hyst}	Schmitt trigger hysteresis (at BT_VIO_B = 1.3 V)	0.2	-	0.3	V

1. Except for the system clock.

Table 4. DC output specification

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OL_BT}	Low level output voltage	$I_d = X^{(1)}$ mA	-	-	0.15	V
V_{OH_BT}	High level output voltage	$I_d = X^{(1)}$ mA	BT_VIO_x - 0.25	-	-	V

1. X is the source/sink current under worst-case conditions according to the drive capabilities (see [Section 3](#))

2.4 Clock specifications

The STA2500D supports, on the BT_REF_CLK_IN pin, the system clock both as a sine wave clock and as a digital clock. For configuration, see [Table 12](#): pin BT_VDD_CLD (E6).

Table 5. System clock supported frequencies

Symbol	Parameter	Values	Unit
F_{IN}	Clock input frequency list	9.6, 10, 13, 16, 16.8, 19.2, 26, 33.6, 38.4	MHz

Table 6. System clock overall specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{INTOL}	Tolerance on input frequency	-20	-	20	ppm

Table 7. System clock, sine wave specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{PP}	Peak to peak voltage range	0.27	0.5	1.8	V
N _H	Total harmonic content of input signal	-	-	-25	dBc
Z _{INRe}	Real part of parallel input impedance at pin	30	60	90	kΩ
Z _{INIm}	Imaginary part of parallel input impedance at pin	-	5	8	pF
Z _{IDRe}	Real impedance discrepancy between active and non-active mode of clock input	-	-	7	kΩ
Z _{IDIm}	Imaginary impedance discrepancy between active and non-active mode of clock input	-	-	500	fF
	Phase noise @ 10 kHz ⁽¹⁾	-	-	-126	dBc/Hz

1. Equivalent to max 10 ps time jitter (rms).

Table 8. System clock, digital clock DC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{IL}	Low level input voltage	-0.2	-	0.35 * BT_VDD_CLD	V
V _{IH}	High level input voltage	0.65 * BT_VDD_CLD	-	(BT_VDD_CLD + 0.2) and (≤ 2.85)	V
C _{IN}	Input capacitance	-	5	8	pF

Table 9. System clock, digital clock AC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
T _{RISE}	10% - 90% rise time	-	1.5	6	ns
T _{FALL}	90% - 10% fall time	-	1.5	6	ns
D _{CYCLE}	Duty cycle	45	50	55	%
-	Phase noise @ 10 kHz ⁽¹⁾	-	-	-121	dBc/Hz

1. Equivalent to max 15 ps time jitter (rms).

Table 10. Low power clock specifications

The low power clock pin is powered by connecting BT_VIO_B to the wanted supply.

Symbol	Parameter	Min.	Typ.	Max.	Unit
F _{IN}	Clock input frequencies	3.2, 32, 32.768			kHz
-	Duty cycle	30	-	70	%
-	Tolerance on input frequency	-250	-	250	ppm
V _{IL}	Low level input voltage	-	-	0.35 * BT_VIO_B	V
V _{IH}	High level input voltage	0.65 * BT_VIO_B	-	-	V
V _{hyst}	Schmitt trigger hysteresis (BT_VIO_B = 1.8 V)	0.4	0.5	0.6	V

Table 10. Low power clock specifications (continued)

The low power clock pin is powered by connecting BT_VIO_B to the wanted supply.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{hyst}	Schmitt trigger hysteresis (BT_VIO_B = 1.3 V)	0.2	0.3	0.4	V
C_{IN}	Input capacitance	1	-	2.5	pF
T_{RISE}	10% - 90% rise time ⁽¹⁾	-	-	1	μ s
T_{FALL}	90% - 10% fall time ⁽¹⁾	-	-	1	μ s
-	Total jitter ⁽²⁾	-	-	250	ppm

- The rise and fall time are not the most important parameters for the low power clock input due to the Schmitt trigger logic. It is more important that the noise on the Low power clock line remains substantially below the hysteresis in amplitude.
- The total jitter is defined as the error that can appear on the actual frequency between two clock edges compared to the perfect frequency. Due to this, the total jitter value must contain the jitter itself and the error due to the accuracy on the clock frequency. The lower the accuracy, the smaller the jitter is allowed to be.

2.5 Current consumption

$T_{amb} = 25^{\circ}\text{C}$, 13 MHz digital clock, 7 dBm output power for BR packets, 3 dBm output power for EDR packets.

Table 11. Current consumption⁽¹⁾

State	Typ.	Unit
Complete Power Down	1	μ A
Deep Sleep mode	20	μ A
Functional Sleep mode ⁽²⁾	1.2	mA
Sniff mode (1.28 s, 2 attempts, 0 timeouts), combined with H4 UART Deep Sleep mode (see section 6.10.3)	55	μ A
Master mode	83	μ A
Slave mode		
Inquiry scan (1.28 seconds period), combined with H4 UART Deep Sleep mode (see section 6.10.3)	318	μ A
HW Page scan (1.28 seconds period), combined with H4 UART Deep Sleep mode (see section 6.10.3)	312	μ A
HW Inquiry and Page scan (1.28 seconds period), combined with H4 UART Deep Sleep mode (see section 6.10.3)	591	μ A
Idle ACL connection (Master)	3.6	mA
Idle ACL connection (Slave)	8.2	mA
Active: audio (HV3) Master (not sniffed)	11.7	mA
Active: audio (HV3) Slave (Sniff 1.28 s, 2 attempts, 0 timeouts)	10.6	mA
Active: data (DH1) Master or Slave (172.8 kbps asymmetrical in TX mode) (172.8 kbps symmetrical)	23 28.5	mA

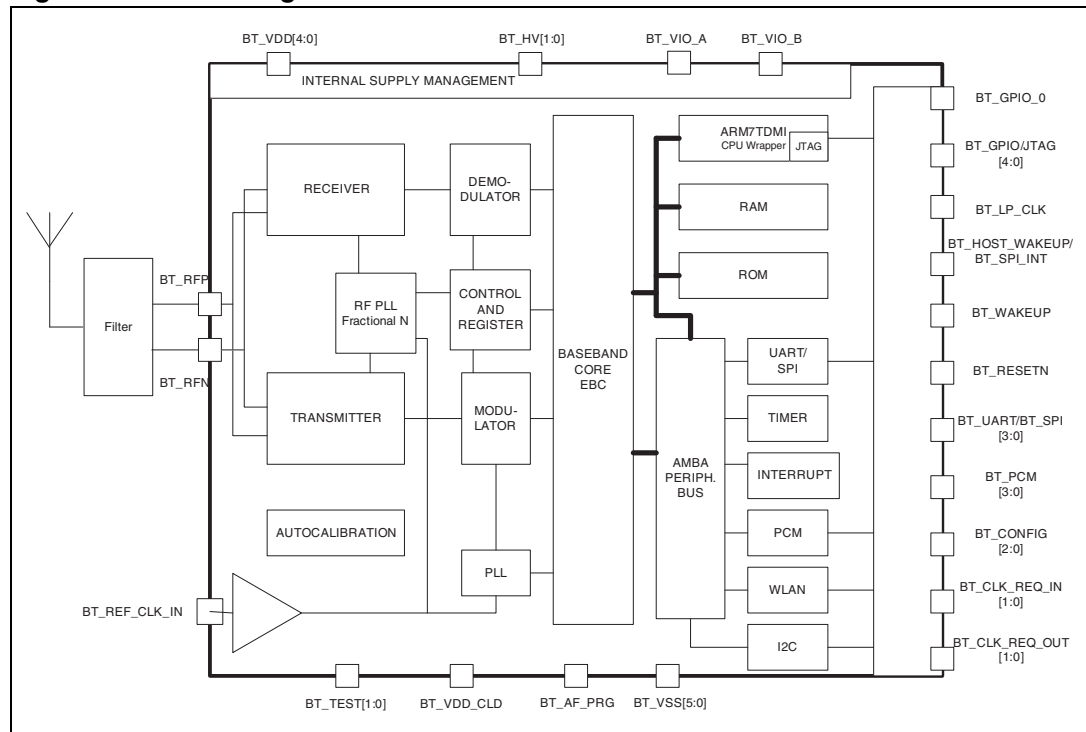
Table 11. Current consumption⁽¹⁾ (continued)

State	Typ.	Unit
Active: data (DH5) Master or Slave (723.2 kbps asymmetrical in TX mode) (433.9 kbps symmetrical)	35.4	mA
	35.4	mA
Active: data (2-DH5) Master or Slave (869.7 kbps symmetrical)	35.4	mA
Active: data (3-DH5) Master or Slave (1306.9 kbps symmetrical)	35.4	mA
Active: audio eSCO (EV3), (64 kbps symmetrical $T_{eSCO} = 6$) Master mode Slave mode	12	mA
	15	mA
Active: audio eSCO (2-EV3), (64 kbps symmetrical $T_{eSCO} = 12$) Master mode Slave mode	7.8	mA
	11.7	mA
Active: audio eSCO (3-EV3), (64 kbps symmetrical $T_{eSCO} = 18$) Master mode Slave mode	6.5	mA
	10.5	mA
Active: audio eSCO (EV5), (64 kbps symmetrical $T_{eSCO} = 36$), Master mode	8	mA
Active: audio eSCO (EV5), (64 kbps symmetrical $T_{eSCO} = 36$), Slave mode	11.9	mA
Active: audio eSCO (2-EV5), (64 kbps symmetrical $T_{eSCO} = 36$), Master mode	6.3	mA
Active: audio eSCO (3-EV5), (64 kbps symmetrical $T_{eSCO} = 36$), Master mode	5.75	mA

1. The power consumption (except for power safe modes i.e. complete power down and deep sleep mode) will rise (with approx. 200 μ A) if an analog system clock is used instead of a digital clock.
2. In functional sleep mode, the baseband clock is still running.

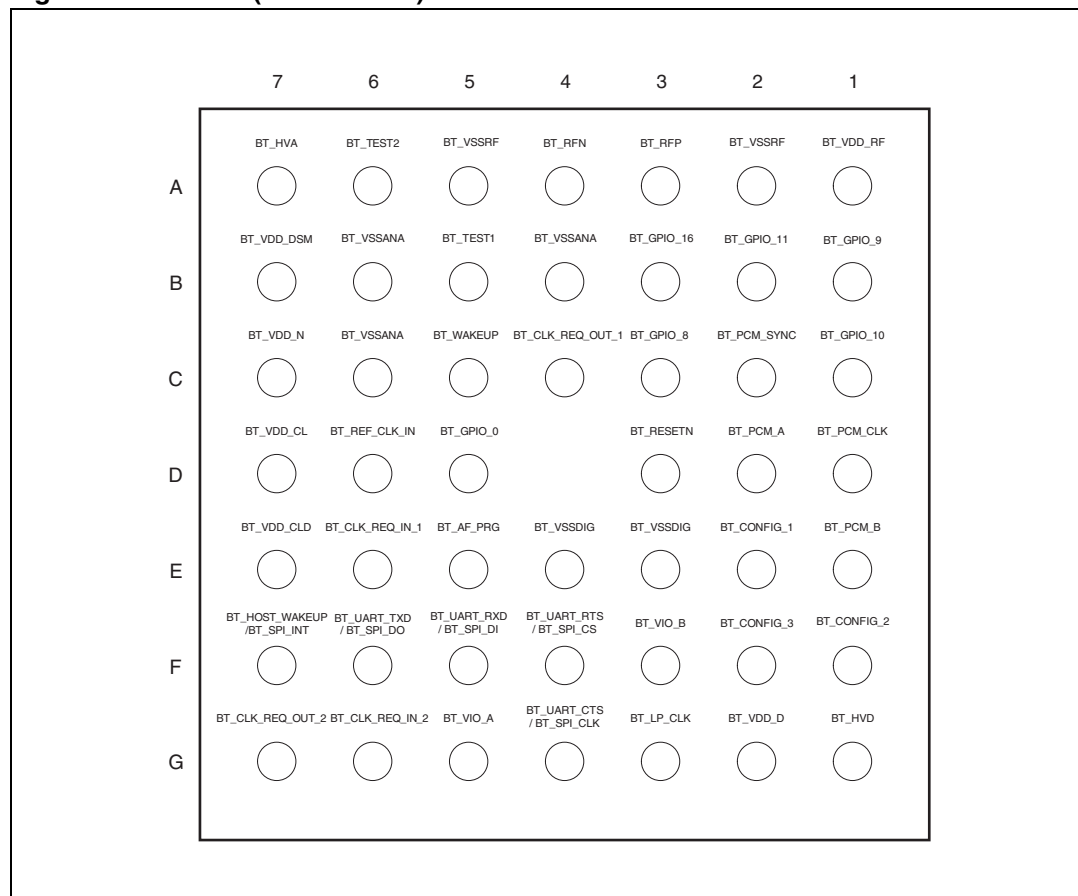
3 Block diagram and electrical schematic

Figure 1. Block diagram and electrical schematic



4 Pinout

Figure 2. Pinout (bottom view)



4.1 Pin description and assignment

Table 12 shows the pin list of the STA2500D.

In columns “Reset” and “Default after reset”, the “PD/PU” shows the pads implementing an internal pull-down/up.

The column “Reset” shows the state of the pins during hardware reset; the column “Default after reset” shows the state of the pins after the hardware reset state is left, but before any software parameter download.

The column “Type” describes the pin directions:

- I for Input (All inputs have a Schmitt trigger function.)
- O for Output
- I/O for Input/Output
- O/t for tri-state output

For the output pin the default drive capability is 2 mA, except for pin K3 (BT_GPIO_11) and pin L3 (BT_GPIO_8) where it is 8 mA such that when used for Class 1, these 2 pins can be used for a switch control in a cheaper way.

Table 12. The STA2500D pin list (functional and supply)

Name	Pin #	Description	Type	Reset ⁽¹⁾	Default ⁽²⁾ after reset
Clock and reset pins					
BT_RESETN	D3	Global reset - active low	-	-	
BT_REF_CLK_IN	D6	Reference clock input ⁽³⁾	I	Input	Input
BT_LP_CLK	G3	Low power clock input	-	-	
SW initiated low power mode					
BT_CLK_REQ_OUT_1	C4	Wake-up signal to Host (Active high or Active low, depending on configuration pins)	I/O ⁽⁴⁾	Input PD/PU, depends on config	Output depends on config
BT_CLK_REQ_OUT_2	G7	Wake-up signal to Host. Active low (SPI mode only)		Input PU	I/O depends on config
BT_CLK_REQ_IN_1	E6	Clock request input (Active high)		Input PD	Input PD
BT_CLK_REQ_IN_2	G6	Clock request input (Active low)		Input PU	Input PU
BT_HOST_WAKEUP/ BT_SPI_INT	F7	Wake-up signal to Host or SPI interrupt		Input PD	Output
BT_WAKEUP	C5	Wake-up signal to Bluetooth (Active high)	I/O	Input ⁽⁵⁾	Input
UART interface					
BT_UART_RXD/ BT_SPI_DI	F5	UART receive data	I/O ⁽⁴⁾	Input PD	Input PD
		SPI data in			Input PD
BT_UART_TXD/ BT_SPI_DO	F6	UART transmit data			Output high
		SPI data out			Input PD
BT_UART_CTS/ BT_SPI_CLK	G4	UART clear to send		Input PU	Input PU
		SPI clock			Input PD
BT_UART_RTS/ BT_SPI_CSN	F4	UART request to send			Output low
		SPI chip select			Input PU
PCM interface					
BT_PCM_SYNC	C2	PCM frame signal	I/O ⁽⁴⁾	Input PD	Input PD
BT_PCM_CLK	D1	PCM clock signal			
BT_PCM_A	D2	PCM data			
BT_PCM_B	E1	PCM data			
JTAG interface					
BT_GPIO_9	B1	JTAG_TDI or GPIO	-	Input PU ⁽⁶⁾	Input PU ⁽⁶⁾

Table 12. The STA2500D pin list (functional and supply) (continued)

Name	Pin #	Description	Type	Reset ⁽¹⁾	Default ⁽²⁾ after reset
BT_GPIO_11	B2	JTAG_TDO or GPIO	-	Input PD ⁽⁶⁾	Input PD ⁽⁶⁾
BT_GPIO_10	C1	JTAG_TMS or GPIO	I/O ⁽⁴⁾	Input PD ⁽⁶⁾	Input PD ⁽⁶⁾
BT_GPIO_16	B3	JTAG_NTRST (Active low) or Alternate function.	-	Input PD ⁽⁶⁾	Input PD ⁽⁶⁾
BT_GPIO_8	C3	JTAG_TCK or GPIO	-	Input PD ⁽⁶⁾	Input PD ⁽⁶⁾
General purpose input/output pins					
BT_GPIO_0	D5	General purpose I/O	I/O ⁽⁴⁾	Input PD	Input PD
Configuration pins					
BT_CONFIG_1	E2		-	-	-
BT_CONFIG_2	F1	Configuration signal	I	Input	Input
BT_CONFIG_3	F2		-	-	-
RF signals					
BT_RFP	A3	Differential RF port	I/O	-	-
BT_RFN	A4			-	-
Power supply					
BT_HVA	A7	Power supply (Connect to 2.75 V)	-	-	-
BT_HVD	G1				
BT_VIO_A	G5	1.65 V to 2.85 V I/Os supply ⁽⁷⁾	-	-	-
BT_VIO_B	F3	1.17 V to 2.85 V I/Os supply ⁽⁷⁾	-	-	-
BT_VDD_CLD	E7	System clock supply 1.65 V to 2.85 V (Connect to BT_VIO_A in case of a digital reference clock input, to BT_VSSANA in case of an analog reference clock input.)	-	-	-
BT_VSSDIG	E3	Digital ground	-	-	-
	E4				
BT_VSSANA	B4	Analog ground	-	-	-
	B6				
	C6				
BT_VSSRF	A2	RF ground	-	-	-
	A5				
BT_VDD_CL	D7	Internal supply decoupling/Regulator output. Need 220nF decoupling capacitor to BT_VSSANA.	-	-	-

Table 12. The STA2500D pin list (functional and supply) (continued)

Name	Pin #	Description	Type	Reset ⁽¹⁾	Default ⁽²⁾ after reset
BT_VDD_D	G2	Internal supply decoupling/Regulator output. Need 220nF decoupling capacitor to BT_VSSDIG.	-	-	-
BT_VDD_DSM	B7	Internal supply decoupling/Regulator output. Need 220nF decoupling capacitor to BT_VSSANA.	-	-	-
BT_VDD_N	C7	Internal supply decoupling/Regulator output. Need 220nF decoupling capacitor to BT_VSSANA.	-	-	-
BT_VDD_RF	A1	Internal supply decoupling/Regulator output. Need 220nF decoupling capacitor to BT_VSSRF.	-	-	-
Other pins					
BT_TEST1	B5	Test pin	I/O	Input ⁽⁸⁾	Input ⁽⁸⁾
BT_TEST2	A6				
BT_AF_PRG	E5	Test pin (Leave unconnected) ⁽⁹⁾	I/O	Open	Open

1. Pin behaviour during HW reset (BT_RESETN low).
2. Pin behaviour immediately after HW reset and internal chip initialization, but before SW parameter download.
3. See also pin BT_VDD_CLD in [Table 12](#).
4. Reconfigurable I/O pin. The functionality of these I/Os can be configured through software parameter download (see [Section 7.5](#)).
5. Should be strapped to BT_VSSDIG if not used.
6. JTAG mode.
7. Described in [Section 4.3](#).
8. To be strapped to BT_VSSANA.
9. Pin is ST - reserved for test function and it must be soldered to an isolated pad (not connected to anything, just floating).

4.2 HW configuration of the STA2500D

By means of the three configuration pins, one can select the Host interface (UART or SPI) and clock request signal polarity to be used at startup.

The available combinations of Host interface and protocol are illustrated in [Table 13](#) (where '1' = BT_VIO_A and '0' = BT_VSSDIG). Additionally, the polarity of the BT_CLK_REQ signals can be programmed through the same pins. The polarity of the BT_CLK_REQ_IN and BT_CLK_REQ_OUT signals is further described in [Section 6.8](#).

Table 13. Configuration programming

BT_CONFIG_1	BT_CONFIG_2	BT_CONFIG_3	Communication Protocol	BT_CLK_REQ_OUT_1	BT_CLK_REQ_OUT_2
0	1	0	H4 UART	Active high	Depending on SW config
0	1	1	H4 UART	Active low	Depending on SW config
1	1	0	Reserved	Reserved	Reserved
1	1	1	Reserved	Reserved	Reserved
1	0	0	Reserved	Reserved	Reserved
1	0	1	Enhanced H4 SPI ⁽¹⁾	Active high	Active low
0	0	1	Reserved	Reserved	Reserved
0	0	0	Reserved	Reserved	Reserved

1. In order to get other SPI modes, the Host must send a specific configuration at start-up in addition of these configuration pins.

4.3 I/O Supply

The device STA2500D has two different I/O supplies: BT_VIO_A and BT_VIO_B.

The two different pins may be potentially connected to separate dedicated voltage supplies in order to harmonize the digital levels to the platform.

They are linked to different interfaces as described in [Table 14](#).

Table 14. I/O supply split diagram

I/O supply name	Voltage range [V]	Function	Associated pins
BT_VIO_A	1.65 - 2.85	Configuration	BT_CONFIG_1, BT_CONFIG_2, BT_CONFIG_3
		Control	BT_WAKEUP
			BT_RESETN
			BT_CLK_REQ_OUT_1, BT_CLK_REQ_OUT_2
		GPIO (JTAG)	BT_GPIO_8 (JTAG_TCK), BT_GPIO_9 (JTAG_TDI), BT_GPIO_10 (JTAG_TMS), BT_GPIO_11 (JTAG_TDO), BT_GPIO_16 (JTAG_NTRST)
		PCM	BT_PCM_A, BT_PCM_B, BT_PCM_SYNC, BT_PCM_CLK
		Control	BT_REG_CTRL
		UART (SPI)	BT_UART_RXD (SPI_DI), BT_UART_TXD (SPI_DO), BT_UART_RTS (SPI_CSN), BT_UART_CTS (SPI_CLK), BT_HOST_WAKEUP (SPI_INT)
		Control (GPIO)	BT_CLK_REQ_IN_1 (GPIO_1), BT_CLK_REQ_IN_2 (GPIO_2)
GPIO	BT_GPIO_0		
BT_VIO_B	1.17 - 2.85	Low - power clock	BT_LP_CLK

5 Functional description

5.1 Transmitter

The transmitter uses the serial transmit data from the Bluetooth Controller. The transmitter modulator converts this data into GFSK, $\pi/4$ -DQPSK or 8-DPSK modulated I and Q digital signals for respectively 1, 2 and 3 Mbps transmission speed. These signals are then converted to analog signals that are low pass filtered before up-conversion. The carrier frequency drift is limited by a closed loop PLL.

5.2 Receiver

The STA2500D implements a low-IF receiver for Bluetooth modulated input signals. The radio signal is taken from a balanced RF input and amplified by an LNA. The mixers are driven by two quadrature LO signals, which are locally generated from a VCO signal running at twice the frequency. The I and Q mixer output signals are band pass filtered by a poly-phase filter for channel filtering and image rejection. The output of the band pass filter is amplified by a VGA to the optimal input range for the A/D converter. Further channel filtering is done in the digital part. The digital part demodulates the GFSK, $\pi/4$ -DQPSK or 8-DPSK coded bit stream by evaluating the phase information. RSSI data is extracted. Overall automatic gain amplification in the receive path is controlled digitally. The RC time constants for the analog filters are automatically calibrated on chip.

5.3 PLL

The on chip VCO is part of a PLL. The tank resonator circuitry for the VCO is completely integrated without need of external components. Variations in the VCO centre frequency are calibrated out automatically.

5.4 Bluetooth controller V1.2 and V2.0 + EDR features

The Bluetooth controller is backward compatible with the Bluetooth specification V1.2 [] and V2.0 + EDR []. Here below is a list with the main features of those specifications:

- Adaptive Frequency Hopping (AFH): hopping kernel, channel assessment as Master and as Slave
- Fast Connection: Interlaced scan for Page and Inquiry scan, answer FHS at first reception, RSSI used to limit range
- Extended SCO (eSCO) links: supports EV3, EV4 and EV5 packets
- Channel Quality Driven Data Rate change (CQDDR)
- QoS Flush
- Synchronization: BT clocks are available at HCI level for synchronization of parallel applications on different Slaves
- L2CAP Flow & Error control
- LMP SCO handling
- 2 Mbps packet types
 - ACL: 2-DH1, 2-DH3, 2-DH5
 - eSCO: 2-EV3, 2-EV5
- 3 Mbps packet types
 - ACL: 3-DH1, 3-DH3, 3-DH5
 - eSCO: 3-EV3, 3-EV5

5.5 Bluetooth controller V2.1 + EDR (“Lisbon”)

- Encryption Pause/Resume (EPR)
- Extended Inquiry Response (EIR)
- Link Supervision Time Out (LSTO)
- Secure Simple Pairing
- Sniff Subrating
- Quality of Service (Qos)
 - Packet Boundary Flag
 - Erroneous Data Delivery

5.6 Processor and memory

- ARM7TDMI
- On chip RAM, including provision for patches
- On chip ROM, preloaded with SW up to HCI

5.7 TX output power control

The STA2500D supports output power control with advanced features:

- Basic feature:
 - With the standard TX power control algorithm enabled, the STA2500D will adapt its output power when a remote BT device supports the RSSI feature; this allows the remote device to measure the link strength and to request the STA2500D to decrease/increase its output power. In case the remote device does not support the RSSI feature, the STA2500D will use its 'default' output power level.
- Advanced features, available via specific HCI commands:
 - Enhanced power control feature: allows the STA2500D to decrease autonomously its output power until the remote BT device, supporting the RSSI feature, requests to increase the output power.

6 General specification

All the values are provided according to the Bluetooth specification V2.1 + EDR ("Lisbon") unless otherwise specified. The below values are preliminary and will be updated in the next version of this datasheet.

6.1 Receiver

All specifications below are given at device pin level and with the conditions as specified. Parameters are given for each of the 3 modulation types supported.

Typical is defined at $T_{amb} = 25\text{ }^{\circ}\text{C}$, $BT_HV = 2.75\text{ V}$. Minimum and Maximum are worst cases over corner lots and temperature. Parameters are given at device pin, except for receiver interferers measured at antenna with a filter having a typical attenuation of 2.3 dB.

Table 15. Mbps receiver parameters - GFSK

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RFin	Input frequency range	-	2402	-	2480	MHz
RXsensC	Receiver sensitivity (Clean transmitter)	@ BER 0.1%	-	-88	-86	dBm
RXsensD	Receiver sensitivity (Dirty transmitter)	@ BER 0.1%	-	-87	-84	dBm
RXmax	Maximum useable input signal level	@ BER 0.1%	-	10	15	dBm
Receiver blocking performance @ BER 0.1% on Channel 58 (without Filter)						
-	signal in GSM band 900 MHz (824 MHz to 960 MHz)	@ Input signal strength = -67 dBm	-	-15	-	dBm
-	signal in GSM band 1800 MHz (1805 MHz to 1990 MHz)	@ Input signal strength = -67 dBm	-	-2.5	-	dBm
-	signal in WCDMA band (2010 MHz to 2170 MHz)	@ Input signal strength = -67 dBm	-	-1.5	-	dBm
Receiver interferer performance @ BER 0.1%						
$C/I_{co-channel}$	Co-channel interference	@ Input signal strength = -60 dBm	-	9.5	11	dB
C/I_{1MHz}	Adjacent (± 1 MHz) interference	@ Input signal strength = -60 dBm	-	-9	0	dB
C/I_{+2MHz}	Adjacent (+2 MHz) interference	@ Input signal strength = -60 dBm	-	-40	-30	dB
C/I_{-2MHz}	Adjacent (-2 MHz) interference	@ Input signal strength = -67 dBm	-	-26	-9	dB
C/I_{+3MHz}	Adjacent (+3 MHz) interference	@ Input signal strength = -67 dBm	-	-46.5	-40	dB

Table 15. Mbps receiver parameters - GFSK (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C/I _{-3MHz}	Adjacent (-3 MHz) interference	@ Input signal strength = -67 dBm	-	-43	-20	dB
C/I _{≥4MHz}	Adjacent (≥ ±4 MHz) interference	@ Input signal strength = -67 dBm	-	-48	-40	dB
Receiver inter-modulation						
IMD	Inter-modulation	Measured as defined in BT test specification [].	-39	-32	=	dBm

Typical is defined at $T_{amb} = 25\text{ }^{\circ}\text{C}$, $BT_HV = 2.75\text{ V}$. Minimum and Maximum are worst cases over corner lots and temperature. Parameters are given at device pin, except for receiver interferers measured at antenna with a filter having a typical attenuation of 2.3 dB.

Table 16. Mbps receiver parameters - $\pi/4$ -DQPSK

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RFin	Input frequency range	=	2402		2480	MHz
RXsensC	Receiver sensitivity (Clean transmitter)	@ BER 0.01%	-	-87	-85	dBm
RXsensD	Receiver sensitivity (Dirty transmitter)	@ BER 0.01%	-	-86.5	-84.5	dBm
RXmax	Maximum useable input signal level	@ BER 0.1%	-15	-9	-	dBm
Receiver blocking performance @ BER 0.1% on channel 58 (without Filter)						
-	signal in GSM band 900 MHz (824 MHz to 960 MHz)	@ Input signal strength = -67 dBm	-	-15.5	-	dBm
-	signal in GSM band 1800 MHz (1805 MHz to 1990 MHz)	@ Input signal strength = -67 dBm	-	-3.5	-	dBm
-	signal in WCDMA band (2010 MHz to 2170 MHz)	@ Input signal strength = -67 dBm	-	-2.5	-	dBm
Receiver interferer performance @ BER 0.1%						
C/I _{co-channel}	Co-channel interference	@ Input signal strength = -60 dBm	-	11	13	dB
C/I _{1MHz}	Adjacent (±1 MHz) interference	@ Input signal strength = -60 dBm	-	-11.5	0	dB
C/I _{+2MHz}	Adjacent (+2 MHz) interference	@ Input signal strength = -60 dBm	-	-40	-30	dB
C/I _{-2MHz}	Adjacent (-2 MHz) interference	@ Input signal strength = -67 dBm	-	-20	-7	dB
C/I _{+3MHz}	Adjacent (+3 MHz) interference	@ Input signal strength = -67 dBm	-	-48.5	-40	dB

Table 16. Mbps receiver parameters - $\pi/4$ -DQPSK (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C/I _{-3MHz}	Adjacent (-3 MHz) interference	@ Input signal strength = -67 dBm	-	-47	-20	dB
C/I _{≥4MHz}	Adjacent ($\geq \pm 4$ MHz) interference	@ Input signal strength = -67 dBm	-	-48	-40	dB

Typical is defined at $T_{amb} = 25$ °C, $BT_{HV} = 2.75$ V. Minimum and Maximum are worst cases over corner lots and temperature. Parameters are given at device pin, except for receiver interferers measured at antenna with a filter having a typical attenuation of 2.3 dB.

Table 17. Mbps receiver parameters - 8-DPSK

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RFin	Input frequency range	-	2402	-	2480	MHz
RXsensC	Receiver sensitivity (Clean transmitter)	@ BER 0.01%	-	-79.5	-77.5	dBm
RXsensD	Receiver sensitivity (Dirty transmitter)	@ BER 0.01%	-	-77	-74.5	dBm
RXmax	Maximum useable input signal level	@ BER 0.1%	-20	-15	-	dBm
Receiver blocking performance @ BER 0.1% on channel 58 (without Filter)						
-	Signal in GSM band 900 MHz (824 MHz to 960 MHz)	@ Input signal strength = -67 dBm	-	-20	-	dBm
-	Signal in GSM band 1800 MHz (1805 MHz to 1990 MHz)	@ Input signal strength = -67 dBm	-	-14.5	-	dBm
-	Signal in WCDMA band (2010 MHz to 2170 MHz)	@ Input signal strength = -67 dBm	-	-14	-	dBm
Receiver interferer performance @ BER 0.1%						
C/I _{co-channel}	Co-channel interference	@ Input signal strength = -60 dBm	-	19	21	dB
C/I _{1MHz}	Adjacent (± 1 MHz) interference	@ Input signal strength = -60 dBm	-	-4	5	dB
C/I _{+2MHz}	Adjacent (+2 MHz) interference	@ Input signal strength = -60 dBm	-	-37	-25	dB
C/I _{-2MHz}	Adjacent (-2 MHz) interference	@ Input signal strength = -67 dBm	-	-12	0	dB
C/I _{+3MHz}	Adjacent (+3 MHz) interference	@ Input signal strength = -67 dBm	-	-46	-33	dB
C/I _{-3MHz}	Adjacent (-3 MHz) interference	@ Input signal strength = -67 dBm	-	-40	-13	dB
C/I _{≥4MHz}	Adjacent ($\geq \pm 4$ MHz) interference	@ Input signal strength = -67 dBm	-	-43	-33	dB

6.2 Transmitter

Unless otherwise stated, typical is defined at $T_{amb} = 25\text{ °C}$, $BT_HV = 2.75\text{ V}$. Minimum and Maximum are worst cases over corner lots and temperature. Parameters are given at device pin, except for in-band spurious measured at antenna.

Table 18. Transmitter parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RFout	Output frequency range	-	2402	-	2480	MHz
RF Transmit Power						
TXpout (GFSK)	Maximum output power ⁽¹⁾	@ 2402 - 2480 MHz @ 25 °C	6	8	10	dBm
TXpout (GFSK)	Maximum output power ⁽¹⁾	@ 2402 - 2480 MHz @ worst cases over corner lots and temperature	4.5	8	10.5	dBm
TXpout (GFSK)	Minimum output power	@ 2402 - 2480 MHz	-52.5	-47.5	-42.5	dBm
TXpout ($\pi/4$ -DQPSK)	Maximum output power ^{(1) (2)}	@ 2402 - 2480 MHz @ 25 °C	3.5	6	8	dBm
TXpout ($\pi/4$ -DQPSK)	Minimum output power ⁽²⁾	@ 2402 - 2480 MHz	-43.5	-38.5	-33.5	dBm
TXpoutrel ($\pi/4$ -DQPSK)	Relative transmit power ⁽³⁾	@ 2402 - 2480 MHz	-	-0.2	-	dB
TXpout (8-DPSK)	Maximum output power ^{(1) (2)}	@ 2402 - 2480 MHz @ 25 °C	3.5	6	8	dBm
TXpout (8-DPSK)	Minimum output power ⁽²⁾	@ 2402 - 2480 MHz	-43.5	-38.5	-33.5	dBm
TXpoutrel (8-DPSK)	Relative transmit power ⁽³⁾	@ 2402 - 2480 MHz	-	-0.2	-	dB
In-band spurious emission⁽⁴⁾						
FCC	FCC's 20 dB BW	-	900	930	950	kHz
ACP_2	Channel offset = ± 2 MHz	-	-	-43.5	-20	dBm
ACP_3	Channel offset = ± 3 MHz	-	-	-52.5	-40	dBm
ACP_4	Channel offset $\geq \pm 4$ MHz	-	-	-54.5	-40	dBm
EDR_IBS_1	Channel offset = ± 1 MHz (2 and 3 Mbps)	-	-	-33.5	-26	dB
EDR_IBS_2	Channel offset = ± 2 MHz (2 and 3 Mbps)	-	-	-31.5	-20	dBm
EDR_IBS_3	Channel offset = ± 3 MHz (2 and 3 Mbps)	-	-	-45	-40	dBm
EDR_IBS_4	Channel offset = ± 4 MHz (2 and 3 Mbps)	-	-	-50	-40	dBm

Table 18. Transmitter parameters (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Initial carrier frequency tolerance (for an exact reference)⁽⁵⁾						
ΔF	$ f_{TX}-f_0 $	-	-	0	-	kHz
Carrier frequency stability⁽⁶⁾						
$ \Delta f_{sl} $	Carrier frequency stability	-	-	3.2	10	kHz
Carrier frequency drift⁽⁷⁾						
$ \Delta f_{p1} $	One slot packet	-	-	12	25	kHz
$ \Delta f_{p3} $	Three slots packet	-	-	14	40	kHz
$ \Delta f_{p5} $	Five slots packet	-	-	14	40	kHz
Carrier frequency drift rate⁽⁷⁾						
$ \Delta f/50\mu s $	Frequency drift rate	-	-	8/50	20/50	kHz/ μs
Modulation accuracy ⁽⁶⁾ ⁽⁷⁾ ⁽⁸⁾						
Δf_{1avg}	Maximum modulation	-	140	163	175	kHz
Δf_{2max}	Minimum modulation	-	115	135	-	kHz
$\Delta f_{1avg}/\Delta f_{2avg}$		-	0.8	0.9	-	
-	2-DH5 RMS DEVM	-	-	8	20	%
-	2-DH5 99% DEVM	-	-	-	30	%
-	2-DH5 Peak DEVM	-	-	21	35	%
-	3-DH5 RMS DEVM	-	-	8	13	%
-	3-DH5 99% DEVM	-	-	-	20	%
-	3-DH5 Peak DEVM	-	-	21	25	%
TX out of band emission						
E850	Emission in GSM band 850 MHz	BW = 200 kHz ⁽⁷⁾ ⁽⁹⁾ ⁽¹⁰⁾	-	-79	-76	dBm
E900	Emission in GSM band 900 MHz	BW = 200 kHz ⁽⁷⁾ ⁽⁹⁾ ⁽¹⁰⁾	-	-79	-76	dBm
E1500	Emission in GPS band	BW = 200 kHz ⁽⁷⁾ ⁽⁹⁾ ⁽¹⁰⁾	-	-85	-84	dBm
E1800	Emission in GSM band 1800 MHz	BW = 200 kHz ⁽⁷⁾ ⁽⁹⁾ ⁽¹⁰⁾	-	-87	-84	dBm
E1900	Emission in GSM band 1900 MHz	BW = 200 kHz ⁽⁷⁾ ⁽⁹⁾ ⁽¹⁰⁾	-	-87	-84	dBm
Ewcdma	Emission in WCDMA band	BW = 3.8 MHz ⁽⁷⁾ ⁽⁹⁾ ⁽¹⁰⁾	-	-78	-75	dBm

- Lower transmit power (i.e. Class 2) can be obtained by programming the radio init power table via software parameter download or an HCI command.
- Power of GFSK part.
- Relative power of EDR part compared to the GFSK part.
- At antenna with maximum output power, filter attenuation of 2.3 dB.
- Phase noise will add maximum [-10 kHz;10 kHz] for worst case clock 270 mVpp at 13 MHz.
- Worst case clock 270 mVpp at 13 MHz. Measurement according to EDR RF test spec V2.0.E.3 [].
- With maximum output power (BR or EDR).
- Measured on reference design STLC2555_rev1.1 following eBOM and layout recommendations.
- Measurement bandwidth.
- Transmitting DH5 packets.