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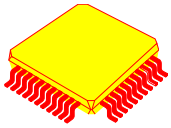
STA308A

Multi-channel digital audio processor with DDX™

Features

- 8 channels of 24-bit DDX®
- >100 dB SNR and dynamic range
- Selectable 32 kHz - 192 kHz input sample rates
- 6 channels of DSD/SACD input
- Digital gain/attenuation +58 dB to -100 dB in 0.5 dB steps
- Soft volume update
- Individual channel and master gain/attenuation plus channel trim (-10 dB to +10 dB)
- Up to 10 independent 32-bit user programmable biquads (EQ) per channel
- Bass/treble tone control
- Pre and post EQ full 8-channel input mix on all 8 channels
- Dual independent limiters/compressors
- Dynamic range compression or anti-clipping modes
- AutoModes:
  - 5-band graphic EQ
  - 32 preset EQ curves (rock, jazz, pop, etc.)
  - Automatic volume controlled loudness
  - 5.1 to 2-channel downmix
  - Simultaneous 5.1- and 2-channel downmix outputs
  - 3 preset volume curves
  - 2 preset anti-clipping modes
  - Preset movie nighttime listening mode
  - Preset TV channel/commercial AGC mode
  - 5.1, 2.1 bass management configurations
  - AM frequency automatic output PWM frequency shifting
  - 8 preset crossover filters
- Individual channel and master soft/hard mute
- Automatic zero-detect and invalid input mute
- Automatic invalid input detect mute



TQFP64

- Advanced PopFree operation
- Advanced AM interference frequency switching and noise suppression modes
- I^2S output channel mapping function
- Independent channel volume and DSP bypass
- Channel mapping of any input to any processing/DDX® channel
- DC blocking selectable high-pass filter
- Selectable per-channel DDX® damped ternary or binary PWM output
- Max power correction for lower full-power THD
- Variable per channel DDX® output delay control
- 192 kHz internal processing sample rate, 24-bit to 36-bit precision

Description

The STA308A is a single chip solution for digital audio processing and control in multi-channel applications. It provides output capabilities for DDX® (direct digital amplification). In conjunction with a DDX® power device, it provides high-quality, high-efficiency, all digital amplification. The device is extremely versatile, allowing for input of most digital formats including 6.1/7.1-channel and 192 kHz, 24-bit DVD-audio, DSD/SACD. In 5.1 application the additional 2 channels can be used for audio line-out or headphone drive. In speaker mode, with 8 channel outputs in parallel, the STA308A can deliver 1 W (maximum).

Table 1. Device summary

Order code	Package
STA308A	TQFP64

Contents

List of tables

List of figures

1 Block diagram

Figure 1. Block diagram

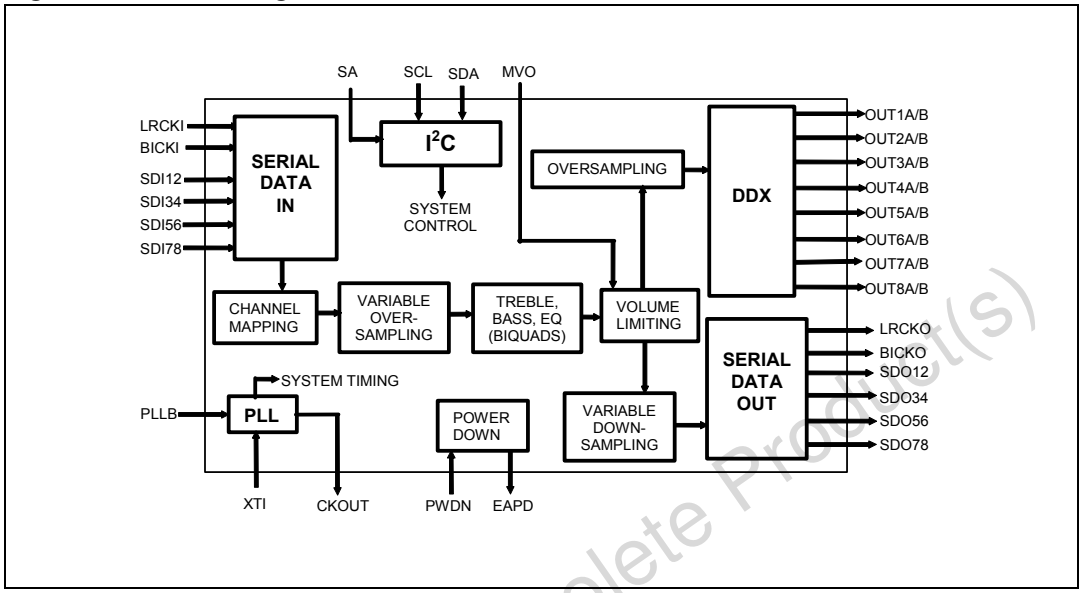
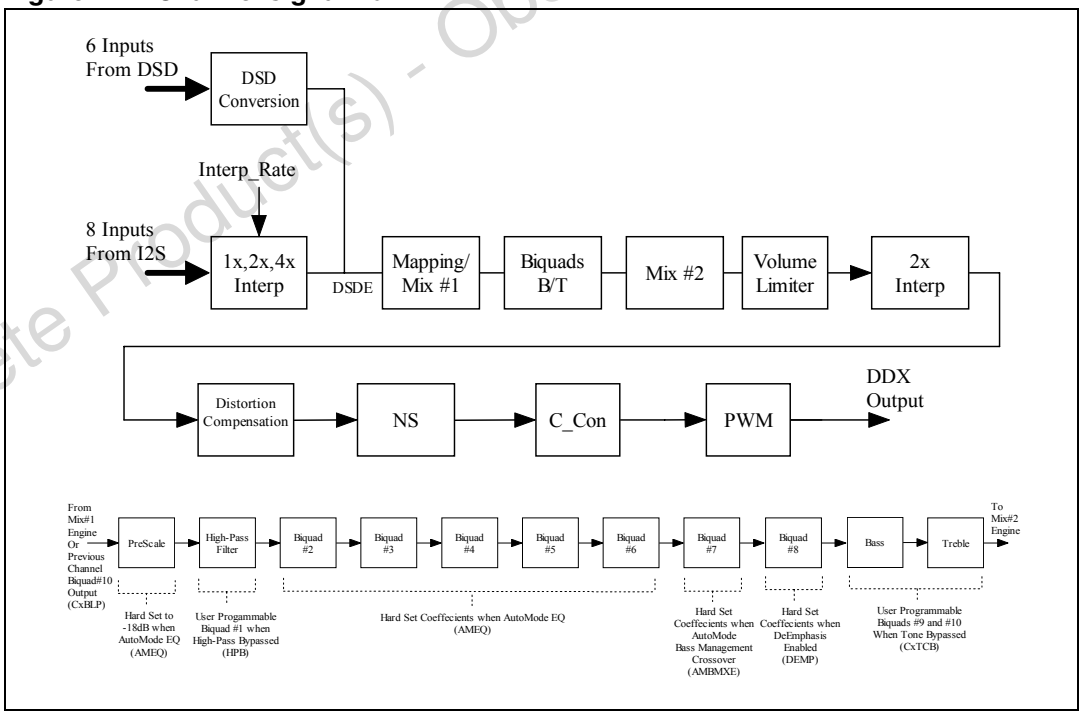


Figure 2. Channel signal flow



2 Pin connections

Figure 3. Pin connection (Top view)

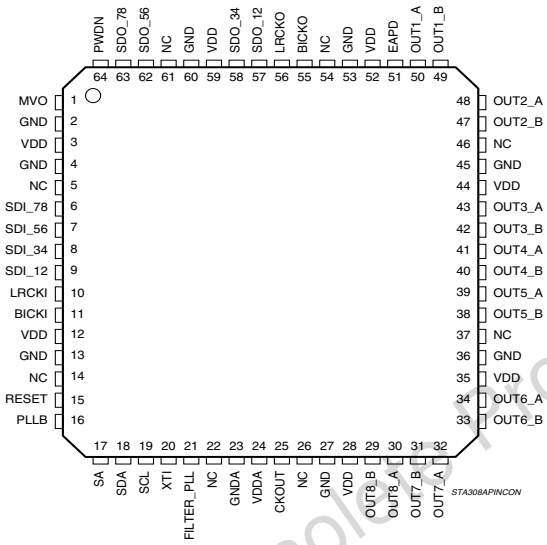


Table 2. Pin description

Pin	Type	Name	Description
1	5-V tolerant TTL input buffer	MVO/DSD_CLK	Master volume override/ DSD input clock
6	5-V tolerant TTL input buffer	SDI_78/DSD_6	Input serial data channels 7 & 8/ DSD input channel 6
7	5-V tolerant TTL input buffer	SDI_56/DSD_5	Input serial data channels 5 & 6/ DSD input channel 5
8	5-V tolerant TTL input buffer	SDI_34/DSD_4	Input serial data channels 3 & 4/ DSD input channel 4
9	5-V tolerant TTL input buffer	SDI_12/DSD_3	Input serial data channels 1 & 2/ DSD input channel 3
10	5-V tolerant TTL input buffer	LRCKI/DSD_2	Input left/right clock/ DSD input channel 2
11	5-V tolerant TTL input buffer	BICKI/DSD_1	Input serial clock/ DSD input channel 1
15	5-V tolerant TTL schmitt trigger input buffer	RESET	Global reset
16	CMOS input buffer with pull-down	PLL_BYPASS	Bypass phase locked loop

Table 2. Pin description (continued)

Pin	Type	Name	Description
17	CMOS input buffer with pull-down	SA	Select address (I^2C)
18	Bidirectional buffer: 5-V tolerant TTL schmitt trigger input; 3.3-V capable 2mA slew-rate controlled output.	SDA	Serial data (I^2C)
19	5-V tolerant TTL schmitt trigger input buffer	SCL	Serial clock (I^2C)
20	5-V tolerant TTL schmitt trigger input buffer	XTI	Crystal oscillator input (clock input)
21	Analog pad	FILTER_PLL	PLL filter
23	Analog ground	GNDA	PLL ground
24	3.3V analog supply voltage	VDDA	PLL supply
25	3.3-V capable TTL tristate 4mA output buffer	CKOUT	Clock output
29	3.3-V capable TTL 2mA output buffer	OUT8B	PWM channel 8 output B
30	3.3-V capable TTL 2mA output buffer	OUT8A	PWM channel 8 output A
31	3.3-V capable TTL 2mA output buffer	OUT7B	PWM channel 7 output B
32	3.3-V capable TTL 2mA output buffer	OUT7A	PWM channel 7 output A
33	3.3-V capable TTL 2mA output buffer	OUT6B	PWM channel 6 output B
34	3.3-V capable TTL 2mA output buffer	OUT6A	PWM channel 6 output A
38	3.3-V capable TTL 2mA output buffer	OUT5B	PWM channel 5 output B
39	3.3-V capable TTL 2mA output buffer	OUT5A	PWM channel 5 output A
40	3.3-V capable TTL 2mA output buffer	OUT4B	PWM channel 4 output B
41	3.3-V capable TTL 2mA output buffer	OUT4A	PWM channel 4 output A
42	3.3-V capable TTL 2mA output buffer	OUT3B	PWM channel 3 output B
43	3.3-V capable TTL 2mA output buffer	OUT3A	PWM channel 3 output A
47	3.3-V capable TTL 2mA output buffer	OUT2B	PWM channel 2 output B

Table 2. Pin description (continued)

Pin	Type	Name	Description
48	3.3-V capable TTL 2mA output buffer	OUT2A	PWM channel 2 output A
49	3.3-V capable TTL 2mA output buffer	OUT1B	PWM channel 1 output B
50	3.3-V capable TTL 2mA output buffer	OUT1A	PWM channel 1 output A
51	3.3-V capable TTL 4mA output buffer	EAPD	Ext. amp power-down
55	3.3-V capable TTL 2mA output buffer	BICKO	Output serial clock
56	3.3-V capable TTL 2mA output buffer	LRCKO	Output left/right clock
57	3.3-V capable TTL 2mA output buffer	SDO_12	Output serial data channels 1&2
58	3.3-V capable TTL 2mA output buffer	SDO_34	Output serial data channels 3&4
62	3.3-V capable TTL 2mA output buffer	SDO_56	Output serial data channels 5&6
63	3.3-V capable TTL 2mA output buffer	SDO_78	Output serial data channels 7&8
64	5-V tolerant TTL schmitt trigger input buffer	PWDN	Device power-down
3,12,28,35, 44,52,59	3.3-V digital supply voltage	VDD	3.3-V supply
2,4,13,27, 36,45,53,60	Digital ground	GND	Ground
5, 14, 22, 26,37,46,54, 61		NC	Not connected

3 Electrical specification

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	3.3-V I/O power supply	-0.5		4	V
V_{DDA}	3.3-V logic power supply	-0.5		4	V
V_i	Voltage on input pins	-0.5		VDD + 0.5	V
V_o	Voltage on output pins	-0.5		VDD + 0.3	V
T_{stg}	Storage temperature	-40		150	°C
T_{amb}	Ambient operating temperature	-40		90	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{thj\text{-}amb}$	Thermal resistance, junction to ambient		85		°C/W

3.3 Recommended operating condition

Table 5. Recommended operating condition

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	I/O power supply	3.0		3.6	V
V_{DDA}	Logic power supply	3.0		3.6	V
T_j	Operating junction temperature	-40		125	°C

3.4 Electrical specifications

The following specifications are valid for VDD = 3.3V ± 0.3V, VDDA = 3.3V ± 0.3V and Tamb = 0 to 70 °C, unless otherwise stated

Table 6. General interface electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Low-level input no pull-up	V_i = 0V			1 (1)	µA
I_{ih}	High-level input no pull-down	$V_i = V_{DD}$			2	µA
I_{OZ}	Tristate output leakage without pull-up/down	$V_i = V_{DD}$			2	µA
V_{esd}	Electrostatic protection (human body model)	Leakage < 1µA	2000			V

1. The leakage currents are generally very small, < 1 nA. The values given here are maximum after an electrostatic stress on the pin.

Table 7. DC electrical characteristics: 3.3-V buffers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
V_{ILhyst}	Low-level threshold	Input falling	0.8		1.35	V
V_{IHhyst}	High-level threshold	Input rising	1.3		2.0	V
V_{hyst}	Schmitt trigger hysteresis		0.3		0.8	V
V_{ol}	Low-level output	Iol = 100uA			0.2	V
V_{oh}	High-level output	Ioh = -100uA	VDD-0.2			V
		Ioh = -2mA	2.4			V

4 Pin description

Master volume override (MVO)

This pin enables the user to bypass the volume control on all channels. When MVO is pulled high, the master volume register is set to 0x00, which corresponds to its full scale setting. The master volume register setting offsets the individual channel volume settings, which default to 0 dB.

Serial data in (SDI_12, SDI_34, SDI_56, SDI_78)

Audio information enters the device here. Six format choices are available including I^2S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

RESET

Driving this pin low turns off the outputs and returns all settings to their defaults.

I^2C bus

The SA, SDA and SCL pins operate per the Phillips I^2C specification. See Section 5.

Phase locked loop (PLL)

The phase locked loop section provides the system timing signals and CKOUT.

Clock output (CKOUT)

System synchronization and master clocks are provided by the CKOUT.

PWM outputs (OUT1 through OUT8)

The PWM outputs provide the input signal for the power devices.

External amplifier power-down (EAPD)

This signal can be used to control the power-down of DDX power devices.

Serial data out (SDO_12, SDO_34, SDO_56, SDO_78)

These are the outputs for audio information. Six different formats are available including I^2S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

Device power-down (PWDN)

Pulling PWDN low begins the power-down sequence which puts the STA308A into a low-power state. EAPD (pin 51) goes low approximately 30 ms later.

5 I²C bus operation

The STA308A supports the I²C protocol via the input ports SCL and SDA_IN (master to slave) and the output port SDA_OUT (slave to master).

This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver.

The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA308A is always a slave device in all of its communications.

5.1 Communication protocol

5.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

5.1.2 Start condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

5.1.3 Stop condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between STA308A and the bus master.

5.1.4 Data input

During the data input the STA308A samples the SDA signal on the rising edge of clock SCL.

For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

5.2 Device addressing

To start communication between the master and the Omega DDX core, the master must initiate with a start condition. Following this, the master sends 8 bits onto the SDA line (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA308A the I²C interface has two device addresses depending on the SA port configuration, 0x40 or 0100000x when SA = 0, and 0x42 or 0100001x when SA = 1.

The 8th bit (LSB) identifies read or write operation RW, this bit is set to 1 in read mode and 0 for write mode. After a START condition the STA308A identifies on the bus the device

address and if a match is found, it acknowledges the identification on SDA bus during the 9th-bit time. The byte following the device identification byte is the internal space address.

5.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA308A acknowledges this and the writes for the byte of internal address.

After receiving the internal byte address the STA308A again responds with an acknowledgement.

5.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by the Omega DDX core. The master then terminates the transfer by generating a STOP condition.

5.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 4. Write mode sequence

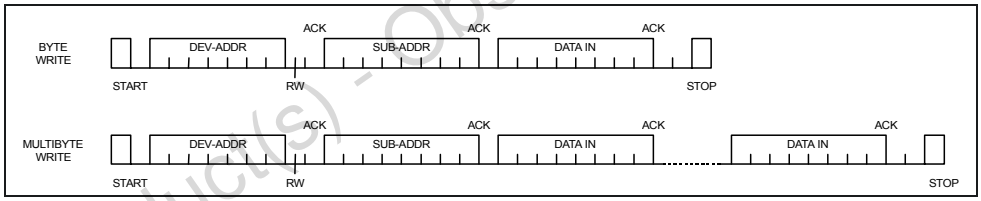
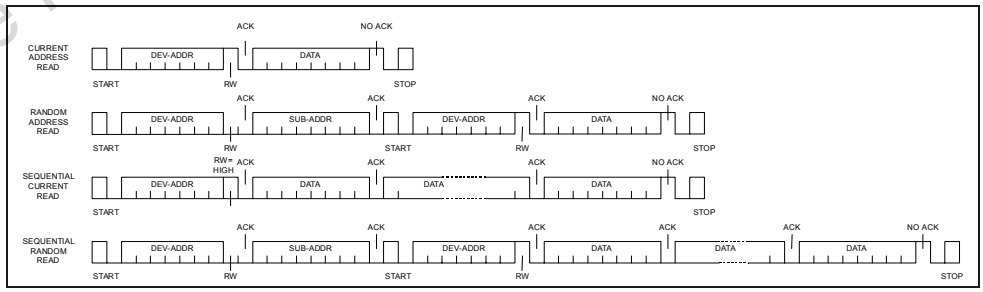
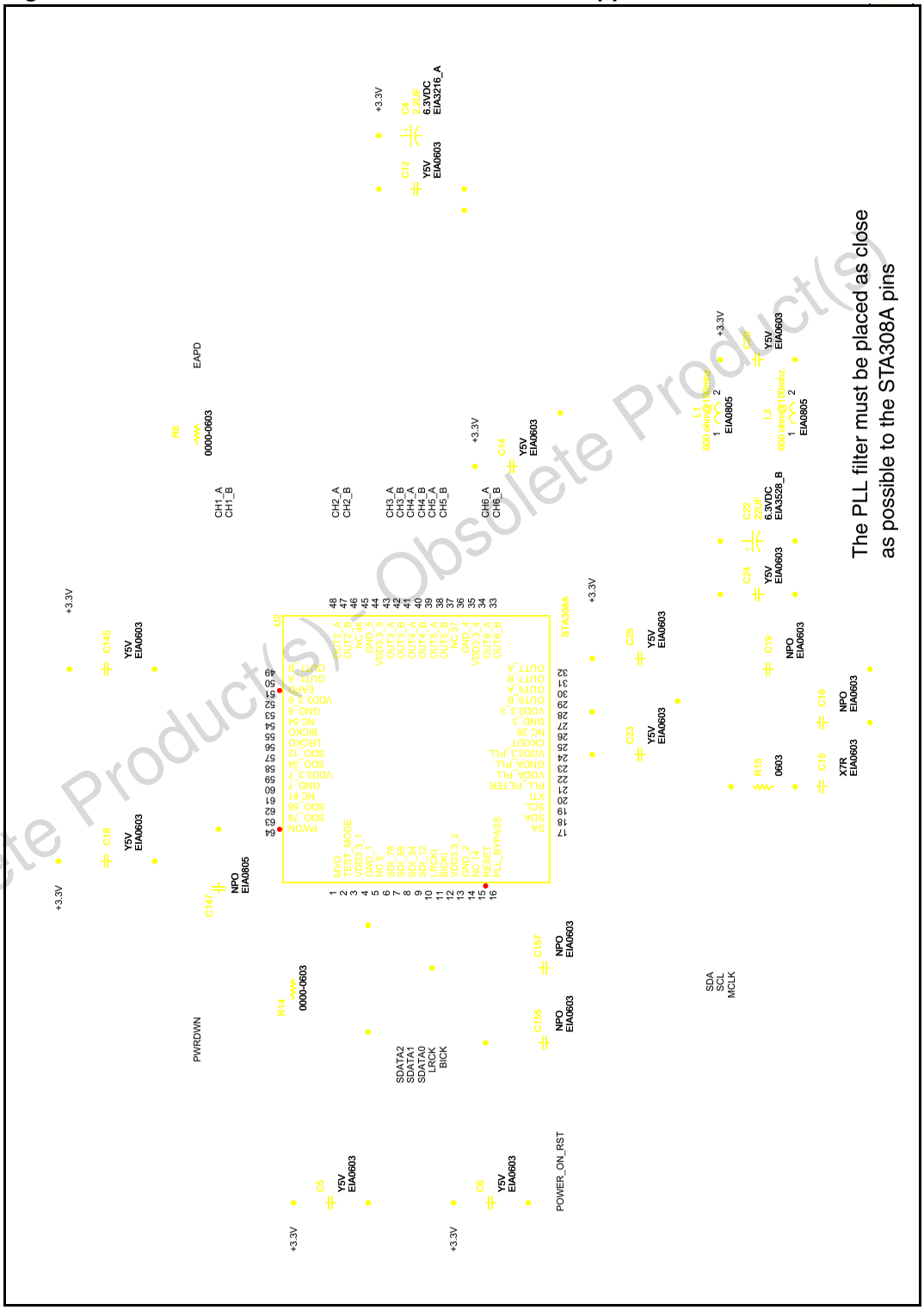


Figure 5. Read mode sequence



6 Application reference schematic

Figure 6. Reference schematic for STA308A-based application



7 Registers

7.1 Register summary

Table 8. Register summary

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
Configuration									
0x00	CONFA	COS1	COS0	DSPB	IR1	IR0	MCS2	MCS1	MCS0
0x01	ConfB				SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	ConfC				SAOFB	SAO3	SAO2	SAO1	SAO0
0x03	ConfD	MPC	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x04	ConfE	C8BO	C7BO	C6BO	C5BO	C4BO	C3BO	C2BO	C1BO
0x05	ConfF	PWMS2	PWMS1	PWMS0	BQL	PSL	DEMP	DRC	HPB
0x06	ConfG	MPCV	DCCV	HPE	AM2E	AME	COD	SID	PWMD
0x07	ConfH	ECLE	LDTE	BCLE	IDE	ZDE	SVE	ZCE	NSBW
0x08	ConfI	EAPD							PSCE
Volume control									
0x09	MMUTE								MMUTE
0x0A	Mvol	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x0B	C1Vol	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x0C	C2Vol	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0D	C3Vol	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0x0E	C4Vol	C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
0x0F	C5Vol	C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
0x10	C6Vol	C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
0x11	C7Vol	C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
0x12	C8Vol	C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
0x13	C1VTMB	C1M	C1VBP		C1VT4	C1VT3	C1VT2	C1VT1	C1VT0
0x14	C2VTMB	C2M	C2VBP		C2VT4	C2VT3	C2VT2	C2VT1	C2VT0
0x15	C3VTMB	C3M	C3VBP		C3VT4	C3VT3	C3VT2	C3VT1	C3VT0
0x16	C4VTMB	C4M	C4VBP		C4VT4	C4VT3	C4VT2	C4VT1	C4VT0
0x17	C5VTMB	C5M	C5VBP		C5VT4	C5VT3	C5VT2	C5VT1	C5VT0
0x18	C6VTMB	C6M	C6VBP		C6VT4	C6VT3	C6VT2	C6VT1	C6VT0
0x19	C7VTMB	C7M	C7VBP		C7VT4	C7VT3	C7VT2	C7VT1	C7VT0
0x1A	C8VTMB	C8M	C8VBP		C8VT4	C8VT3	C8VT2	C8VT1	C8VT0
Input mapping									
0x1B	C12im		C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0

Table 8. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x1C	C34im		C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
0x1D	C56im		C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
0x1E	C78im		C8IM2	C8IM1	C8IM0		C7IM2	C7IM1	C7IM0
AutoMode									
0x1F	Auto1	AMDM	AMGC2	AMGC1	AMGC0	AMV1	AMV0	AMEQ1	AMEQ0
0x20	Auto2	SUB	RSS1	RSS0	CSS1	CSS0	FSS	AMBMXE	AMBMME
0x21	Auto3	AMAM2	AMAM1	AMAM0	AMAME			MSA	AMPS
0x22	PreEQ	XO2	XO1	XO0	PEQ4	PEQ3	PEQ2	PEQ1	PEQ0
0x23	Ageq				AGEQ4	AGEQ3	AGEQ2	AGEQ1	AGEQ0
0x24	Bgeq				BGEQ4	BGEQ3	BGEQ2	BGEQ1	BGEQ0
0x25	Cgeq				CGEQ4	CGEQ3	CGEQ2	CGEQ1	CGEQ0
0x26	Dgeq				DGEQ4	DGEQ3	DGEQ2	DGEQ1	DGEQ0
0x27	Egeq				EGEQ4	EGEQ3	EGEQ2	EGEQ1	EGEQ0
Processing loop									
0x28	BQlp	C8BLP	C7BLP	C6BLP	C5BLP	C4BLP	C3BLP	C2BLP	C1BLP
0x29	MXlp	C8MXLP	C7MXLP	C6MXLP	C5MXLP	C4MXLP	C3MXLP	C2MXLP	C1MXLP
Processing pypass									
0x2A	EQbp	C8EQBP	C7EQBP	C6EQBP	C5EQBP	C4EQBP	C3EQBP	C2EQBP	C1EQBP
0x2B	ToneBP	C8TCB	C7TCB	C6TCB	C5TCB	C4TCB	C3TCB	C2TCB	C1TCB
Tone control									
0x2C	Tone	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
Dynamics control									
0x2D	C1234ls	C4LS1	C4LS0	C3LS1	C3LS0	C2LS1	C2LS0	C1LS1	C1LS0
0x2E	C5678ls	C8LS1	C8LS0	C7LS1	C7LS0	C6LS1	C6LS0	C5LS1	C5LS0
0x2F	L1ar	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x30	L1atrt	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0x31	L2ar	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0x32	L2atrt	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
PWM output timing									
0x33	C12ot		C2OT2	C2OT1	C2OT0		C1OT2	C1OT1	C1OT0
0x34	C34ot		C4OT2	C4OT1	C4OT0		C3OT2	C3OT1	C3OT0
0x35	C56ot		C6OT2	C6OT1	C6OT0		C5OT2	C5OT1	C5OT0
0x36	C78ot		C8OT2	C8OT1	C8OT0		C7OT2	C7OT1	C7OT0
I^2S output channel mapping									
0x37	C12om		C2OM2	C2OM1	C2OM0		C1OM2	C1OM1	C1OM0

Table 8. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x38	C34om		C4OM2	C4OM1	C4OM0		C3OM2	C3OM1	C3OM0
0x39	C56om		C6OM2	C6OM1	C6OM0		C5OM2	C5OM1	C5OM0
0x3A	C78om		C8OM2	C8OM1	C8OM0		C7OM2	C7OM1	C7OM0
User-defined coefficient RAM									
0x3B	Cfaddr1							CFA9	CFA8
0x3C	Cfaddr2	CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0x3D	B1cf1	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0x3E	B1cf2	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0x3F	B1cf3	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0x40	B2cf1	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0x41	B2cf2	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0x42	B2cf3	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0x43	A1cf1	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
0x44	A1cf2	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0x45	A1cf3	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0x46	A2cf1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0x47	A2cf2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0x48	A2cf3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0x49	B0cf1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0x4A	B0cf2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0x4B	B0cf3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0x4C	Cfud							WA	W1
0x4D	MPCC1	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x4E	MPCC2	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x4F	DCC1	DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
0x50	DCC2	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0x51	PSC1	RCV11	RCV10	RCV9	RCV8	RCV7	RCV6	RCV5	RCV4
0x52	PSC2	RCV3	RCV2	RCV1	RCV0	CNV11	CNV10	CNV9	CNV8
0x53	PSC3	CNV7	CNV6	CNV5	CNV4	CNV3	CNV2	CNV1	CNV0

7.2 Register description

7.2.1 Configuration register A (0x00)

D7	D6	D5	D4	D3	D2	D1	D0
COS1	COS0	DSPB	IR1	IR0	MCS2	MCS1	MCS0
1	0	0	0	0	0	1	1

Bit	RW	RST	Name	Description
0	RW	1	MCS0	Master clock select: selects the ratio between the input I^2S sample frequency and the input clock.
1	RW	1	MCS1	
2	RW	0	MCS2	

The DDX8000 supports sample rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz, and 2.8224 MHz DSD. Therefore the internal clocks are:

- 65.536 MHz for 32 kHz
- 90.3168 MHz for 44.1 kHz, 88.2 kHz, 176.4 kHz, and DSD
- 98.304 MHz for 48 kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency (fs). The relationship between the input clock and the input sample rate is determined by both the MCSn and the IRn (input rate) register bits. The MCSn bits determine the PLL factor generating the internal clock and the IRn bits determine the oversampling ratio used internally.

Input sample rate *fs* (kHz)	IR	MCS[2:0]				
		1XX	011	010	001	000
32, 44.1, 48	00	128 * fs	256 * fs	384 * fs	512 * fs	768 * fs
88.2, 96	01	64 * fs	128 * fs	192 * fs	256 * fs	384 * fs
176.4, 192	10	64 * fs	128 * fs	192 * fs	256 * fs	384 * fs
DSD	11	2 * fs	4 * fs	6 * fs	8 * fs	10 * fs

Interpolation ratio select

Bit	RW	RST	Name	Description
3	RW	0	IR0	Interpolation ratio select: selects internal interpolation ratio based on input I^2S sample frequency
4	RW	0	IR1	

The STA308A has variable interpolation (oversampling) settings such that internal processing and DDX output rates remain consistent. The first processing block interpolates by either 4 times, 2 times, or 1 time (pass-through).

The oversampling ratio of this interpolation is determined by the IR bits.

IR[1,0]	Input sample rate *Fs* (kHz)	1st stage interpolation ratio
00	32	4-times oversampling
00	44.1	4-times oversampling
00	48	4-times oversampling
01	88.2	2-times oversampling
01	96	2-times oversampling
10	176.4	Pass-through
10	192	Pass-through
11	DSD	DSD to 176.4 kHz conversion

Bit	RW	RST	Name	Description
0	RW	0	DSPB	DSP bypass bit: 0: normal operation 1: bypass of biquad and bass/treble functions

Setting the DSPB bit bypasses the biquad function of the Omega DDX core.

COS[1,0]	CKOUT frequency
00	PLL output
01	PLL output / 4
10	PLL output / 8
11	PLL output / 16

7.2.2 Configuration register B (0x01) - serial input formats

D7	D6	D5	D4	D3	D2	D1	D0
			SAIFB	SAI3	SAI2	SAI1	SAI0
			0	0	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	SAI0	Serial audio input interface format: determines the interface format of the input serial digital audio interface.
1	RW	0	SAI1	
2	RW	0	SAI2	
3	RW	0	SAI3	

Serial data interface

The STA308A audio serial input interfaces with standard digital audio components and accepts a number of serial data formats. STA308A always acts a slave when receiving audio input from standard digital audio components. Serial data for eight channels is provided using 6 input pins: left/right clock LRCKI (pin 10), serial clock BICKI (pin 11), serial data 1 and 2 SDI12 (pin 9), serial data 3 and 4 SDI34 (pin 8), serial data 5 and 6 SDI56 (pin 7), and serial data 7 and 8 SDI78 (pin 6). The SAI/SAIFB register (Configuration Register B, address 0x01) is used to specify the serial data format. The default serial data format is I^2S, MSB-first. Available formats are shown in the tables and figure that follow.

Bit	RW	RST	Name	Description
4	RW	0	SAIFB	Determines MSB or LSB first for all SAO formats: 0: MSB first 1: LSB first

Note: Serial input and output formats are specified separately

For example, SAI = 1110 and SAIFB = 1 would specify right-justified 16-bit data, LSB-first.

The table below lists the serial audio input formats supported by STA308A as related to BICKI = 32 * fs, 48 * fs, 64 * fs, where sampling rate, fs = 32, 44.1, 48, 88.2, 96, 176.4, 192 kHz.

BICKI	SAI [3:0]	SAIFB	Interface format
32 * fs	1100	X	I^2S 15-bit data
	1110	X	Left/right-justified 16-bit data
48 * fs	0100	X	I^2S 23-bit data
	0100	X	I^2S 20-bit data
	1000	X	I^2S 18-bit data
	0100	0	MSB-first I^2S 16-bit data
	1100	1	LSB-first I^2S 16-bit data
	0001	X	Left-justified 24-bit data
	0101	X	Left-justified 20-bit data
	1001	X	Left-justified 18-bit data
	1101	X	Left-justified 16-bit data
	0010	X	Right-justified 24-bit data
	0110	X	Right-justified 20-bit data
	1010	X	Right-justified 18-bit data
	1110	X	Right-justified 16-bit data
64 * fs	0000	X	I^2S 24-bit data
	0100	X	I^2S 20-bit data
	1000	X	I^2S 18-bit data
	0000	0	MSB-first I^2S 16-bit data
	1100	1	LSB-first I^2S 16-bit data
	0001	X	Left-justified 24-bit data
	0101	X	Left-justified 20-bit data
	1001	X	Left-justified 18-bit data
	1101	X	Left-justified 16-bit data
	0010	X	Right-justified 24-bit data
	0110	X	Right-justified 20-bit data
	1010	X	Right-justified 18-bit data
	1110	X	Right-justified 16-bit data

7.2.3 Configuration register C (0x02) - serial output formats

D7	D6	D5	D4	D3	D2	D1	D0
			SAOFB	SAO3	SAO2	SAIO	SAO0
			0	0	0	0	0

Bit	RW	RST	Name	Description
0	RW	0	SAO0	Serial audio output interface format: determines the interface format of the output serial digital audio interface.
1	RW	0	SAO1	
2	RW	0	SAO2	
3	RW	0	SAO3	

The STA308A features a serial audio output interface that consists of 8 channels. The serial audio output always acts as a slave to the serial audio input interface and, therefore, all output clocks are synchronous with the input clocks. The output sample frequency (fs) is also equivalent to the input sample frequency. In the case of SACD/DSD input, the serial audio output acts as a master with an output sampling frequency of 176.4 kHz. The output serial format can be selected independently from the input format and is done via the SAO and SAOFB bits.

Bit	RW	RST	Name	Description
4	RW	0	SAOFB	Determines MSB or LSB first for all SAO formats: 0: MSB first 1: LSB first

BICKI = BICKO	SAO[3:0]	Interface data format
32 * fs	0111	I^2S data
	1111	Left/right-justified 16-bit data
48 * fs	1110	I^2S data
	0001	Left-justified data
	1010	Right-justified 24-bit data
	1011	Right-justified 20-bit data
	1100	Right-justified 18-bit data
	1101	Right-justified 16-bit data
64 * fs	0000	I^2S data
	0001	Left-justified data
	0010	Right-justified 24-bit data
	0011	Right-justified 20-bit data
	0100	Right-justified 18-bit data
	0101	Right-justified 16-bit data