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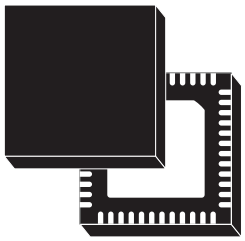
STA311B

Multichannel digital audio processor with FFX™

Datasheet - production data



VFQFN-56

Features

- 8 channels of 24-bit FFX™
- >100 dB SNR and dynamic range
- Selectable 32 kHz-192 kHz input sampling rates
- 6 channels of DSD/SACD
- Digital gain/attenuation +58 dB to -100 dB in 0.5 dB steps
- Advanced “pop-free” operation
- Digital “pop-free” operation for single-ended mode
- Soft volume update
- Individual channel and master gain/attenuation plus channel trim (-10 dB to +10 dB)
- Up to 10 independent 32-bit user-programmable biquads (EQ) per channel
- Bass/treble tone control
- Pre- and post-EQ full 8-channel input mix on all 8 channels
- Dual independent limiters/compressors
- Dynamic range compression or anti-clipping modes
- AutoModes
  - 5-band graphic EQ
  - 32 preset EQ curves (rock, jazz, pop, etc.)
  - Automatic volume-controlled loudness
  - 5.1 to 2-channel downmix
  - Simultaneous 5.1- and 2-channel downmix outputs
  - 3 preset volume curves
  - 2 preset anti-clipping modes
  - Preset movie nighttime listening mode
  - Preset TV channel/commercial AGC mode
  - 5.1, 2.1 bass management configurations
  - AM frequency automatic output PWM frequency shifting
  - 8 preset crossover filters
- Individual channel and master soft/hard mute
- Automatic zero-detect and invalid input mute
- Automatic amplifier power-down on clock loss
- Advanced AM interference frequency switching and noise suppression modes
- I²S output channel mapping function
- Independent channel volume and DSP bypass
- Channel mapping of any input to any processing/FFX channel
- Selectable per-channel FFX damped ternary or binary PWM output
- Max power correction for lower full-power THD
- Variable per-channel FFX output delay control
- 192 kHz internal processing sampling rate, 24-bit to 36-bit precision

Table 1. Device summary

Order code	Package	Packaging
STA311B	VFQFPN56	Tray
STA311BTR	VFQFPN56	Tape and reel

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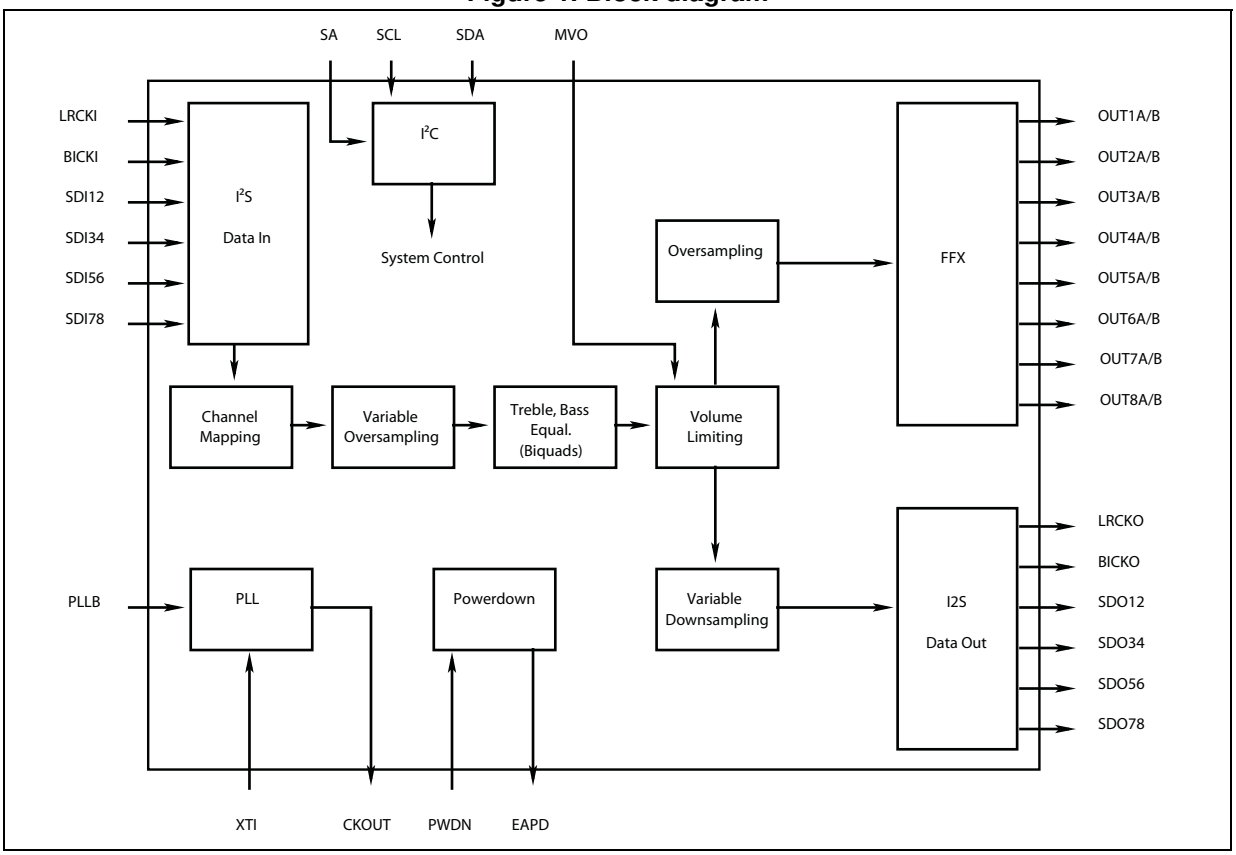
1 Description

The STA311B is a single-chip solution for digital audio processing and control in multichannel applications and provides output capabilities for FFX™ (full flexible amplification). In conjunction with an FFX™ power device, it provides high-quality, high-efficiency, all digital amplification. The device is extremely versatile, allowing for input of most digital formats including 6.1/7.1-channel and 192 kHz, 24-bit DVD-audio, DSD/SACD. In the 5.1 application the additional 2 channels can be used for audio line-out or headphone drive.

2 Device overview

2.1 Block diagram

Figure 1. Block diagram



2.2 Pin description

Figure 2. Pin connections VFQFPN-56 (top view)

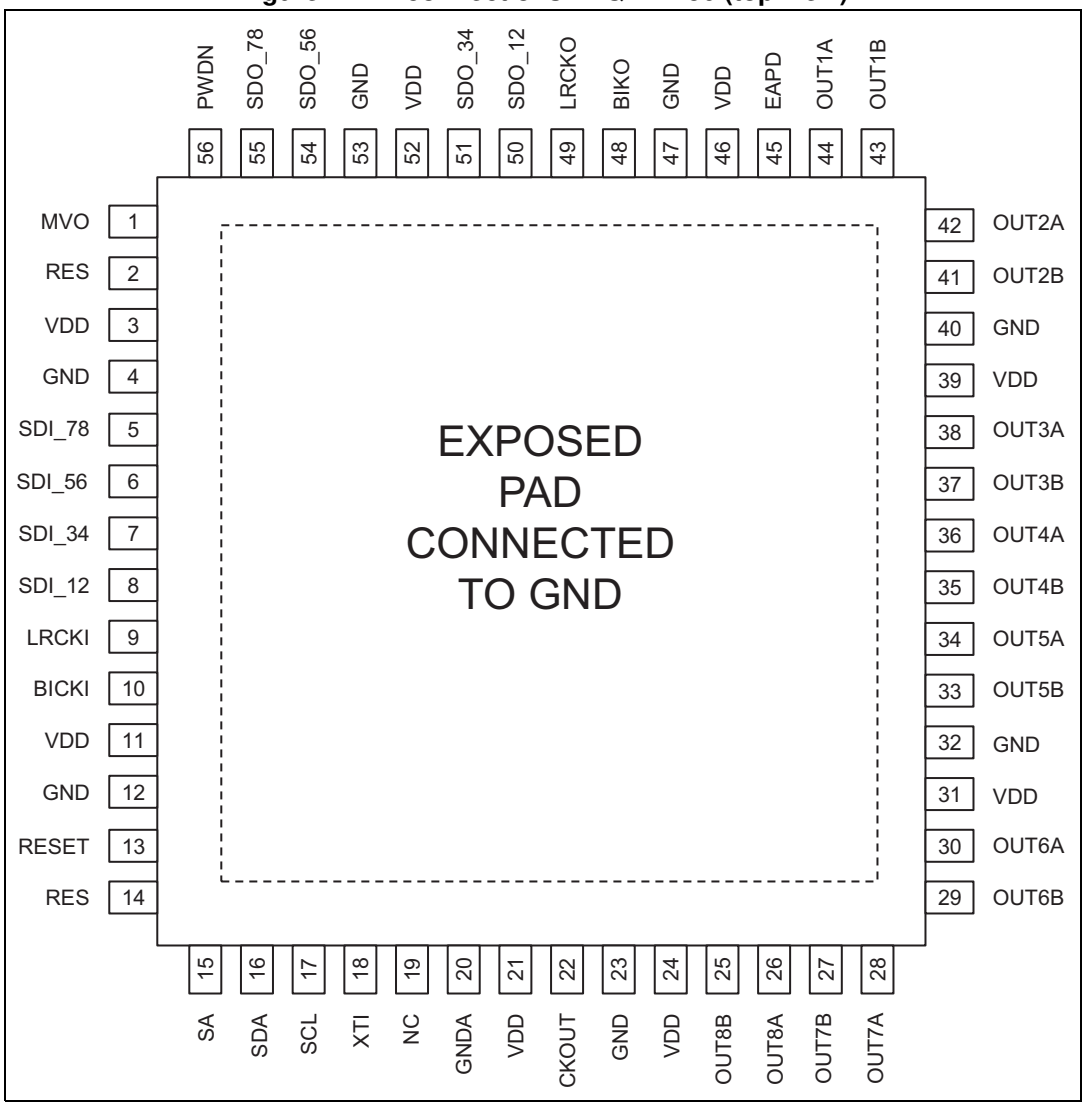


Table 2. Pin description

Pin	Type	Name	Description
1	5-V tolerant TTL input buffer	MVO/DSD_CLK	Master volume override/ DSD input clock
2	Reserved	RES	Connect to GND
5	5-V tolerant TTL input buffer	SDI_78/DSD_6	Input serial data channels 7 & 8/ DSD input channel 6
6	5-V tolerant TTL input buffer	SDI_56/DSD_5	Input serial data channels 5 & 6/ DSD input channel 5
7	5-V tolerant TTL input buffer	SDI_34/DSD_4	Input serial data channels 3 & 4/ DSD input channel 4
8	5-V tolerant TTL input buffer	SDI_12/DSD_3	Input serial data channels 1 & 2/ DSD input channel 3
9	5-V tolerant TTL input buffer	LRCKI/DSD_2	Input left/right clock/ DSD input channel 2
10	5-V tolerant TTL input buffer	BICKI/DSD_1	Input serial clock/ DSD input channel 1
18	5-V tolerant TTL Schmitt trigger input buffer	RESETN	Global reset
14	Reserved	RES	Connect to GND
15	1.8V CMOS input buffer with pull-down	SA	Select address (I²C)
16	Bidirectional buffer: 5-V tolerant TTL Schmitt trigger input; 3.3-V capable 2 mA slew-rate controlled output.	SDA	Serial data (I²C)
17	5-V tolerant TTL Schmitt trigger input buffer	SCL	Serial clock (I²C)
18	5-V tolerant TTL Schmitt trigger input buffer	XTI	Crystal oscillator input (clock input)
19	Not connected	NC	Reserved
20	Analog ground	GNDA	PLL ground
22	3.3-V capable TTL tristate 4 mA output buffer	CKOUT	Clock output
25	3.3-V capable TTL 2 mA output buffer	OUT8B	PWM channel 8 output B
26	3.3-V capable TTL 2 mA output buffer	OUT8A	PWM channel 8 output A
27	3.3-V capable TTL 2 mA output buffer	OUT7B	PWM channel 7 output B
28	3.3-V capable TTL 2 mA output buffer	OUT7A	PWM channel 7 output A
29	3.3-V capable TTL 2 mA output buffer	OUT6B	PWM channel 6 output B
30	3.3-V capable TTL 2 mA output buffer	OUT6A	PWM channel 6 output A
33	3.3-V capable TTL 2 mA output buffer	OUT5B	PWM channel 5 output B
34	3.3-V capable TTL 2 mA output buffer	OUT5A	PWM channel 5 output A
35	3.3-V capable TTL 2 mA output buffer	OUT4B	PWM channel 4 output B

Table 2. Pin description (continued)

Pin	Type	Name	Description
36	3.3-V capable TTL 2 mA output buffer	OUT4A	PWM channel 4 output A
37	3.3-V capable TTL 2 mA output buffer	OUT3B	PWM channel 3 output B
38	3.3-V capable TTL 2 mA output buffer	OUT3A	PWM channel 3 output A
41	3.3-V capable TTL 2 mA output buffer	OUT2B	PWM channel 2 output B
42	3.3-V capable TTL 2 mA output buffer	OUT2A	PWM channel 2 output A
43	3.3-V capable TTL 2 mA output buffer	OUT1B	PWM channel 1 output B
44	3.3-V capable TTL 2 mA output buffer	OUT1A	PWM channel 1 output A
45	3.3-V capable TTL 4 mA output buffer	EAPD	External amp power-down
48	3.3-V capable TTL 2 mA output buffer	BICKO	Output serial clock
49	3.3-V capable TTL 2 mA output buffer	LRCKO	Output left/right clock
50	3.3-V capable TTL 2 mA output buffer	SDO_12	Output serial data channels 1&2
51	3.3-V capable TTL 2 mA output buffer	SDO_34	Output serial data channels 3&4
54	3.3-V capable TTL 2 mA bidirectional buffer	SDO_56	Output serial data channels 5&6 External power bridge fault input
55	3.3-V capable TTL 2mA output buffer	SDO_78	Output serial data channels 7&8 External power bridge tristate signal (‘0’ = tristate)
56	5-V tolerant TTL Schmitt trigger input buffer	PWDN	Device power-down
3, 11,21,24, 31, 39, 46, 52	3.3-V digital supply voltage	VDD	3.3-V supply
4, 12, 23, 32, 40, 47, 53	Digital ground	GND	Ground

Master volume override (MVO)

This pin enables the user to bypass the volume control on all channels. When MVO is pulled high, the master volume register is set to 0x00, which corresponds to its full-scale setting. The master volume register setting offsets the individual channel volume settings, which default to 0 dB.

Serial data in (SDI_12, SDI_34, SDI_56, SDI_78)

Audio information enters the device here. Six format choices are available including I²S, left-justified or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

RESET

Driving this pin low turns off the outputs and returns all settings to their defaults.

I²C bus

The SA, SDA and SCL pins operate per the Phillips I²C specification. See *Section 7: I²C bus operation on page 23*.

Phase-locked loop (PLL)

The phase-locked loop section provides the system timing signals and CKOUT.

Clock output (CKOUT)

System synchronization and master clocks are provided by CKOUT.

PWM outputs (OUT1 through OUT8)

The PWM outputs provide the input signal for the power devices.

External amplifier power-down (EAPD)

This signal can be used to control the power-down of the FFX power devices.

Serial data out (SDO_12, SDO_34, SDO_56, SDO_78)

When the pop-noise removal feature is disabled, these are the outputs for the audio information. Six different formats are available including I²S, left-or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

However, when the pop-noise removal feature is enabled, SDO_12 and SDO_34 output the audio information, whereas SDO_56 is used as the external power bridge fault input and SDO_78 as the external power bridge tristate signal.

Device power-down (PWDN)

Pulling PWDN low begins the power-down sequence which puts the STA311B into a low-power state. EAPD goes low approximately 30 ms later.

Frequency sampling autodetection

The system clock is generated by PLL using XTI or BICKI input, and the ratio (IR) between the frequency sampling (Fs) of the audio serial and the PLL clock has to be set in the appropriate registers via the I²C interface. If the Fs autodetection function has been enabled, the IR parameter will be set automatically based on the Fs input (see *Fs autodetection on page 32*).

3 Electrical characteristics

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	3.3-V I/O power supply	-0.5		4	V
V_i	Voltage on input pins	-0.5		VDD + 0.5	V
V_o	Voltage on output pins	-0.5		VDD + 0.3	V
VSA	Voltage on SA pin 15	-0.5		2.0	V
T_{stg}	Storage temperature	-40		150	°C
T_{amb}	Ambient operating temperature	-40		90	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{thj\text{-}amb}$	Thermal resistance, junction to ambient		85		°C/W

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	I/O power supply	3.0	3.3	3.6	V
VSA	Voltage on SA pin 15	0.0	1.8	1.95	V
T_j	Operating junction temperature	-40	25	125	°C

3.4 Electrical specifications

The following specifications are valid for V_{DD} =3.3 V ± 0.3 V, VSA=0V and T_{amb} = 25 °C, unless otherwise stated.

Table 6. General interface electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Low-level input, no pull-up	V_i = 0 V			1	µA
I_{ih}	High-level input, no pull-down	$V_i = V_{DD}$			2	µA
I_{OZ}	Tristate output leakage without pull-up/down	$V_i = V_{DD}$			2	µA
V_{esd}	Electrostatic protection (human body model)	Leakage < 1 µA	2000			V

Table 7. DC electrical characteristics: 3.3-V buffers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
V_{ILhyst}	Low-level threshold	Input falling	0.8		1.35	V
V_{IHhyst}	High-level threshold	Input rising	1.3		2.0	V
V_{hyst}	Schmitt trigger hysteresis		0.3		0.8	V
V_{ol}	Low-level output	I_{ol} = 100 µA			0.2	V
V_{oh}	High-level output	I_{oh} = -100 µA	VDD-0.2			V
		I_{oh} = -2 mA	2.4			V
Idd	Quiescent current	Reset conditions		15		mA
		Normal conditions with CKOUT		60		mA
fCKOUT		Reset=1 PWDN=1		2.85		MHz

4 Serial audio interface

The STA311B audio serial input interfaces with standard digital audio components and accepts a number of serial data formats. The STA311B always acts as a slave when receiving audio input from standard digital audio components. Serial data for eight channels is provided using 6 input pins: left/right clock LRCKI, serial clock BICKI, serial data 1 and 2 SDI_12, serial data 3 and 4 SDI_34, serial data 5 and 6 SDI_56, and serial data 7 and 8 SDI_78. The SAI/SAIFB register (configuration register B, address 0x01) is used to specify the serial data format. The default serial data format is I²S, MSB-first.

4.1 Timings

In the STA311B, the BICKI and LRCKI pins are configured as inputs and they must be supplied by the external peripheral.

Figure 3. Timing diagram for SAI interface

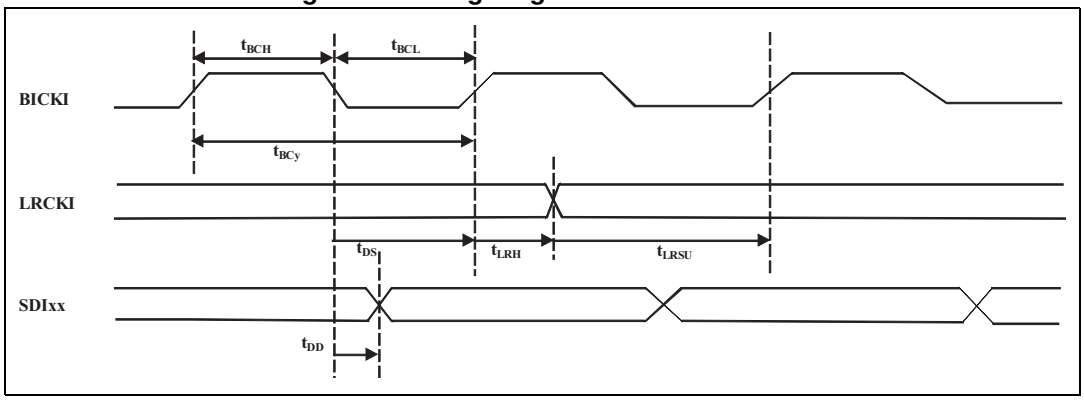


Table 8. Timing parameters for slave mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{BCy}	BICK cycle time	50	-	-	ns
t_{BCH}	BICK pulse width high	20	-	-	ns
t_{BCL}	BICK pulse width low	20	-	-	ns
t_{LRSU}	LRCKI setup time to BICKI strobing edge	10	-	-	ns
t_{LRH}	LRCKI hold time to BICKI strobing edge	10	-	-	ns
t_{DD}	SDI propagation delay from BICKI active edge	0	-	10	ns

4.2 Serial data formats

Available formats are shown in the following tables.

Table 9. Serial data bit first

Bit	RW	RST	Name	Description
4	RW	0	SAIFB	Determines MSB or LSB first for all SAO formats: 0: MSB first 1: LSB first

Note: Serial input and output formats are specified separately

For example, SAI = 1110 and SAIFB = 1 would specify right-justified 16-bit data, LSB-first.

The table below lists the serial audio input formats supported by the STA311B as related to BICKI = 32 * fs, 48 * fs, 64 * fs, where the sampling rate, fs = 32, 44.1, 48, 88.2, 96, 176.4, 192 kHz.

Table 10. Serial audio input formats according to sampling rate

BICKI	SAI [3:0]	SAIFB	Interface format
32 * fs	1100	X	I²SI²S 15-bit data
	1110	X	Left/right-justified 16-bit data
48 * fs	0100	X	I²S 23-bit data
	0100	X	I²S 20-bit data
	1000	X	I²S 18-bit data
	0100	0	MSB-first I²S 16-bit data
	1100	1	LSB-first I²S 16-bit data
	0001	X	Left-justified 24-bit data
	0101	X	Left-justified 20-bit data
	1001	X	Left-justified 18-bit data
	1101	X	Left-justified 16-bit data
	0010	X	Right-justified 24-bit data
	0110	X	Right-justified 20-bit data
	1010	X	Right-justified 18-bit data
	1110	X	Right-justified 16-bit data

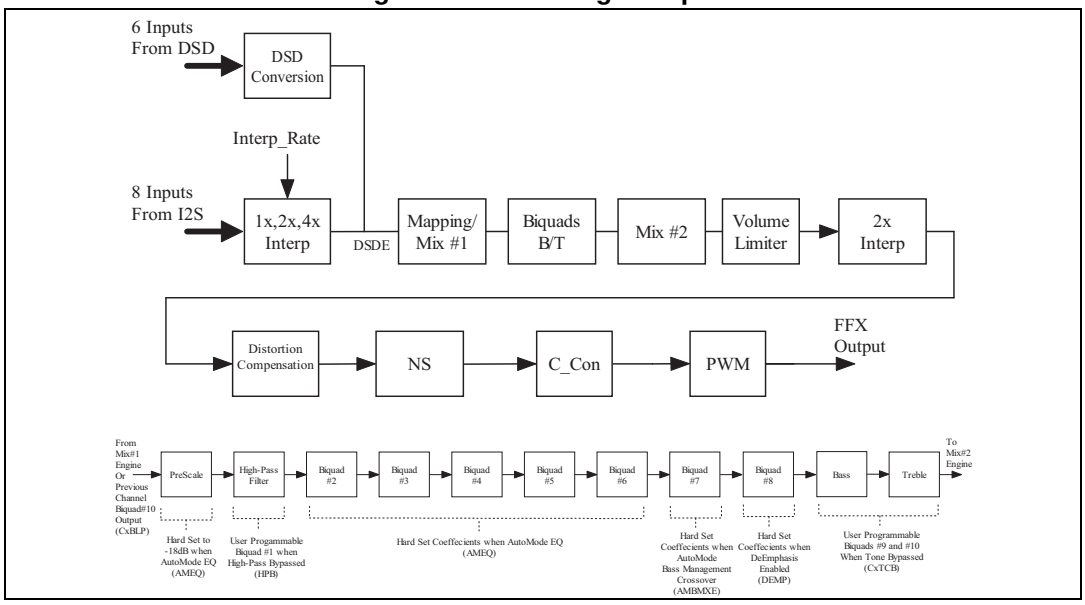
Table 10. Serial audio input formats according to sampling rate (continued)

BICKI	SAI [3:0]	SAIFB	Interface format
64 * fs	0000	X	I²S 24-bit data
	0100	X	I²S 20-bit data
	1000	X	I²S 18-bit data
	0000	0	MSB-first I²S 16-bit data
	1100	1	LSB-first I²S 16-bit data
	0001	X	Left-justified 24-bit data
	0101	X	Left-justified 20-bit data
	1001	X	Left-justified 18-bit data
	1101	X	Left-justified 16-bit data
	0010	X	Right-justified 24-bit data
	0110	X	Right-justified 20-bit data
	1010	X	Right-justified 18-bit data
	1110	X	Right-justified 16-bit data

4.3 Processing data paths

The whole STA311B processing chain is depicted in *Figure 4*. A programmable rate conversion algorithm is applied to the incoming digital audio data (x3,x2,x1,/2) resampling it to the processing rate. A dual-channel plus line out processing is then implemented, with mixing, EQ capability followed by a Volume/DRC block and final DC cut filter. The final oversampling stage and post scaler will provide the output data stream to the PWM modulators. Three different DRC configurations can be used, single-band, dual-band or enhanced dual-band DRC, as shown below.

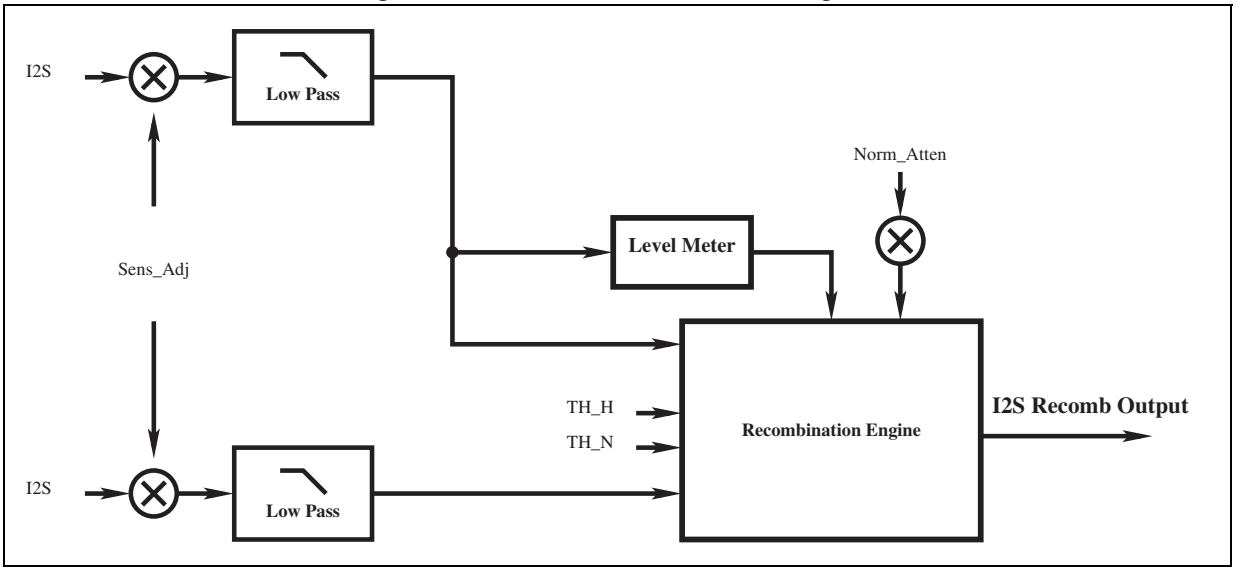
Figure 4. Processing data path



5 I²S recombination interface

The I²S recombination interface shares the same controls for thresholds and gains. However, the low-pass filter is not present and thus the I²S signals coming from the outside should be correctly filtered and conditioned for a correct recombination.

Figure 5. I²S recombination block diagram



6 Startup/shutdown pop noise removal in SE application

Click and pop can generally be defined as undesired audible transients generated by the amplifier system not coming from the system input signal. Such transients can be generated when the amplifier system changes its operating mode: system power-up/power-down, mute/unmute. Every time the PWM starts or stops, if no soft charge method is applied, the result is an audible pop noise.

The STA311B integrates a “pop-elimination” circuitry that removes undesired audible pop noise at the PWM switching start and stop either in single-ended or single-ended virtual ground configurations.

In particular the pop elimination circuit receives as inputs the PWMs generated by the modulator (PWMs_in) and it generates both a delayed version of the PWMs (PWMs_out) and a tristate signal that are sent to the Power stages to attenuate the audible pop at the power up/down.

6.1 PWM start

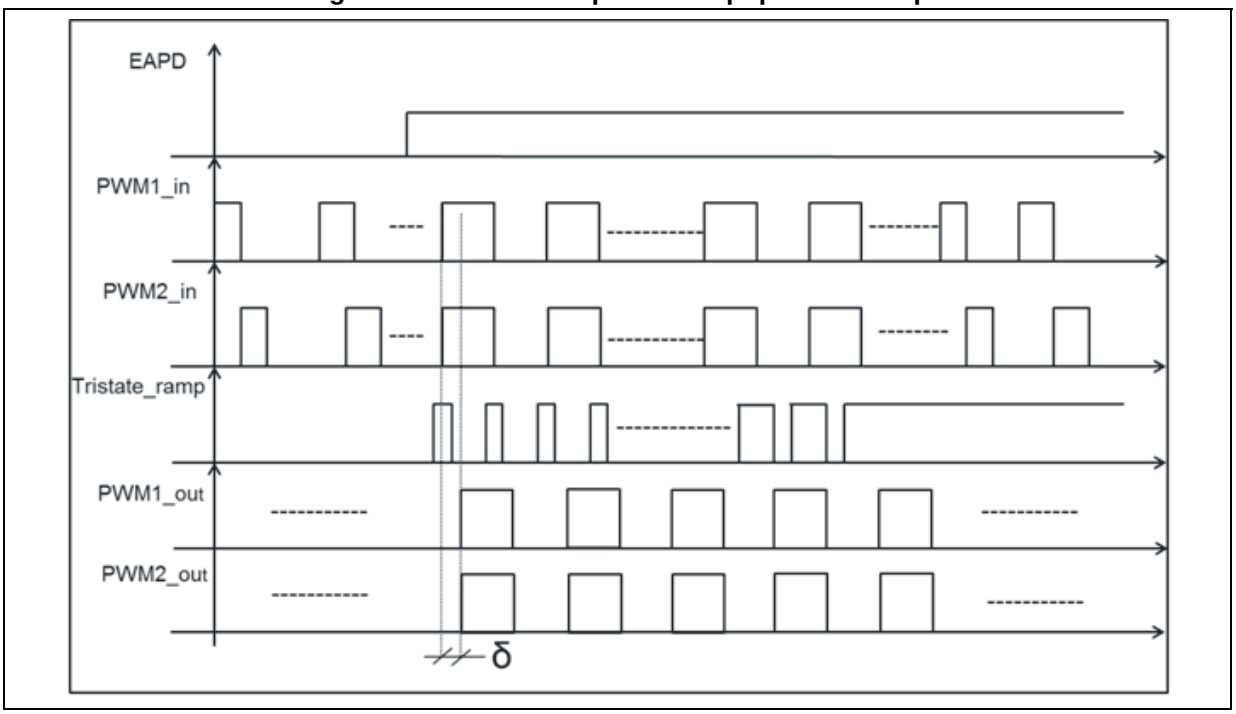
At power-up as soon as the external amplifier power-down (EAPD) is set to one, if at least one channel at the output of the modulator is in binary mode, the pop elimination circuit selects the related PWM input which exhibits the lower PWM timing delay (set using the I²C registers 0x33, 0x34,0x35, 0x36), and it uses it as a PWM reference to synchronize the remaining PWMs_in whose channels are set in binary mode (synchronization phase).

Moreover, during the synchronization phase the modulator is internally muted by setting the audio input signal to

zero. At the end of this phase, all the PWMs_in are synchronous with the PWM reference and they have a duty cycle of 50%.

At each rising edge of the PWM reference, twoTristate_ramp pulses with increasing duty cycle are generated. As depicted in *Figure 10*, where for the sake of simplicity, only two PWMs_in (PWM1_in and PWM2_in) are shown, each pulse is centered with respect to both the rising and falling edges of the PWM reference, and their duty cycle initially set to 21.87% increases gradually and becomes equal to 100% at the end of theTristate_ramp.

Figure 6. Power-on sequence for pop-free startup



Moreover in order to compensate an internal delay between the tristate signal and the PWM present in the Power stage devices, the pop noise removal circuit generates a delayed version of the PWM_in with respect to the Tristate_ramp signal named PWM1_out and PWM2_out in *Figure 6*. The delay value delta between the Tristate_ramp and the PWM_in is programmable using the I²C register 0x80 and the default value is 290 ns.

Finally when the Tristate_ramp duty cycle is equal to 100%, during the de-synchronization phase the PWM time slots, equal for all the PWMs outputs, are changed so that the final channel shift will be the one configured by registers 0x33, 0x34, 0x35 and 0x36. At this point the PWM modulator is automatically un-muted so that the processing outputs can be played.

6.2 PWM stop

When the EAPD signal is set to zero, the modulator is stopped internally, forcing the input audio signal, used to feed the modulator, to zero. After that, the PWM which exhibits the lower PWM timing delay is internally selected and used as a reference. Using the PWM reference, all the PWMs are re-synchronized, and as soon as all PWMs are aligned, at each rising edge of a PWM reference, a reverse tristate_ramp signal is generated. As during startup, the reverse tristate_ramp pulses are centered with respect to the rising and falling edge of the PWM reference, but in this case the starting duty cycle is equal to 100% and gradually becomes equal to zero when the reverse tristate_ramp finishes.

In the STA311B the pop-elimination circuit is activated only when at least one channel is set in binary mode, and the PWMs out speed is set to 384 kHz. In all the other cases the no pop-free PWM switching start/stop procedure is adopted.

7 I²C bus operation

The STA311B supports the I²C protocol via the input ports SCL and SDA_IN (master to slave) and the output port SDA_OUT (slave to master).

This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver.

The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA311B is always a slave device in all of its communications.

7.1 Communication protocol

7.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. An SDA transition while the clock is high is used to identify a START or STOP condition.

7.1.2 Start condition

START is identified by a high-to-low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

7.1.3 Stop condition

STOP is identified by a low-to-high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the STA311B and the bus master.

7.1.4 Data input

During the data input the STA311B samples the SDA signal on the rising edge of clock SCL.

For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

7.2 Device addressing

To start communication between the master and the Omega FFX core, the master must initiate with a start condition. Following this, the master sends 8 bits onto the SDA line (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA311B the I²C interface has two device addresses depending on the SA port configuration, 0x40 or 0100000x when SA = 0, and 0x42 or 0100001x when SA = 1.

The 8^{th} bit (LSB) identifies read or write operation RW, this bit is set to 1 in read mode and 0 for write mode. After a START condition the STA311B identifies on the bus the device address and if a match is found, it acknowledges the identification on SDA bus during the 9^{th}-bit time. The byte following the device identification byte is the internal space address.

7.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA311B acknowledges this and the writes for the byte of internal address.

After receiving the internal byte address the STA311B again responds with an acknowledgement.

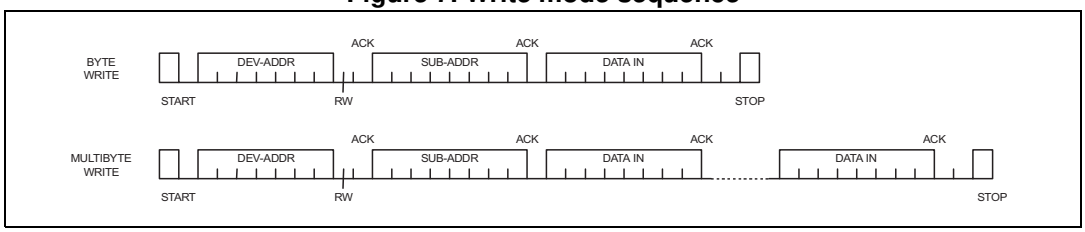
7.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by the Omega FFX core. The master then terminates the transfer by generating a STOP condition.

7.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 7. Write mode sequence



7.4 Read operation

7.4.1 Current address byte read

Following the START condition, the master sends a device select code with the RW bit set to 1. The STA311B acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

7.4.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA311B. The master acknowledges each data byte read and then generates a STOP condition, terminating the transfer.

7.4.3 Random address byte read

Following the START condition, the master sends a device select code with the RW bit set to 0. The STA311B acknowledges this and then the master writes the internal address byte. After receiving the internal byte address, the STA311B again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA311B acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

7.4.4 Random address multi-byte read

The multi-byte read mode can start from any internal address. Sequential data bytes are read from sequential addresses within the STA311B. The master acknowledges each data byte read and then generates a STOP condition, terminating the transfer.

Figure 8. Read mode sequence