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STA321MPL1

Scalable digital microphone processor

Datasheet - production data

TQFP64
10 mm x 10 mm

Features

- 8 digital processing channels each 24-bits
  - 6 channels of PDM input
  - 2 additional virtual channels
- >100 dB SNR and dynamic range
- Digital gain/attenuation 58 dB to -100 dB in 0.5 dB steps
- Soft volume update
- Individual channel and master level control
- Up to 10 independent 32-bit user-programmable biquads (EQ) per channel
- Bass/treble tone control
- Pre- and post-EQ full 8-channel input mix on all 8 channels
- Dual independent limiters/compressors
- Dynamic range compression or anti-clipping modes
- Individual channel and master soft/hard mute
- 3 I²S data outputs
- I²S data output channel mapping function
- Independent channel volume and DSP bypass
- Channel mapping of any input to any processing channel

Applications

- Tablets
- Gaming
- Audio conference sets
- Legacy microphone-equipped devices

Description

The STA321MPL1 is a PDM, high-performance, multichannel processor with ultra-low quiescent current. It is designed for general-purpose digital microphone applications. The device is fully digital and is comprised of three main sections. The first section is the PDM input interface which can accept up to six serial digital inputs. The second section is a high-quality audio processor allowing flexible channel mixing/muxing and provides up to 10 biquads for general sound equalization and voice enhancement with independent volume control. The last block is the I²S output interface which streams out the processed digital audio. The output interface can also be programmed for flexible channel mapping. The device offers some of the most commonly required audio enhancements such as programmable voice tuning and equalization, limiter/compressor for improved voice quality, multiband selection for customizable microphone usage, and configurable wind-noise rejection. The embedded digital processor allows the microphone processing to be offloaded from the main CPU or SoC to the device.

The STA321MPL1 has six digital microphone inputs, providing connections for up to three dual-membrane microphones.

Table 1. Device summary

Order code	Package	Packaging
STA321MPL1TR	TQFP64	Tape and reel

Contents

1 Device overview

1.1 Block diagram

Figure 1. Block diagram

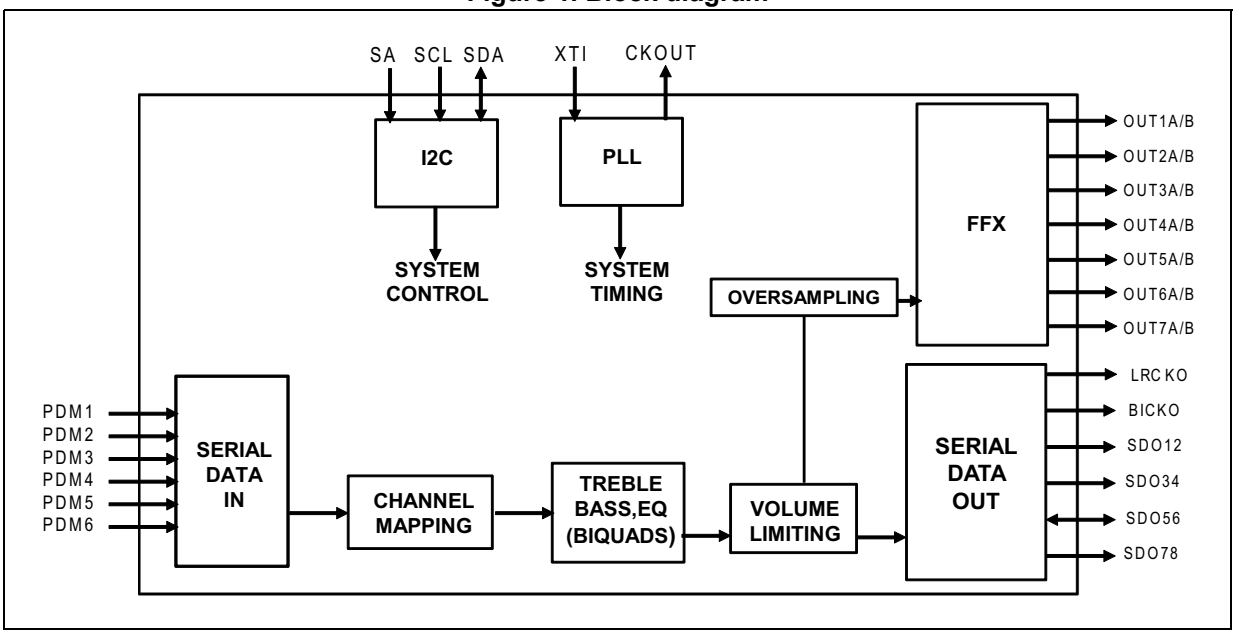
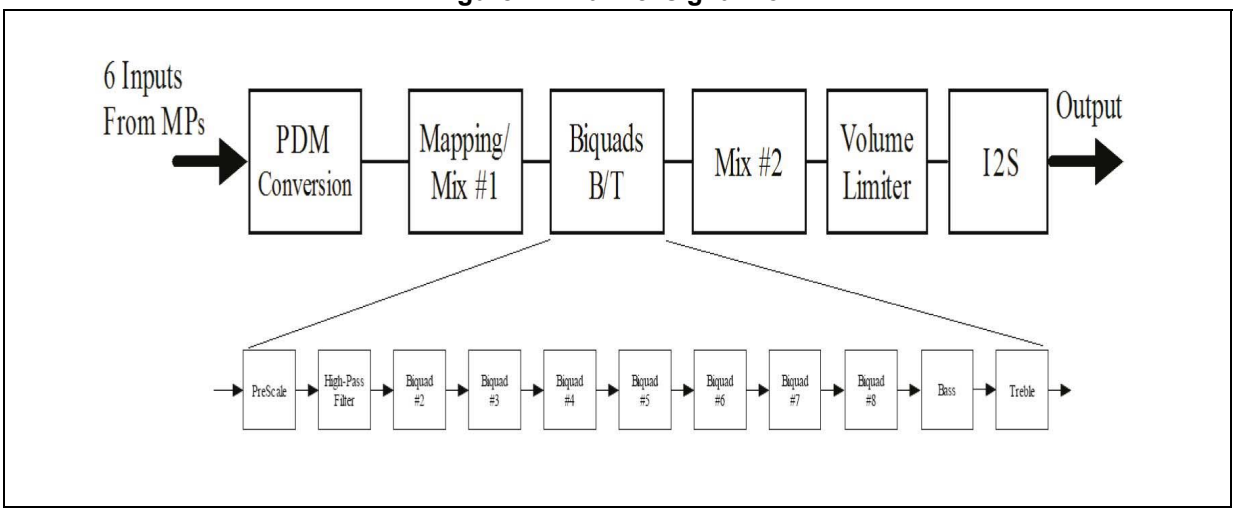


Figure 2. Channel signal flow



1.2 Pin description

Figure 3. Pin connections (top view)

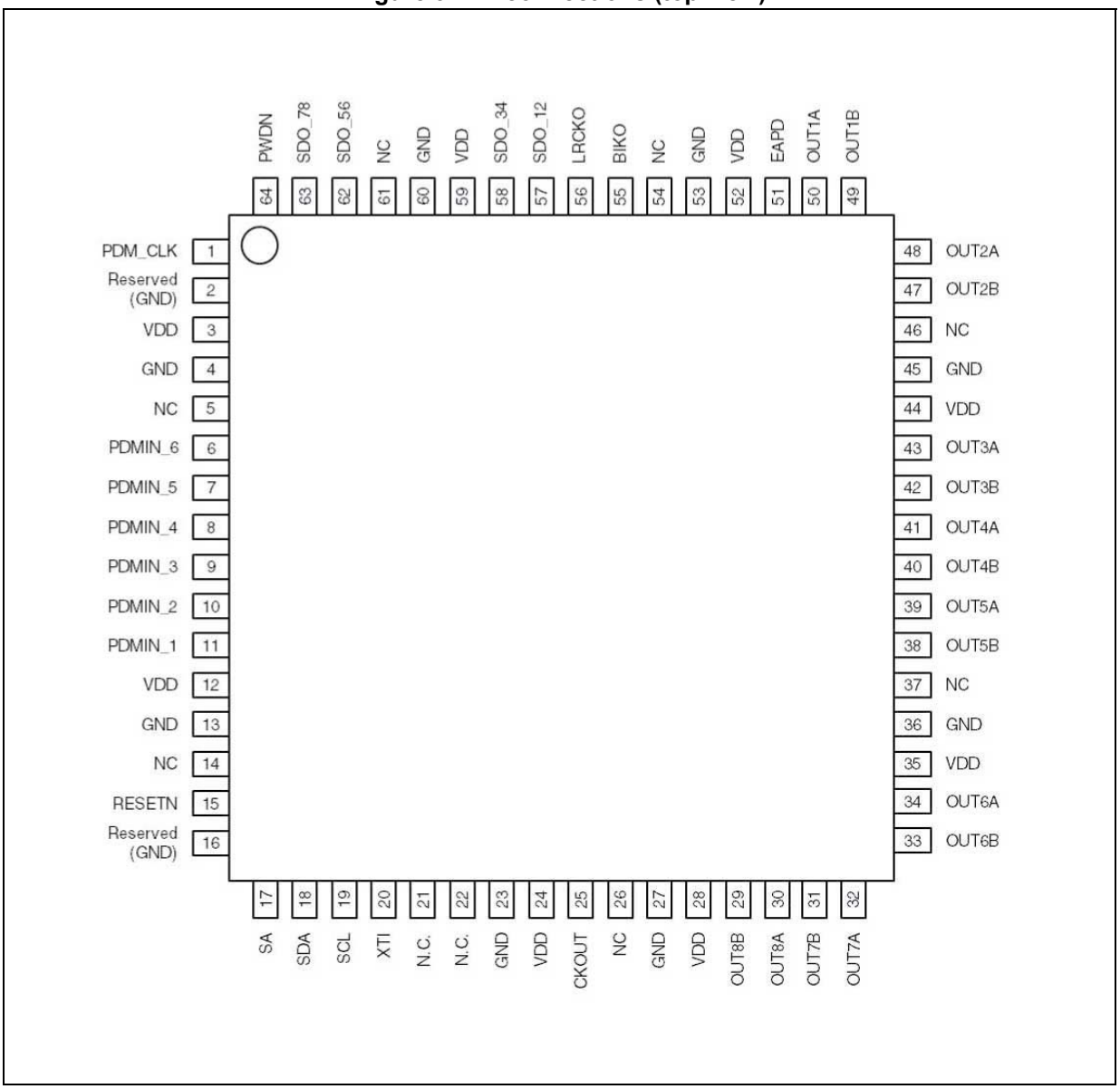


Table 2. Pin description

Pin number	Type	Name	Description
1	5-V tolerant TTL input buffer	PDM_CLK	PDM I/F CLK
6		PDMIN_6	PDM input channel 6
7		PDMIN_5	PDM input channel 5
8		PDMIN_4	PDM input channel 4
9		PDMIN_3	PDM input channel 3
10		PDMIN_2	PDM input channel 2
11		PDMIN_1	PDM input channel 1
15	5-V tolerant TTL Schmitt trigger input buffer	RESETN	Global reset
16	CMOS input buffer with pull-down	PLLB	Bypass phase-locked loop
17	1.8-V CMOS input buffer with pull-down	SA	Select address (I^2C)
18	Bidirectional buffer: 5-V tolerant TTL Schmitt trigger input; 3.3-V capable 2 mA slew-rate controlled output	SDA	Serial data (I^2C)
19	5-V tolerant TTL Schmitt trigger input buffer	SCL	Serial clock (I^2C)
20		XTI	Crystal oscillator input (clock input)
21		NC	Not connected
23	Analog ground	GND	PLL ground
25	3.3-V capable TTL tristate 4 mA output buffer	CKOUT	Clock output
29	3.3-V capable TTL 2 mA output buffer	OUT8B	PWM channel 8 output B
30		OUT8A	PWM channel 8 output A
31		OUT7B	PWM channel 7 output B
32		OUT7A	PWM channel 7 output A
33		OUT6B	PWM channel 6 output B
34		OUT6A	PWM channel 6 output A
38		OUT5B	PWM channel 5 output B
39		OUT5A	PWM channel 5 output A
40		OUT4B	PWM channel 4 output B
41		OUT4A	PWM channel 4 output A
42		OUT3B	PWM channel 3 output B
43		OUT3A	PWM channel 3 output A
47		OUT2B	PWM channel 2 output B
48		OUT2A	PWM channel 2 output A
49		OUT1B	PWM channel 1 output B
50		OUT1A	PWM channel 1 output A
51	3.3-V capable TTL 4 mA output buffer	EAPD	Ext. amp power-down

Table 2. Pin description (continued)

Pin number	Type	Name	Description
55	3.3-V capable TTL 2 mA output buffer	BICKO	Output serial clock
56		LRCKO	Output left/right clock
57		SDO_12	Output serial data channels 1 and 2
58		SDO_34	Output serial data channels 3 and 4
62		SDO_56	Output serial data channels 5 and 6
63		SDO_78	Output serial data channels 7 and 8
64	5-V tolerant TTL Schmitt trigger input buffer	PWDN	Device power-down
3, 12, 24, 28, 35, 44, 52, 59	3.3-V digital supply voltage	VDD	3.3-V supply
2, 4, 13, 27, 36, 45, 53, 60	Digital ground	GND	Ground
14, 21, 22, 26, 37, 46, 54, 61		NC	Not connected

2 Electrical characteristics

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	3.3-V I/O power supply	-0.5	—	4	V
V_{SA}	Voltage on SA pin (17)	-0.5		2	
V_i	Voltage on input pins	-0.5		VDD + 0.5	
V_o	Voltage on output pins	-0.5		VDD + 0.3	
T_{stg}	Storage temperature	-40		150	°C
T_{amb}	Ambient operating temperature	-40		90	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{thj\text{-}amb}$	Thermal resistance, junction-to-ambient	—	85	—	°C/W

2.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	I/O power supply	3.0	3.3	3.6	V
V_{SA}	Voltage on SA pin (17)	1.55	1.8	1.95	
T_j	Operating junction temperature	-40	25	125	°C

2.4 Electrical specifications

The following specifications are valid for V_{DD} = 3.3 V ± 0.3 V, V_{SA} = 0 V and T_{amb} = 25 °C, unless otherwise stated.

Table 6. General interface electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Low-level input, no pull-up	V_i = 0 V		—	1	µA
I_{ih}	High-level input, no pull-down	$V_i = V_{DD}$			2	
I_{OZ}	Tristate output leakage without pull-up/down	$V_i = V_{DD}$			2	
V_{esd}	Electrostatic protection, human body model	Leakage < 1 µA	2000			V

Table 7. DC electrical characteristics: 3.3-V buffers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			
V_{ILhyst}	Low-level threshold	Input falling	0.8		1.35	
V_{IHhyst}	High-level threshold	Input rising	1.3		2.0	
V_{hyst}	Schmitt trigger hysteresis		0.3		0.8	
V_{ol}	Low-level output	I_{ol} = 100 µA			0.2	
V_{oh}	High-level output	I_{oh} = -100 µA	VDD-0.2			
		I_{oh} = -2 mA	2.4			
Idd	Quiescent current	Reset conditions		15		mA
		Normal conditions with CKOUT		60		

3 Microphone interface

3.1 PDM clock generator (for microphones)

To correctly start the device in microphone processor mode, it is necessary to set registers 0x00 to 0x9B and register 0x5D to 0x01.

The CKOUT pin can be used to properly provide a clock source for digital microphones.

When the mikemode bit is asserted (reg 0x5D bit 0), the CKOUT generator is automatically configured to generate a clock with sys_clk/32 frequency (corresponding to a PDM over-sampling rate of 64).

For example, considering a base sample frequency of:

Fs = 44.1 kHz

XTI = 11.289 MHz (user provided)

System clock = 90.3168 MHz (system generated)

Clock out = 2.8224 MHz (system generated)

Fs = 48.0 kHz

XTI = 12.288 MHz (user provided)

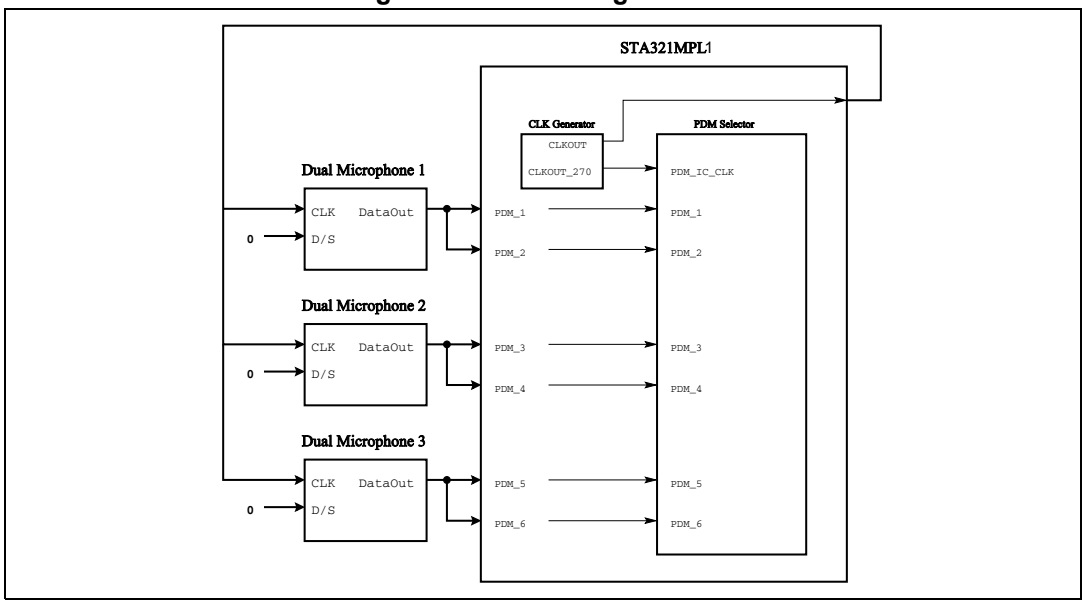
System clock= 98.304 MHz (system generated)

Clock out = 3.072 MHz (system generated)

Technical details

The clock generator creates two output clocks with the same frequency, CKOUT270 has a 270 degrees phase shift with respect to CKOUT. One is exported outside the device and used to clock the microphones, the other is used internally to clock the PDM interface of the STA321MPL1.

Figure 4. PDM clock generator



3.2 PDM resampling interface

The PDM resampling interface is used to properly sample external data.

It can work in three different modes: compatibility mode, dual-membrane mode and advanced mode. In each mode, data are sampled at the rising or falling edge.

Table 8. Modes for PDM resampling interface

Mode	Behavior
00	Compatibility (old)
01	Reserved
10	Dual-membrane
11	Advanced

Compatibility mode

In this mode every channel is sampled at the rising edge.

Dual-membrane mode

The dual-membrane mode is a particular configuration (automatically applied when the proper bit is asserted) which permits the use of the dual-membrane microphone. In particular, it has 2 PDM data channels (normal and high) muxed in a single wire. The normal channel is sampled at the falling edge, while the high channel is sampled at the rising edge.

Advanced mode

In this mode every channel can be sampled at the rising or falling edge according to the configuration register.

3.3 PDM recombination (dual-membrane microphone support)

Dual microphone scenario:

A dual-membrane microphone has two separate PDM signal paths:

- Normal channel for moderate SPL (sound pressure level) acoustic signals
- High channel for high SPL acoustic signals

The sensitivity of the high channel is configurable and is set by default to 20 dBSPL lower than the sensitivity of the normal channel to avoid saturation in any part of the signal path.

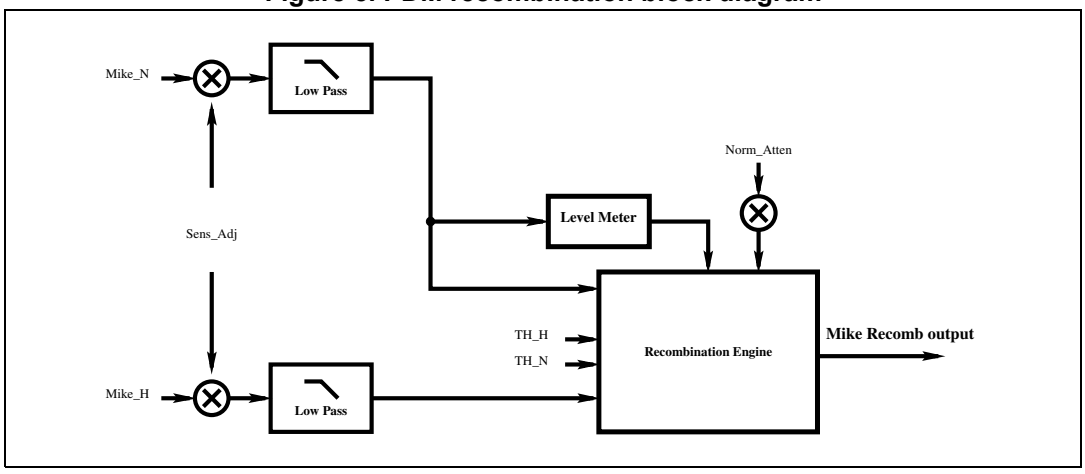
The two channels can be combined together to enlarge the dynamic range and have a good trade-off between the DNR and the noise floor (which is lower in the case of the normal channel).

The main functionality is based on a signal level measurement and a dual-threshold system.

If the signal of the normal channel is:

- above the upper threshold (TH_H), the output is taken from the high channel
- under the lower threshold (TH_N), the output is taken from the normal channel
- between TH_H and TH_N, the output is a combination of the high and normal channels.

Figure 5. PDM recombination block diagram



3.4 Low-pass filter

A filter is provided (and needed) to suppress the noise outside the audio band that may be still present before the recombination stage.

The filter is a 2nd order IIR (infinite impulse response) low-pass with a cutoff frequency of 20 kHz. It can be bypassed through the I^2C bit.

Configuration registers: 0x62(6), 0x63(6), 0x64(6)

3.5 Sensitivity adjustment

The sensitivity adjustment control can be used to compensate the differences between theoretical and real sensitivity. It is applied to all membranes of the microphone.

Sensitivity adjustment = [-4, 3.875) with a 0.125 dB step

Configuration registers: 0x5F(5-0), 0x60(5-0), 0x61(5-0)

3.6 Normal channel attenuation

The NORM_Att is a parameter which must be set to the sensitivity difference between the High SPL channel and the Normal SPL channel. By default its value is set to 20 dB.

Configuration registers: 0x52(5-0), 0x63(5-0), 0x64(5-0)

3.7 Thresholds

Two thresholds can be configured to control/select the recombination engine behavior. In particular, they can be used to give more weight (in the final output) to the Normal Channel or to the High Channel which leads to choosing between having lower distortion (High Channel) or lower noise floor (Normal Channel).

Configuration registers: 0x65(5-0), 0x66(5-0), 0x67(5-0), 0x68(5-0), 0x69(5-0), 0x6A(5-0)

4 I²C bus operation

The STA321MPL1 supports the I²C protocol via the input ports SCL and SDA_IN (master to slave) and the output port SDA_OUT (slave to master).

This protocol defines any device that sends data to the bus as a transmitter and any device that reads data as a receiver.

The device that controls the data transfer is known as the master and the other is the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA321MPL1 is a slave device in all of its communications.

4.1 Communication protocol

4.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. An SDA transition while the clock is high is used to identify a START or STOP condition.

4.1.2 Start condition

START is identified by a high-to-low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

4.1.3 Stop condition

STOP is identified by a low-to-high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the STA321MPL1 and the bus master.

4.1.4 Data input

During data input, the STA321MPL1 samples the SDA signal on the rising edge of the clock SCL.

For correct device operation the SDA signal must be stable during the rising edge of the clock. The data can change only when the SCL line is low.

4.2 Device addressing

To start communication between the master and the Omega FFX core, the master must initiate with a start condition. Following this, the master sends 8 bits onto the SDA line (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA321MPL1 the I²C interface has two device addresses depending on the SA port configuration, 0x40 or 0100000x when SA = 0, and 0x42 or 0100001x when SA = 1.

The 8th bit (LSB) identifies a read or write operation RW. This bit is set to 1 in read mode and 0 for write mode. After a START condition, the STA321MPL1 identifies the device address on the bus and if a match is found, it acknowledges the identification on the SDA bus during the 9th-bit time. The byte following the device identification byte is the internal space address.

4.3 Write operation

Following a START condition, the master sends a device select code with the RW bit set to 0. The STA321MPL1 acknowledges this and the writes for the byte of the internal address.

After receiving the internal byte address, the STA321MPL1 responds again with an acknowledgement.

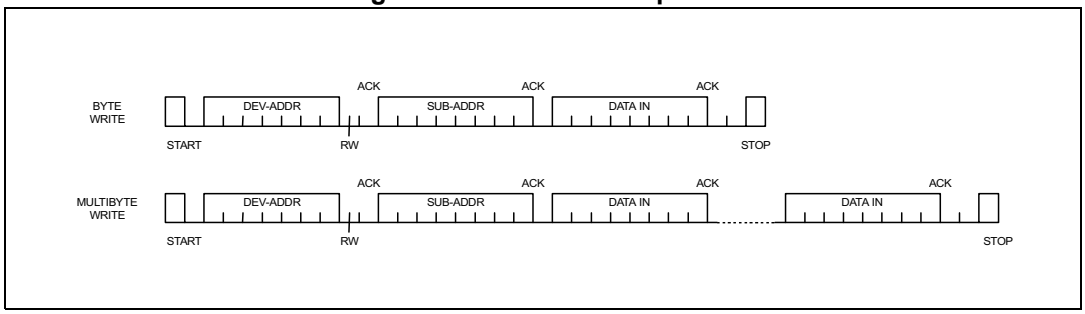
4.3.1 Byte write

In byte write mode, the master sends one data byte, this is acknowledged by the Omega FFX core. The master then terminates the transfer by generating a STOP condition.

4.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 6. Write mode sequence



4.4 Read operation

4.4.1 Current address byte read

Following the START condition, the master sends a device select code with the RW bit set to 1. The STA321MPL1 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

4.4.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA321MPL1. The master acknowledges each data byte read and then generates a STOP condition, terminating the transfer.

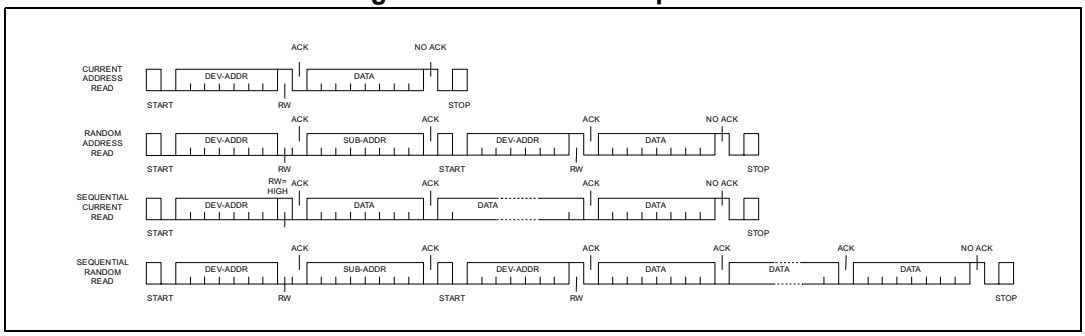
4.4.3 Random address byte read

Following the START condition, the master sends a device select code with the RW bit set to 0. The STA321MPL1 acknowledges this and then the master writes the internal address byte. After receiving the internal byte address, the STA321MPL1 again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA321MPL1 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

4.4.4 Random address multi-byte read

The multi-byte read mode can start from any internal address. Sequential data bytes are read from sequential addresses within the STA321MPL1. The master acknowledges each data byte read and then generates a STOP condition, terminating the transfer.

Figure 7. Read mode sequence



5 Registers

5.1 Register summary

Table 9. Register summary

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
Configuration									
0x00	CONFA	COS1	COS0	DSPB	IR1	IR0	MCS2	MCS1	MCS0
0x01									
0x02	ConfC			SAOD4	SAOFB	SAO3	SAO2	SAO1	SAO0
0x03	ConfD	MPC	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x04	ConfE	C8BO	C7BO	C6BO	C5BO	C4BO	C3BO	C2BO	C1BO
0x05	ConfF	PWMS2	PWMS1	PWMS0	BQL	PSL	DEMP	DRC	HPB
0x06	ConfG	MPCV	DCCV	HPE	AM2E	AME	COD	SID	PWMD
0x07	ConfH	ECLE	LDTE	BCLE	IDE	ZDE	SVE	ZCE	NSBW
0x08	ConfI	EAPD							PSCE
Volume control									
0x09	MMUTE								MMUTE
0x0A	Mvol	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x0B	C1Vol	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x0C	C2Vol	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0D	C3Vol	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0x0E	C4Vol	C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
0x0F	C5Vol	C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
0x10	C6Vol	C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
0x11	C7Vol	C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
0x12	C8Vol	C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
0x13	C1VTMB	C1M	C1VBP		C1VT4	C1VT3	C1VT2	C1VT1	C1VT0
0x14	C2VTMB	C2M	C2VBP		C2VT4	C2VT3	C2VT2	C2VT1	C2VT0
0x15	C3VTMB	C3M	C3VBP		C3VT4	C3VT3	C3VT2	C3VT1	C3VT0
0x16	C4VTMB	C4M	C4VBP		C4VT4	C4VT3	C4VT2	C4VT1	C4VT0
0x17	C5VTMB	C5M	C5VBP		C5VT4	C5VT3	C5VT2	C5VT1	C5VT0
0x18	C6VTMB	C6M	C6VBP		C6VT4	C6VT3	C6VT2	C6VT1	C6VT0
0x19	C7VTMB	C7M	C7VBP		C7VT4	C7VT3	C7VT2	C7VT1	C7VT0
0x1A	C8VTMB	C8M	C8VBP		C8VT4	C8VT3	C8VT2	C8VT1	C8VT0

Table 9. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
Input mapping									
0x1B	C12im		C2IM2	C2IM1	C2IM0		C1IM2	C1IM1	C1IM0
0x1C	C34im		C4IM2	C4IM1	C4IM0		C3IM2	C3IM1	C3IM0
0x1D	C56im		C6IM2	C6IM1	C6IM0		C5IM2	C5IM1	C5IM0
0x1E	C78im		C8IM2	C8IM1	C8IM0		C7IM2	C7IM1	C7IM0
Processing loop									
0x28	BQlp	C8BLP	C7BLP	C6BLP	C5BLP	C4BLP	C3BLP	C2BLP	C1BLP
0x29	MXlp	C8MXLP	C7MXLP	C6MXLP	C5MXLP	C4MXLP	C3MXLP	C2MXLP	C1MXLP
Processing bypass									
0x2A	EQbp	C8EQBP	C7EQBP	C6EQBP	C5EQB	C4EQBP	C3EQBP	C2EQBP	C1EQBP
0x2B	ToneBP	C8TCB	C7TCB	C6TCB	C5TCB	C4TCB	C3TCB	C2TCB	C1TCB
Tone control									
0x2C	Tone	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
Dynamics control									
0x2D	C1234ls	C4LS1	C4LS0	C3LS1	C3LS0	C2LS1	C2LS0	C1LS1	C1LS0
0x2E	C5678ls	C8LS1	C8LS0	C7LS1	C7LS0	C6LS1	C6LS0	C5LS1	C5LS0
0x2F	L1ar	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x30	L1atrt	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0x31	L2ar	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0x32	L2atrt	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
PWM output timing									
0x33	C12ot		C2OT2	C2OT1	C2OT0		C1OT2	C1OT1	C1OT0
0x34	C34ot		C4OT2	C4OT1	C4OT0		C3OT2	C3OT1	C3OT0
0x35	C56ot		C6OT2	C6OT1	C6OT0		C5OT2	C5OT1	C5OT0
0x36	C78ot		C8OT2	C8OT1	C8OT0		C7OT2	C7OT1	C7OT0
I²S output channel mapping									
0x37	C12om		C2OM2	C2OM1	C2OM0		C1OM2	C1OM1	C1OM0
0x38	C34om		C4OM2	C4OM1	C4OM0		C3OM2	C3OM1	C3OM0
0x39	C56om		C6OM2	C6OM1	C6OM0		C5OM2	C5OM1	C5OM0
0x3A	C78om		C8OM2	C8OM1	C8OM0		C7OM2	C7OM1	C7OM0

Table 9. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
User-defined coefficient RAM									
0x3B	Cfaddr1							CFA9	CFA8
0x3C	Cfaddr2	CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0x3D	B1cf1	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0x3E	B1cf2	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0x3F	B1cf3	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0x40	B2cf1	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0x41	B2cf2	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0x42	B2cf3	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0x43	A1cf1	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
0x44	A1cf2	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0x45	A1cf3	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0x46	A2cf1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0x47	A2cf2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0x48	A2cf3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0x49	B0cf1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0x4A	B0cf2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0x4B	B0cf3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0x4C	Cfud							WA	W1
0x4D	MPCC1	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x4E	MPCC2	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x4F	DCC1	DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
0x50	DCC2	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0x51	PSC1	RCV11	RCV10	RCV9	RCV8	RCV7	RCV6	RCV5	RCV4
0x52	PSC2	RCV3	RCV2	RCV1	RCV0	CNV11	CNV10	CNV9	CNV8
0x53	PSC3	CNV7	CNV6	CNV5	CNV4	CNV3	CNV2	CNV1	CNV0
BIST									
0x57	BACT	R8BACT	R7BACT	R6BACT	R5BACT	R4BACT	R3BACT	R2BACT	R1BCAT
0x58	BEND	R8BEND	R7BEND	R6BEND	R5BEND	R4BEND	R3BEND	R2BEND	R1BEND
0x59	BBAD	R8BBAD	R7BBAD	R6BBAD	R5BBAD	R4BBAD	R3BBAD	R2BBAD	R1BBAD
0x5A	L12new								NLENAR
0x5B	FineVol	CFINE8	CFINE7	CFINE6	CFINE5	CFINE4	CFINE3	CFINE2	CFINE1

Table 9. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
PDM and recombination IP interface									
0x5C	MRBist	MHFail	MHBad	MHEnd	MHAct	MNFail	MNBad	MNEnd	MNAct
0x5D	RCTR1	Boost6db			I²S_byp	I²S_en	mike_en	mike_byp	m_mode
0x5E	PDMCT	AdvM6	AdvM5	AdvM4	AdvM3	AdvM2	AdvM1	PDMSM[1:0]	
0x5F	RCTR2		bypRM1	CH1GG[5:0]					
0x60	RCTR3		bypRM2	CH2GG[5:0]					
0x61	RCTR4		bypRM3	CH3GG[5:0]					
0x62	RCTR5		LP1en	CH1NCA[5:0]					
0x63	RCTR6		LP2en	CH2NCA[5:0]					
0x64	RCTR7		LP3en	CH3NCA[5:0]					
0x65	RCTR8			CH1TH_N[5:0]					
0x66	RCTR9			CH2TH_N[5:0]					
0x67	RCTR10			CH3TH_N[5:0]					
0x68	RCTR11			CH1TH_H[5:0]					
0x69	RCTR12			CH2TH_H[5:0]					
0x6A	RCTR13			CH3TH_H[5:0]					
Clock manager configuration/status registers									
0x71	pllfrac1	PLFI15	PLFI14	PLFI13	PLFI12	PLFI11	PLFI10	PLFI9	PLFI8
0x72	pllfrac0	PLFI7	PLFI6	PLFI5	PLFI4	PLFI3	PLFI2	PLFI1	PLFI0
0x73	pll div	PLLDD1	PLLDD0	PLLND5	PLLND4	PLLND3	PLLND2	PLLND1	PLLND0
0x74	pll conf0	PDPDC	PLLFC	PLSTRB	PLSTBB	PLIFD3	PLIFD2	PLIFD1	PLIFD0
0x75	pll conf1					PLLBYP	PLLDPR	LOWEN	BST32K
0x76	pll stat					PLLBYS	PLLPDS	OSCOK	LOWCKS
Biquad configuration									
0x77	CBQ1	EBQ3_1	EBQ3_0	EBQ2_1	EBQ2_0	EBQ1_1	EBQ1_0	EBQ0_0	EBQ0_0
0x78	CBQ2	EBQ7_1	EBQ7_0	EBQ6_1	EBQ6_0	EBQ5_1	EBQ5_0	EBQ4_0	EBQ4_0
0x79	CBQ3				nshen	EBQ9_1	EBQ9_0	EBQ8_0	EBQ8_0
RMS status registers									
0x7A	rmsZMH	RZM15	RZM14	RZM13	RZM12	RZM11	RZM10	RZM9	RZM8
0X7B	rmsZML	RZM7	RZM6	RZM5	RZM4	RZM3	RZM2	RZM1	RZM0
0X7C	rmsPOH	RPO15	RPO14	RPO13	RPO12	RPO11	RPO10	RPO9	RPO8
0X7D	rmsPOL	RPO7	RPO6	RPO5	RPO4	RPO3	RPO2	RPO1	RPO0
Tristate startup/shutdown pop removal signals									
0x80	DPT				DPT4	DPT3	DPT2	DPT1	DPT0
0x81	CFR129	RL3	RL2	RL1	RL0	RD	SID1	FBYP	RTP
0x82	TSDLY1	UDDT15	UDDT14	UDDT13	UDDT12	UDDT11	UDDT10	UDDT9	UDDT8
0x83	TSDLY2	UDDT7	UDDT6	UDDT5	UDDT4	UDDT3	UDDT2	UDDT1	UDDT0

5.2 Register description

5.2.1 Configuration register A (0x00)

D7	D6	D5	D4	D3	D2	D1	D0
COS1	COS0	DSPB	IR1	IR0	MCS2	MCS1	MCS0
1	0	0	1	1	0	1	1

Bit	RW	RST	Name	Description
0	RW	1	MCS0	Master clock select: selects the ratio between the input sampling frequency (PDM I/FCLK)and the input clock (XTI).
1	RW	1	MCS1	
2	RW	0	MCS2	

- The internal clock depends on the external clock frequency provided to the XTI pin. The internal clock can be either 90.3168 MHz or 98.304 MHz. In the case of the XTI, it is respectively 11.2896MHz or 12.288MHz.
- The relationship between the input clock XTI and the PDM interface clock is determined by both the MCSn and the IRn (input rate) register bits. IR[1,0] = 11 sets the PDM interface enable and MCS[2:0] = 011 means XTI = 4*PDM interface clock.

If XTI input is not used, the related pin must be tied to GND.

Input sampling rate *fs* (kHz)	IR	MCS[2:0]				
		1xx	011	010	001	000
XTI	11	2*PDM_CK	4*PDM_CK	6*PDM_CK	8*PDM_CK	12*PDM_CK

Interpolation ratio select

Bit	RW	RST	Name	Description
0	RW	0	DSPB	DSP bypass bit: 0: normal operation 1: bypass of biquad and bass/treble functions

Setting the DSPB bit bypasses the biquad function of the FFX core.

COS [1,0]	CKOUT frequency
00	PLL output
01	PLL output / 4
10	PLL output / 8
11	PLL output / 16

cos [1,0] sets the clock out value. Clock out frequency is a ratio of the internal clock and the ratio depends on the cos[1,0] setting.

Example cos[1,0] = 10:

XTI = 12.288

PLL output = 98.304 MHz

CK_out = 98.304/8 = 12.288

Clock out is automatically configured to obtain a frequency of 64 Fs (sys_clock/32) if the bit0 of the register 0x5D is asserted. This generates a valid clock to be provided to a digital (PDM) microphone.