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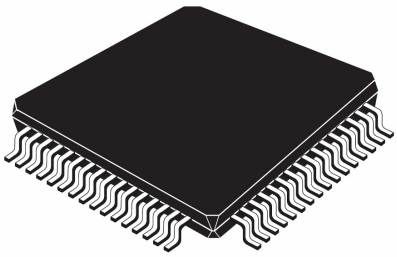
STA321

4-channel digital audio system with FFX™ driver

Features

- High efficiency FFX™ class-D modulator
- 100-dB dynamic range
- Two stereo channels with I^2S input/output data interface
- 16-bit stereo ADC input with PGA and microphone biasing
- Analog and digital muxing/mixing capability
- 4-channel input sample rate converter (8 kHz to 192 kHz)
- Four channels of 24-bit audio processing
- Flexible channel mapping and routing
- Output configurations:
  - 2.0
  - 2.1
  - 4.0
  - Mono
- Embedded CMOS bridge: up to 0.5 W/channel
- pfStart™ for pop-free single-ended operations
- Play and record simultaneous operation
- Pre and post mix stages
- Individual channel and master gain/attenuation



LQFP-64 package
with exposed pad down (EPD)

- Digital gain/attenuation -105 dB to +36 dB in 0.5-dB steps
- Soft volume update and muting
- DC-blocking selectable high-pass filter
- Selectable de-emphasis filter
- Up to 13 28-bit user programmable biquads (EQ) per channel
- Bass/treble tone control
- Ternary, binary or phase shift modulation
- PWM output
- Headphone output with jack detector
- I^2C control.

Table 1. Device summary

Order code	Temperature range	Package	Packaging
STA321	0 to 70 °C	LQFP-64 EPD	Tray
STA321TR	0 to 70 °C	LQFP-64 EPD	Tape and reel

Contents

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1 Overview

The STA321 is a single chip solution for digital audio processing applications of up to 4.0 channels.

The STA321 is part of the Sound Terminal™ family that together with the digital power stage provides full digital audio streaming to the speaker, offering cost effectiveness, low energy dissipation and sound enrichment.

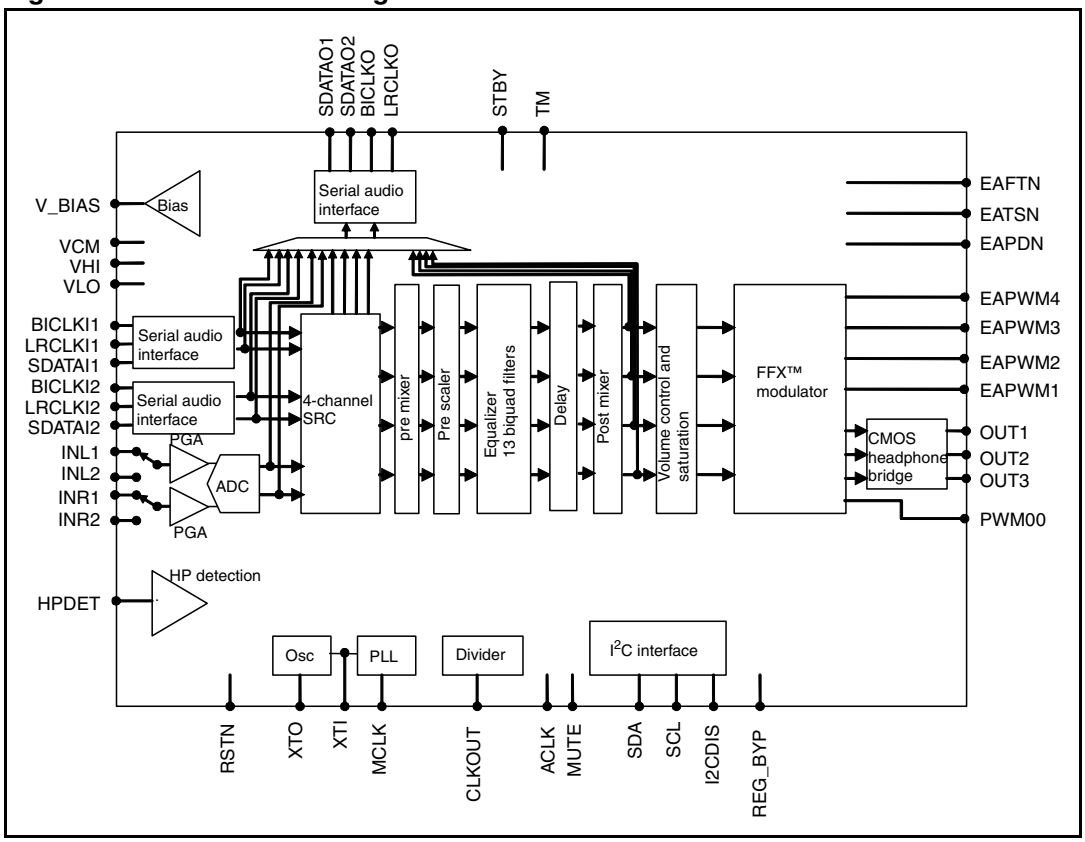
The STA321 input section consists of two multiplexed stereo analog inputs, a 16-bit ADC and two independent digital input interfaces. The serial audio data input interface accepts all possible formats, including the popular I^2S format. There is also a digital output interface fed by the ADC or by the digitally processed signals.

The device has a full assortment of digital processing features. This includes sample rate converter, pre and post mixing, up to 13 programmable 28-bit biquads (EQ) per channel, bass/treble tone control and DRC. The embedded headphone detector indicates when headphone jack is inserted.

The STA321 provides four independent channels of FFX™ output capabilities. In conjunction with a power device, it provides high-quality, high-efficiency, all digital amplification.

The embedded CMOS bridge supplies up to 0.5 W into an 8-Ω load and 70 mW into a 16-Ω load for the headphones output.

Figure 1. STA321 block diagram



2 Pin description

Figure 2. Pin out

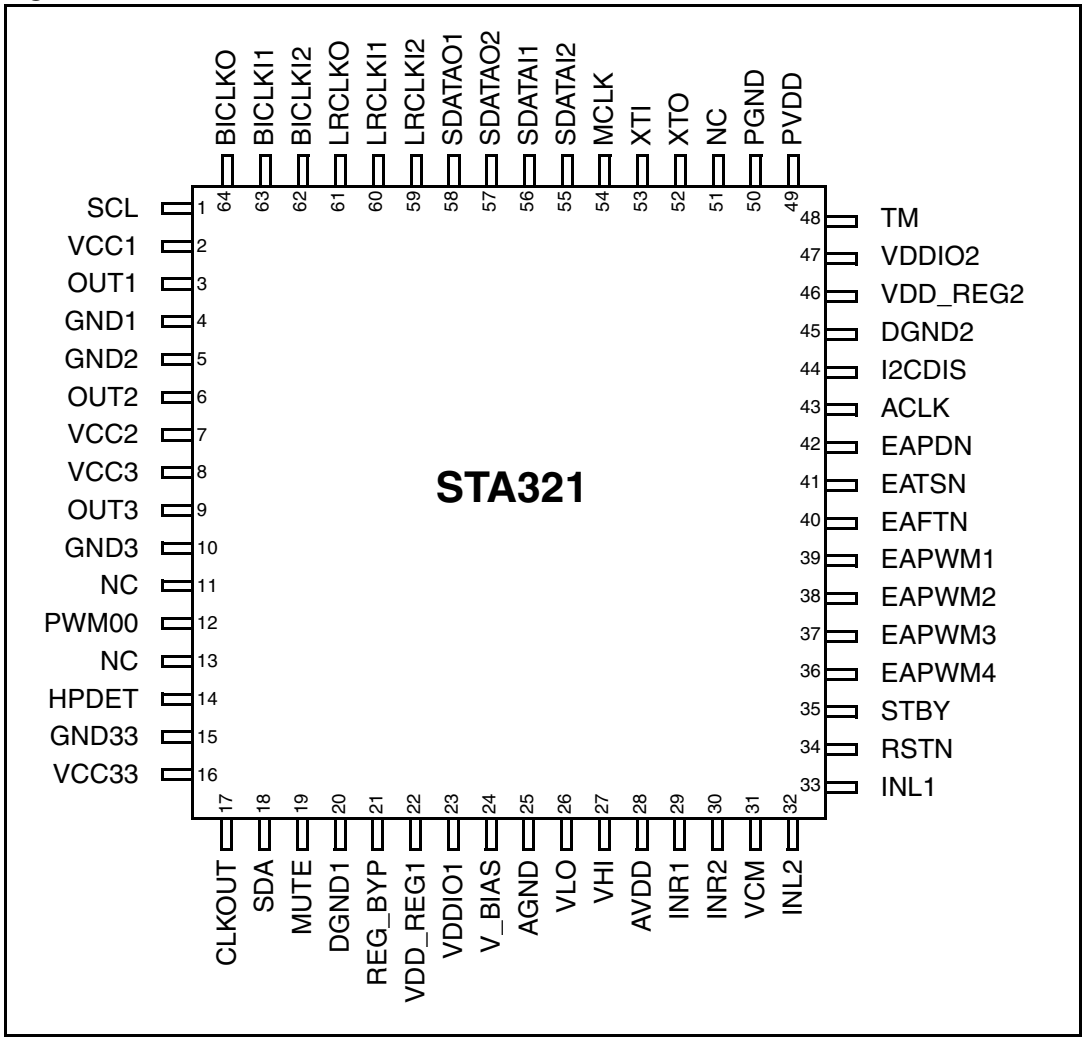


Table 2. Pin list

Pin	Pull	Name	Type	Description
1	-	SCL	In (digital), schmitt tr	I^2C serial clock, schmitt trigger input
3	-	OUT1	Out (analog)	HP/line-out PWM 1
6	-	OUT2	Out (analog)	HP/line-out PWM 2
9	-	OUT3	Out (analog)	HP/line-out PWM 3
11	-	NC	-	Not connected
12	-	PWM00	Out (digital)	Auxiliary PWM
13	-	NC	-	Not connected
14	-	HPDET	In (analog)	Headphone detection

Table 2. Pin list (continued)

Pin	Pull	Name	Type	Description
17	-	CLKOUT	Out (digital)	Buffered clock output
18	-	SDA	In/Out (digital)	I^2C serial data
19	H	MUTE	In (digital)	Mute (active high)
21	-	REG_BYPASS	In (analog)	DC regulator bypass: 0: normal operation, regulator enabled 1: regulator bypassed
24	-	BIAS	In/Out (analog)	ADC microphone bias voltage
26	-	VLO	In (analog)	ADC low reference voltage
27	-	VHI	In (analog)	ADC high reference voltage
29	-	INR1	In/Out (analog)	ADC right channel line input1
30	-	INR2	In/Out (analog)	ADC right channel line input2
31	-	VCM	In/Out (analog)	ADC common mode voltage
32	-	INL2	In (analog)	ADC left channel line input2 or microphone input2
33	-	INL1	In (analog)	ADC left channel line input1 or microphone input1
34	H	RSTN	In (digital)	Reset: 0: reset state 1: normal operation
35	-	STBY	In (digital)	Standby mode: 0: normal operation 1: power-down
36	-	EAPWM4	Out (digital)	External amplifier PWM 4B
37	-	EAPWM3	Out (digital)	External amplifier PWM 4A
38	-	EAPWM2	Out (digital)	External amplifier PWM 3B
39	-	EAPWM1	Out (digital)	External amplifier PWM 3A
40	H	EAFTN	Out (digital)	External power fault signal: 0: fault 1: normal operational mode
41	-	EATSN	Out (digital)	External amplifier control: 0: active 1: 3-state
42	-	EAPDN	Out (digital)	External amplifier powerdown (active low)
43	-	ACLK	In (digital), schmitt tr	Reserved pin, connect to ground
44	L	I2CDIS	In (digital)	I^2C disable: 0: I^2C enabled 1: I^2C disabled
48	L	TM	In (digital)	Test mode: 0: normal operation
51	-	NC	-	Not connected

Table 2. Pin list (continued)

Pin	Pull	Name	Type	Description
52	-	XTO	Out (digital), 1.8 V	Crystal output
53	-	XTI	In (digital), 1.8 V	Crystal input or master clock input
54	-	MCLK	In (digital), schmitt tr	Master clock input 3.3-V compatible, schmitt input
55	-	SDATAI2	In (digital)	Input serial audio interface data
56	-	SDATAI1	In (digital)	Input serial audio interface data
57	-	SDATAO2	Out (digital)	Output serial audio interface data
58	-	SDATAO1	Out (digital)	Output serial audio interface data
59	-	LRCLKI2	In/Out (digital)	Input serial audio interface L/R-clock
60	-	LRCLKI1	In/Out (digital)	Input serial audio interface L/R-clock
61	-	LRCLKO	In/Out (digital)	Output serial audio interface L/R-clock (volume DOWN when I2CDIS=1)
62	-	BICLKI2	In/Out (digital)	Input serial audio interface bit clock
63	-	BICLKI1	In/Out (digital)	Input serial audio interface bit clock
64	-	BICLKO	In/Out (digital)	Output serial audio interface bit clock (volume UP when I2CDIS=1)

Table 3. Power supply pin list

Number	Name	Type	Description
2	VCC1	Supply	CMOS bridge channel 1 supply
4	GND1	Ground	CMOS bridge channel 1 ground
5	GND2	Ground	CMOS bridge channel 2 ground
7	VCC2	Supply	CMOS bridge channel 2 supply
8	VCC3	Supply	CMOS bridge channel 3 supply
10	GND3	Ground	CMOS bridge channel 3 ground
15	GND33	Ground	CMOS bridge level shifter ground
16	VCC33	Supply	CMOS bridge level shifter supply
20	DGND1	Ground	Digital ground
22	VDD_REG1	Supply	DC regulator unit supply
23	VDDIO1	Supply	3.3-V IO supply
25	AGND	Ground	ADC analog ground
28	AVDD	Supply	ADC analog supply
45	DGND2	Ground	Digital ground
46	VDD_REG2	Supply	DC regulator unit supply
47	VDDIO2	Supply	3.3-V IO supply
49	PVDD	Supply	PLL analog supply
50	PGND	Ground	PLL analog ground

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Pin name/Symbol	Parameter	Negative	Positive	Unit
VDD_REG1, VDD_REG2	Digital supply voltage	-0.3	4.0	V
VDDIO1, VDDIO2	Digital IO supply voltage	-0.3	4.0	V
PVDD	PLL analog supply voltage	-0.3	4.0	V
AVDD	ADC analog supply voltage	-0.3	4.0	V
VCC1, VCC2, VCC3	CMOS bridge supply voltage	-0.3	4.0	V
VCC33	CMOS bridge level shifter power supply	-0.3	4.0	V
T_{STG}	Storage temperature	-40	150	°C
T_{OP}	Operating junction temperature	-20	125	°C

Note: All grounds must always be within 0.3 V of each other.

3.2 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{VDD_REG1}, V_{VDD_REG2}	Digital supply voltage	2.5	3.3	3.6	V
V_{PVDD}	PLL analog supply voltage	2.5	3.3	3.6	V
V_{AVDD}	ADC analog supply voltage	1.8	3.3	3.6	V
V_{VCC1}, V_{VCC2}, V_{VCC3}	CMOS bridge supply voltage	1.55	-	3.3	V
V_{VCC33}	CMOS bridge level shifter power supply. Ensure that V_{VCC33} <= V_{VCCx} always	1.55	-	3.3	V
V_{VDDIO1}, V_{VDDIO2}	3.3-V IO supply	2.7	3.3	3.6	V
V_{IH}	High input voltage, 1.8-V pads	1.3	-	-	V
	High input voltage, 3.3-V pads	2.0	-	-	
V_{IL}	Low input voltage, 1.8-V pads	-	-	0.6	V
	Low input voltage, 3.3-V pads	-	-	0.8	
T_{amb}	Ambient temperature	0	-	70	°C

3.3 Electrical characteristics

Unless otherwise specified, the results in *Table 6* below are given for the operating conditions V_{CC} = 3.3 V, R_L = 32 Ω, f_{MCLK} = 12.288 MHz, Tamb = 25 °C and with the PLL set to default conditions.

Table 6. Electrical specifications

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
General						
V_{OH}	High output voltage, 1.8-V pads	-	1.4	-	-	V
	High output voltage, 3.3-V pads	-	V_{VDDIO} - 0.15	-	-	
V_{OL}	Low output voltage, 1.8-V pads	I_{OL} = 2 mA	-	-	0.15	V
	Low output voltage, 3.3-V pads	I_{OL} = 2 mA	-	-	0.15	
V_{hys}	Schmitt trigger hysteresis, 3.3-V IO	-	-	0.4	-	V
R_{UP}	Pull-up resistance	-	-	50	-	kΩ
R_{DN}	Pull-down resistance	-	-	50	-	kΩ
I_{STBYIO}	Standby current, pins VDDIO1,2	Pin STBY = 3.3 V CLKOUT disabled	-	450	-	µA
I_{DDIO}	Operating current, pins VDDIO1,2	-	-	3	-	mA
I_{STBYL0}	Standby current, pins VDD_REG1,2	Deep power-down, $V_{VDD\_REG1,2}$ = 3.3 V	-	450	-	µA
I_{STBYL1}	Standby current, pins VDD_REG1,2	Mild power-down, $V_{VDD\_REG1,2}$ = 3.3 V	-	2	-	mA
I_{DDL1}	Operating current, pins VDD_REG1,2	f_{MCLK} = 12.288 MHz, Play from SAI to CMOS bridge and EAPWM, f_{ADC} = 48 kHz on SAI_out, V_{AVDD} = 3.3 V, $V_{VDD\_REG1,2}$ = 3.3 V	-	45	-	mA
I_{STBYPD}	Pre-drive supply current in standby, pin VCC33	-	-	4.7	-	µA

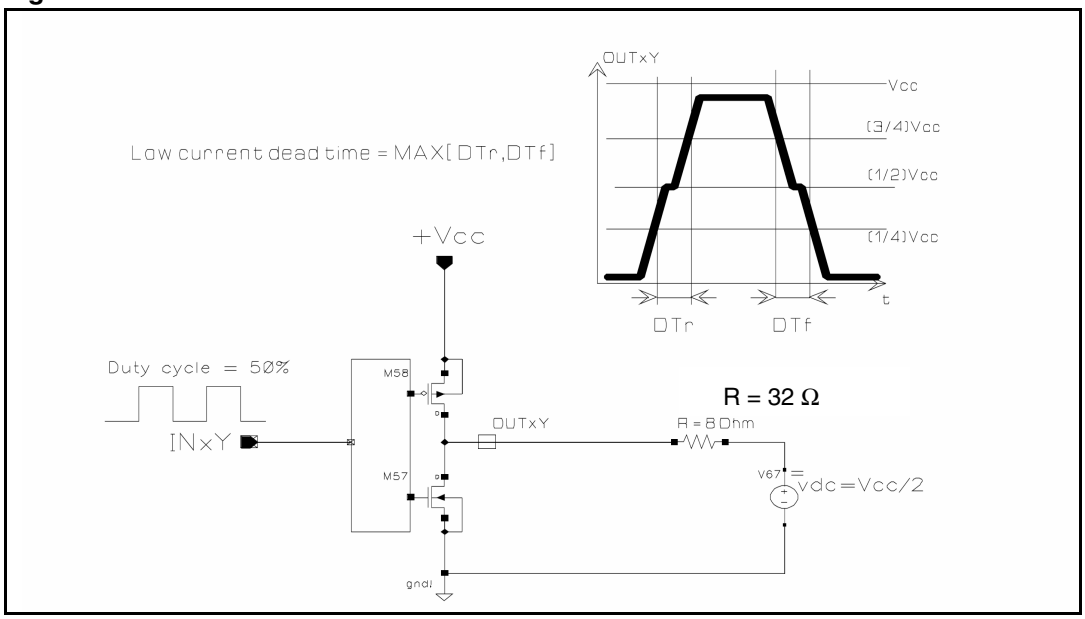
Table 6. Electrical specifications (continued)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
Amplifier (CMOS bridge)							
η	Output power efficiency	-		-	90	-	%
P_{HPOUT}	Output power in HP mode with THD = 1%	3.3-V supply	R_L = 32 Ω	-	41	-	mW
	Output power in HP mode with THD = 10%	3.3-V supply	R_L = 32 Ω	-	53	-	
SNR	Signal to noise ratio	20 Hz to 20 kHz		-	75	-	dB
THD + N	Total harmonic distortion plus noise	RL = 32 Ω, HP mode	0 dBFs In	-	0.3	-	%
			-6 dBFs In	-	0.05	-	
DR	Dynamic range	A-weighted		-	80	-	dB
I_{STBYP}	Current in standby, pins VCCx	-		-	2	-	µA
I_{DDP}	Operating current, pins VCCx	No LC filter, no load, PWM at 50% duty-cycle		-	1	-	mA
I_{DDPD}	Pre-drive supply current in operation, pin VCC33	No load, PWM at 50% duty-cycle		-	250	350	µA
t_R	Driver rise time, pins OUT1-3	Resistive load, see *Figure 3*		-	5	-	ns
t_F	Driver fall time, pins OUT1-3	Resistive load, see *Figure 3*		-	5	-	ns
R_{DSON}	Headphone output stage N/P MOS on-resistance	-		-	500	700	mΩ
I_{OCH}	Over-current limit for OUT1-3 to VCCx short circuit	-		-	1.88	-	A
I_{OCL}	Over-current limit for OUT1-3 to ground short circuit	-		-	1.72	-	A
PLL							
$I_{STDBYPLL}$	PLL supply current in standby	-		-	20	-	µA
I_{DDPLL}	PLL supply current in operation	-		-	0.4	1.0	mA
f_{CLKIN_Range}	Input clock frequency range	-		2.048	-	49.152	MHz
$Duty_{CLKIN}$	Input clock duty cycle	-		40	-	60	%
t_{CLKIN_RF}	Input clock rise/fall time	-		-	-	0.2	ns
f_{F_INT}	PFD input clock frequency	PLL_FR_CTRL = 1		2.048	-	12.288	MHz
f_{VCO_Range}	Clock out range	-		65.536	-	98.304	MHz
$Duty_{VCO}$	Clock out duty cycle	-		35	-	65	%
T_{LOCK}	Lock time	-		-	-	200	µs

Table 6. Electrical specifications (continued)

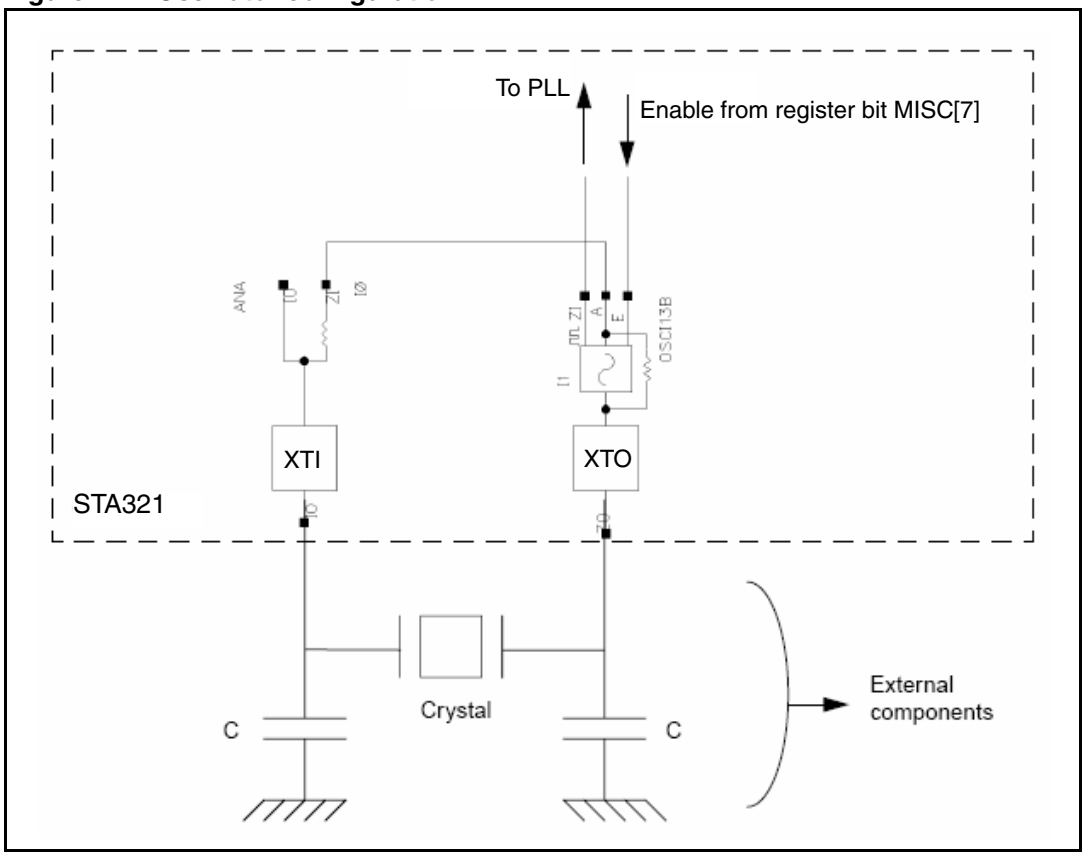
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ADC						
I_{DDA}	Supply current in operating mode	V_{AVDD} = 3.3V	-	10	15	mA
I_{STDBYA}	AVDD supply current in standby	V_{AVDD} = 3.3V	-	2	-	µA
DR	Dynamic range	1 kHz, A-weigthed V_{AVDD} = 3.3 V	-	90	-	dB
SNR_{ADC}	Signal to noise ratio	1 kHz, A-weighted V_{AVDD} = 3.3 V	-	92	-	dB
THD_{ADC}	Total harmonic distortion	1 kHz, -1dB V_{AVDD} = 3.3 V	-	85	-	dB
CT	Channel cross talk	V_{AVDD} = 3.3 V	-	80	-	dB
-	Group delay	Fs mode (f_S = 32 kHz)	-	0.4	-	ms
		Fs_by_2 mode (f_S = 16 kHz)	-	0.7	-	
		Fs_by_4 mode (f_S = 8 kHz)	-	1.4	-	
-	Pass band	-	-	0.4535	-	Fs
-	Pass band ripple	Fs mode (f_S = 44.1 kHz)	-	0.08	-	dB
		Fs_by_2 mode (f_S = 22.05 kHz)	-	0.08	-	
		Fs_by_4 mode (f_S = 11.025 kHz)	-	0.08	-	
-	Stop band attenuation	Fs mode (f_S = 44.1 kHz)	-	45	-	dB
		Fs_by_2 mode (f_S = 22.05 kHz)	-	45	-	
		Fs_by_4 mode (f_S = 11.025 kHz)	-	45	-	
-	Frequency response	-3 dB	-	7	-	Hz
		-0.08 dB	-	50	-	Hz
-	Linear phase deviation	at 20 Hz	-	19.35	-	deg
-	Pass-band ripple	-	-	0.08	-	dB
Headphone detector threshold limits						
E_HP1	HP low threshold	-	-	2.34	-	V
	HP high threshold	-	-	2.52	-	
E_HP2	HP low threshold	-	-	0.7	-	V
	HP high threshold	-	-	0.9	-	

Figure 3. Test circuit



3.4 Embedded crystal oscillator

Figure 4. Oscillator configuration



The STA321 has an integrated oscillator between pins XTI and XTO.

The architecture is a single-stage oscillator with an inverter working as an amplifier. The oscillator stage is biased by an internal resistor (of about 500 kΩ), and requires an external PI network consisting of a crystal and two capacitors as shown in *Figure 4* below. An enable feature is provided in bit 7 of register MISC (address 0xC8) to stop the oscillator and thereby to reduce power consumption.

Not all crystals operate satisfactorily with the type of oscillator used in the STA321. To find out if a crystal is suitable for this device the following transconductance formula must be evaluated and compared to the critical transconductance for the embedded oscillator:

$$Gm = Rm * \omega^2 * (C + 2 * Co)^2 < Gm_{CRITICAL} / 3$$

where ω is the crystal operating frequency, C = CA = CB, Co and Rm are shown in *Figure 5* and $Gm_{CRITICAL}$ is given in *Table 7*.

Figure 5. Equivalent circuit of crystal and external components

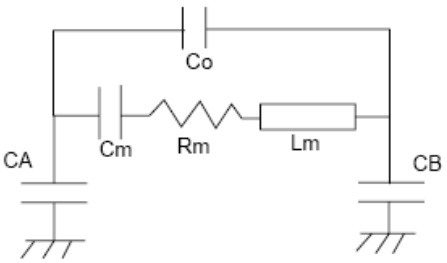


Table 7. Oscillator specifications

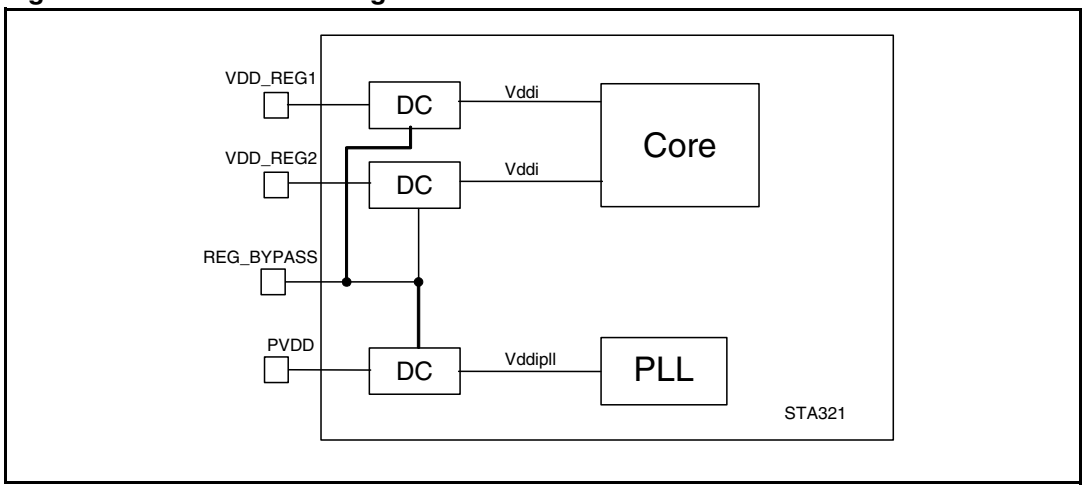
Symbol	Parameter	Min	Typ	Max	Unit
I_{OSC}	Oscillator power consumption with crystal connected (1)	-	-	215	µA
$Duty_{OSC}$	Duty cycle	46.9	47.8%	48.9	%
T_{UP}	Startup time	-	15 * τx	-	s (2)
$Gm_{CRITICAL}$	Oscillator transconductance	1060	-	-	µA/V

1. If no crystal is connected then the power consumption could be much higher.
2. τx is the time constant of the crystal and external components; a typical value is 44 µs.

3.5 Embedded DC regulator

The power supply to the digital STA321 core and PLL is provided via embedded linear DC regulators as shown below in *Figure 6*. When pin REG_BYPASS is tied to ground, the DC regulators are active so that a voltage in the range 2.5 V to 3.6 V applied to pins VDD_REGx or PVDD provides a regulated internal voltage to the core and the PLL. The voltages Vddi and Vddipll range from 1.55 V to 1.95 V depending on operating conditions.

Figure 6. Embedded DC regulator scheme



If the application allows multiple supplies or the power supply requirements are a fundamental constraint, pin REG_BYPASS can be tied high and a 1.8 V external supply can be applied directly to pins VDD_REGx and PVDD. In this case the operating range for such an external supply is 1.55 V to 1.95 V.

Embedded DC regulators imply also static power consumption that must be take into account when the power-down modes are active. The STA321 provides a deep powerdown mode where also the regulators are active but in a low power consumption mode (see *Section 4.3.2 on page 27*).

4 Power-up and power-down sequences

4.1 Device power-up

After providing the power supply to the device, it is necessary to wait until the DC regulator PWUP time has elapsed before the device can be set up and used for normal operations. (see *Figure 7*).

Figure 7. Startup sequence

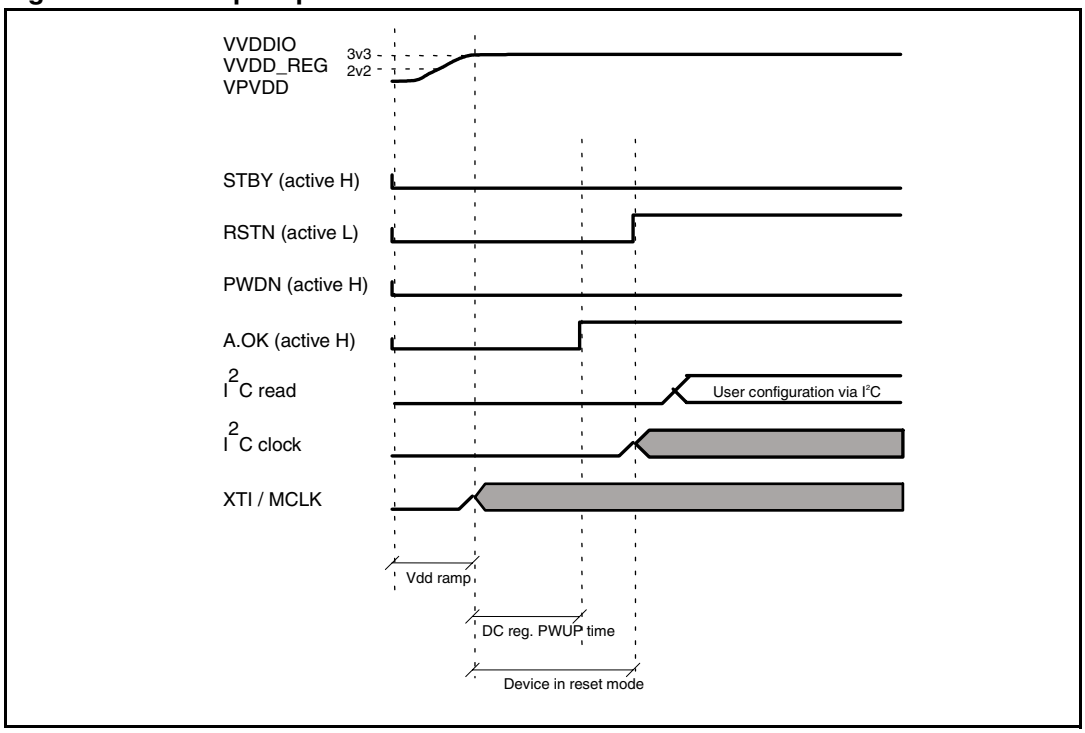


Table 8. Power-up signal description

Signal/pin	Type	Description
VDDIO	Supply	Power supply of the digital pads (= VDDIO1,2)
VDD_REG	Supply	Power supply of the system core (= VDD_REG1,2)
PVDD	Supply	Power supply of the PLL
STBY	In (digital)	External standby signal provided by the user
RSTN	In (digital)	External reset signal provided by the user
PWDN	Internal	Power-down of the DC regulator cell, controlled by the core
A. OK	Internal	DC regulator status, when active the 1.8 V is provided to the core
I^2C read	In (I^2C)	Configuration commands coming to the I^2C interface
I^2C clock	Internal	I^2C peripheral clock
XTI/MCLK	In (digital)	Clock input source

Table 9. Startup timings

Parameter	Description	Min	Typ	Max	Unit
DC reg. power-up time	Start up time of the DC Regulator after connecting the power	-	-	300	µs
Device in reset mode	Must be greater than (VDD time + DC reg. power-up time)	-	-	-	µs

Table 10. Configuration example

Register address	Value	Description
0xC9	0x00	Remove PLL bypass
0xCA	0x00	Headphone detection polarity = 0
0xB8	0x4A	Configure SAI output: SAI_out1 = SAI_in1, SAI_out2 = SAI_in2
0xB7	0x38	SRC source select: SRC1 = ADC, SRC2 = ADC
0xC6	0x02	ADC clock on
0xB2	0xF3	I^2S configuration
0xC8	0x21	Core clock on, SAI/ADC audio set to 32 kHz - 48 kHz range
0xB2	0xD3	SAI_out: output enabled
0xA0	0x00	Soft volume removed
0x00	0x00	Remove bridge 3-state

4.2 Software power-down mode

The software power-down is obtained by configuring the appropriate I^2C registers.

In order to obtain flexibility every peripheral has its independent, standby signal and several gating clock cells are available.

Obviously, the I^2C peripheral can not be turned off in this mode, otherwise the device can recover from the power-down state only via the reset pin.

In the table below EA is embedded amplifier and CB is CMOS bridge. For complete information this table must be used in conjunction with *Chapter 14: Register description on page 77*.

Table 11. Registers for power-down

Description	Register bit	Address
Put EA in standby	*FFXCFG1*[7]	*0x00 on page 81*
Put CB in standby	*FFXCFG1*[6]	*0x00*
Put PLL in standby	*PLLPFE*[5]	*0xC4 on page 132*
Put ADC in standby	*ADCCFG0*[3]	*0xC6 on page 133*
Turn core clock off	*MISC*[0]	*0xC8 on page 135*
Turn ADC clock off	*ADCCFG0*[1]	*0xC6*

Table 11. Registers for power-down (continued)

Description	Register bit	Address
Turn SRC clock off	*CKOCFG*[3]	*0xC7 on page 134*
Turn PROC clock off	*CKOCFG*[2]	*0xC7*
Turn FFX clock off	*CKOCFG*[4]	*0xC7*

4.2.1 Configuration example

This is an example of the register setup for power-down clock. It is assumed that every peripheral is already configured and working correctly.

There are other configuration examples to help you get started please refer to other chapters and also to *Chapter 14: Register description on page 77* in order to get all the necessary and complementary details.

Turn off all the peripherals.

Note: The MCLK (or XTI) must be used as system clock (sys_clk) before setting the PLL to standby.

Table 12. Example configurations for power-down

Register bit	Address	Value	Description
EA_STBY CB_STBY	*0x00 on page 81*	0xC0	Set the embedded power amplifier and CMOS bridge to power-down
CLK_FFX_ON	*0xC7 on page 134*	0x0C	Turn off the FFX modulator clock
ADC_STBY	*0xC6 on page 133*	0x09	Set the ADC into standby mode
CLK_ADC_ON	*0xC6*	0x80	Turn the ADC clock off
CLK_PROC_ON	*0xC7*	0x08	Turn the processing clock off
CLK_SRC_ON	*0xC7*	0x00	Turn the sample rate converter clock to off
PLL_BYP_UNL	*0xC4 on page 132*	0x80	Bypass the PLL clock and use MCLK (or XTI) as source clock when the PLL is not locked (a safety operational mode)
PLL_PWDN	*0xC4*	0xA0	Put the PLL in standby
CLK_CORE_ON	*0xC8 on page 135*	0x00	Turning off the core clock

4.3 Hardware power-down mode

The hardware power-down is obtained by asserting pin STBY to high.

There are two power-down options available, namely mild mode and full (or deep) mode, that could be selected using the DC_STBY_EN signal in register STBY_MODES

Figure 8 summarizes the main power-down sequence. “Power on” is the normal operating status where all the startup procedures have already been executed. The rectangular boxes indicate the steps to be done by the user whilst the rounded boxes indicate the steps done by the device.

Figure 8. Hardware power-done sequence

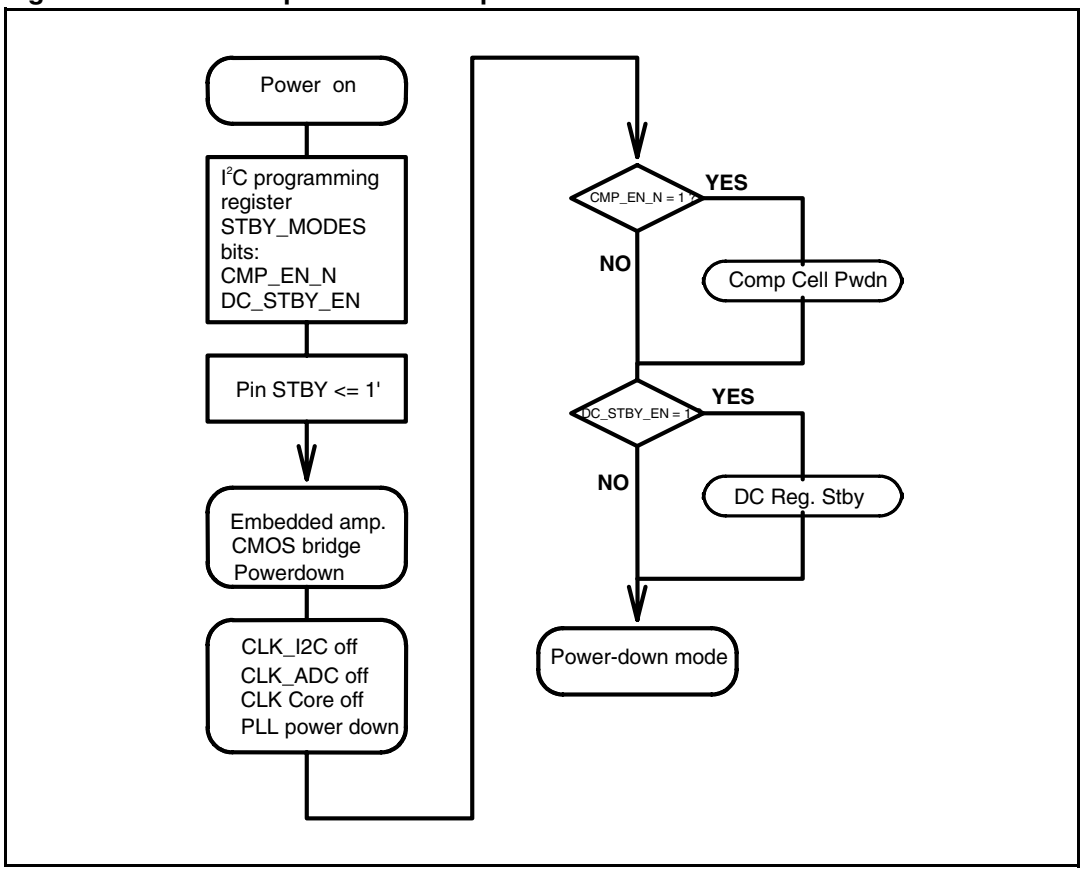


Table 13. Frequently used signals

Name	Description
STBY	Input pin *STBY on page 11*
PWDN DC regulator	Internal
A. OK DC regulator	Internal
CMP_EN_N	Bit 1, register *STBY_MODES on page 139*
EA_STBY CB_STBY	Bits 7:6, register *FFXCFG1 on page 81*
EA/CB volume	Internal
PLL_UNLOCK	Bit 7, register *PLLST on page 132*
PLL_PWDN	Bit 5, register *PLLPFE on page 132*
CLK_PROC_ON	Bit 2, register *CKOCFG on page 134*
CLK_PROC	Processing clock
CLK_FFX_ON	Bit 4, register *CKOCFG on page 134*
clk_ffx	FFX clock
CLK_ADC_ON	Bit 1, register *ADCCFG0 on page 133*
clk_adc	ADC clock
CLK_SRC_ON	Bit 3, register *CKOCFG on page 134*
clk_src	SRC clock
CMP_EN_N	Bit 1, register *STBY_MODES on page 139*
DC_STBY_EN	Bit 0, register *STBY_MODES on page 139*
FFX_ULCK_PLL	Bits 4:3, register *FFXCFG1 on page 81*

4.3.1 Mild power-down

In this case, the device is put into a mild power-down mode.

All the peripherals are set to standby and their clocks turned off.

The I^2C configuration is not required as the default values of the registers are sufficient.

- Initial conditions:

  FFX_ULCK_PLL = 10

  CMP_EN_N = 0

  DC_STBY_EN = 0

- Going into power-down:

  After the assertion of the pin STBY, the following actions are taken by the device:

1. Embedded amplifier (EA) and CMOS bridge (CB) volume are set to mute (the length of this step changes according to the fade-out ramp configuration).
2. EA and CB are put into power-down.

   After the previous operation is completed:
3. All peripherals are turned off (regardless the register settings).
4. The PLL clock is bypassed, the system clock (sys_clk in *Figure 11 on page 29*) is XTI.
5. All clocks are shut down.

- Returning to normal mode:

  After the release of the pin STBY, the power-up procedure takes place:

1. All clocks are turned on.
2. All peripherals are restored to their previous status (based on the last register settings).
3. If the PLL clock was the system clock it will be selected again after the locking time.
4. The EA and the CB execute the fade-in procedure before becoming ready to be used (the length of this step changes according to the fade-in ramp configuration).