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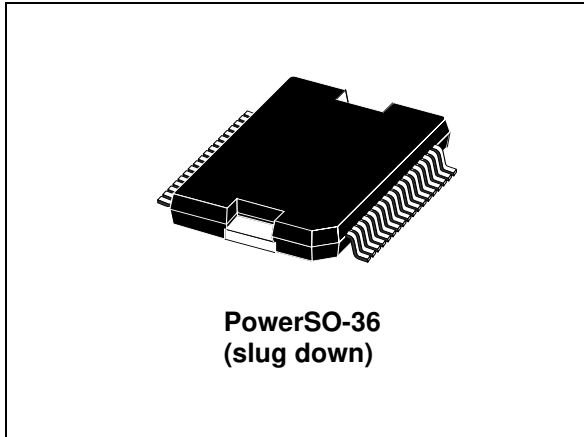
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2.1 channel high-efficiency digital audio system

Datasheet - production data



Features

- Wide supply voltage range (10 V - 36 V)
- Three power output configurations
 - 2 x 10 W + 1 x 20 W
 - 2 x 20 W
 - 1 x 40 W
- Thermal protection
- Under-voltage protection
- Short-circuit protection
- PowerSO-36 slug down package
- 2.1 channels of 24-bit DDX[®]
- 100-dB SNR and dynamic range
- 32 kHz to 192 kHz input sample rates
- Digital gain/attenuation +48 dB to -80 dB in 0.5-dB steps
- Four 28-bit user programmable biquads (EQ) per channel
- I²C control
- 2-channel I²S input data interface
- Individual channel and master gain/attenuation
- Individual channel and master soft and hard mute
- Individual channel volume and EQ bypass
- DDX[®] POP free operation
- Bass/treble tone control
- Dual independent programmable limiters/compressors
- AutoModes™ settings for:
 - 32 preset EQ curves
 - 15 preset crossover settings
 - Auto volume controlled loudness
 - 3 preset volume curves
 - 2 preset anti-clipping modes
 - Preset night-time listening mode
 - Preset TV AGC
- Input and output channel mapping
- AM noise-reduction and PWM frequency shifting modes
- Soft volume update and muting
- Auto zero detect and invalid input detect muting selectable DDX[®] ternary or binary PWM output plus variable PWM speeds
- Selectable de-emphasis
- Post-EQ user programmable mix with default 2.1 bass-management settings
- Variable max power correction for lower full-power THD
- Four output routing configurations
- Selectable clock input ratio
- 96 kHz internal processing sample rate, 24 to 28-bit precision
- Video application supports 576 * fs input mode

Table 1. Device summary

Order code	Package
STA323W13TR	PowerSO-36 in tape & reel

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1 Description

The STA323W is a single-chip audio system comprising digital audio processing, digital amplifier control and a DDX[®] power-output stage. The STA323W uses all-digital amplification to provide high-power, high-quality and high-efficiency.

The STA323W power section consists of four independent half-bridges. These can be configured, by digital control, to operate in the following modes.

Two channels, provided by two half-bridges, and a single full-bridge giving up to 2 x 10 W + 1 x 20 W of power output.

Two channels, provided by two full-bridges, giving up to 2 x 20 W of power.

A single, parallel, full-bridge channel capable of high-current operation and giving 1 x 40W output.

The STA323W also provides a full set of digital processing features. This includes up to four programmable 28-bit biquads (EQ) per channel, and bass and treble tone control. AutoModes™ enable a time-to-market advantage by substantially reducing the amount of software development needed for specific functions. These includes auto volume loudness, preset volume curves and preset EQ settings. New advanced AM radio-interference reduction modes are also provided.

The serial audio data input interface accepts all existing formats, including the I²S.

Three channels of DDX[®] processing are provided. This high-quality conversion from PCM audio to DDX patented 3-state PWM switching provides over 100 dB of SNR and dynamic range.

Figure 1. Block diagram

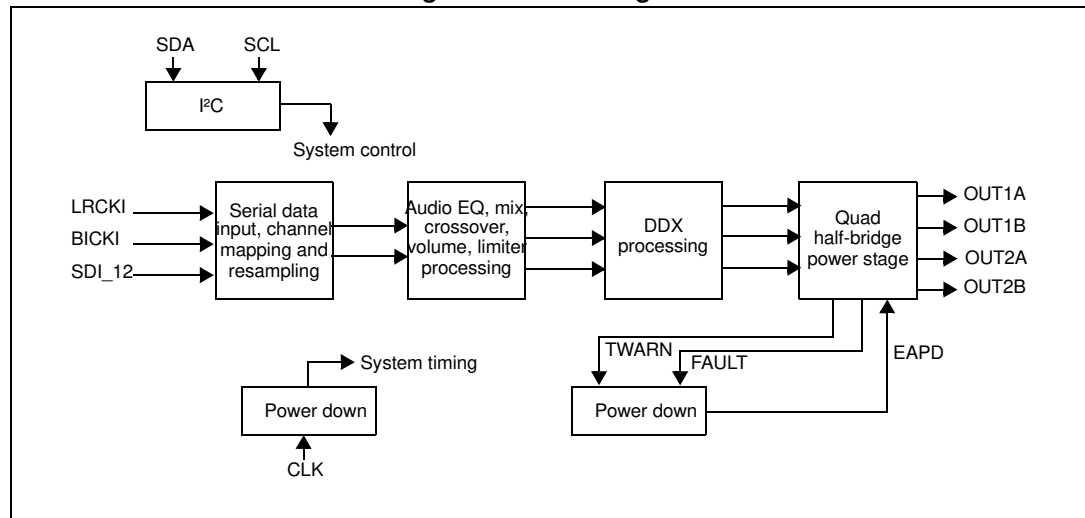
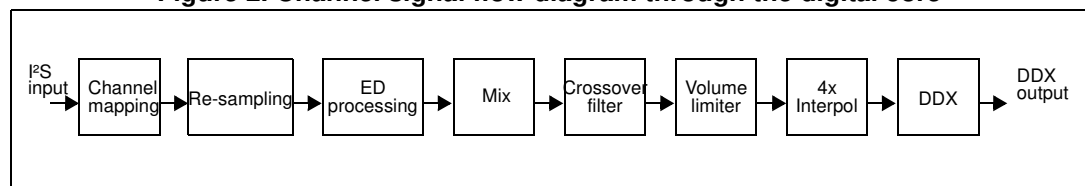


Figure 2. Channel signal flow diagram through the digital core

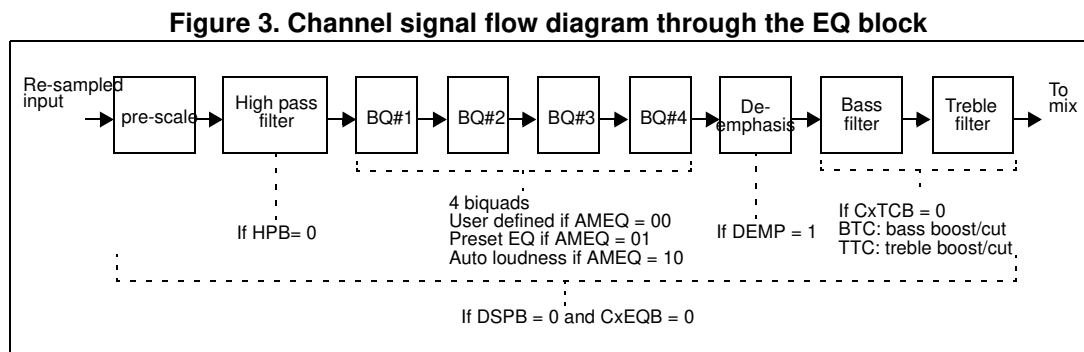


1.1 EQ processing

Two channels of input data (re-sampled if necessary) at 96 kHz are provided to the EQ processing block. In these blocks, up to four user-defined Biquads can be applied to each of the two channels.

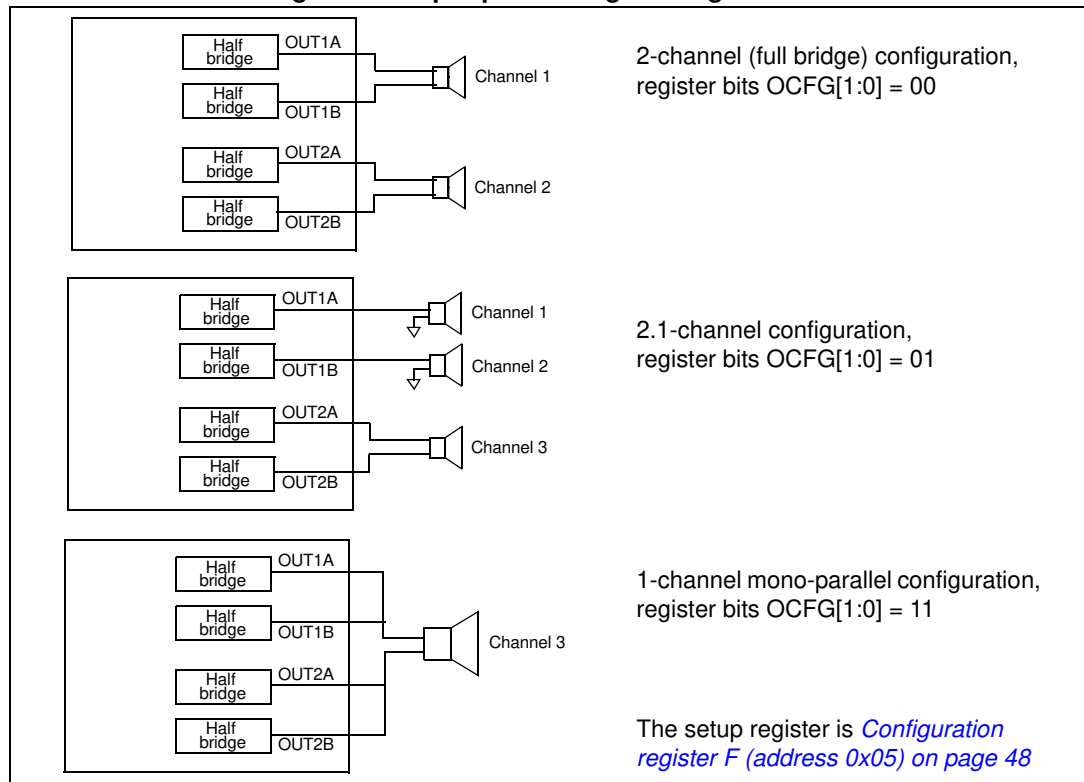
Pre-scaling, DC-blocking high-pass, de-emphasis, bass, and tone control filters can also be implemented by means of configuration parameter settings.

The entire EQ block can be bypassed for all channels simultaneously by setting the DSPB bit to 1. The CxEQBP bits can also be used to bypass the EQ functionality on a per channel basis. *Figure 3* shows the internal signal flow through the EQ block.



1.2 Output options

Figure 4. Output power stage configurations



2 Applications

Table 2. Component selection "Table A" - full-bridge operation

Load	Inductor	Capacitor
4 Ω	10 μH	1.0 μF
6 Ω	15 μH	470 nF
8 Ω	22 μH	470 nF

Table 3. Component selection "Table B" - binary half-bridge operation

Load	Inductor	Capacitor
4 Ω	22 μH	680 nF
6 Ω	33 μH	470 nF
8 Ω	47 μH	390 nF

Table 4. Component selection "Table C" - mono operation

Load	Inductor	Capacitor
2 Ω	4.7 μH	2.0 μF
3 Ω	6.8 μH	1.0 μF
4 Ω	10 μH	1.0 μF

Figure 5. Schematic for 2 (half-bridge) channels + 1 (full-bridge) channel

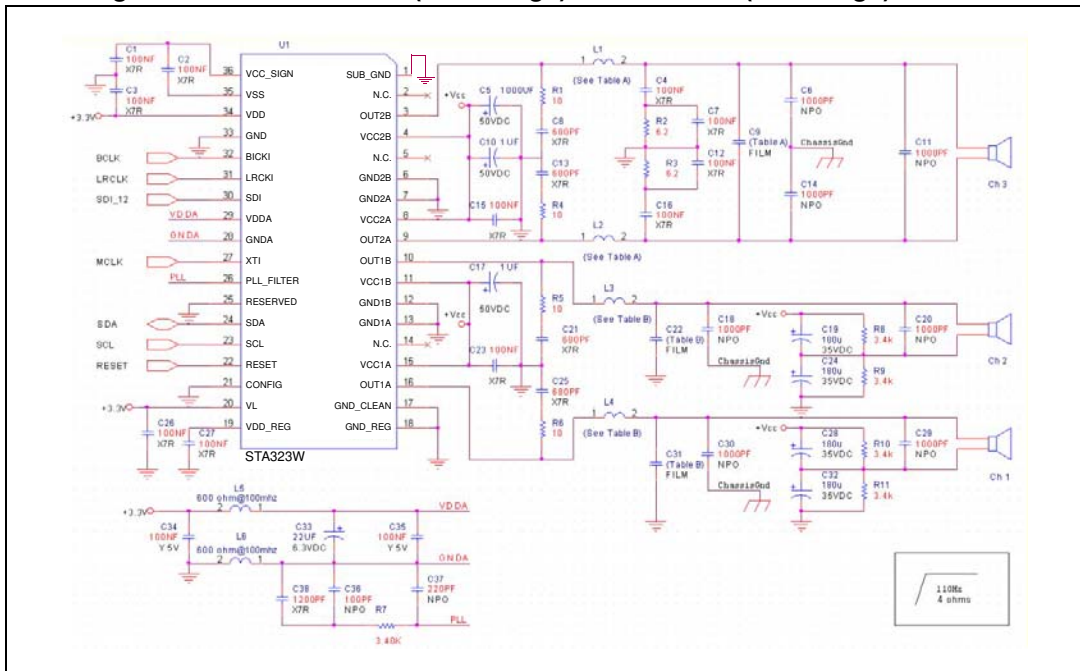


Figure 6. Power schematic for 2 (full-bridge) channels

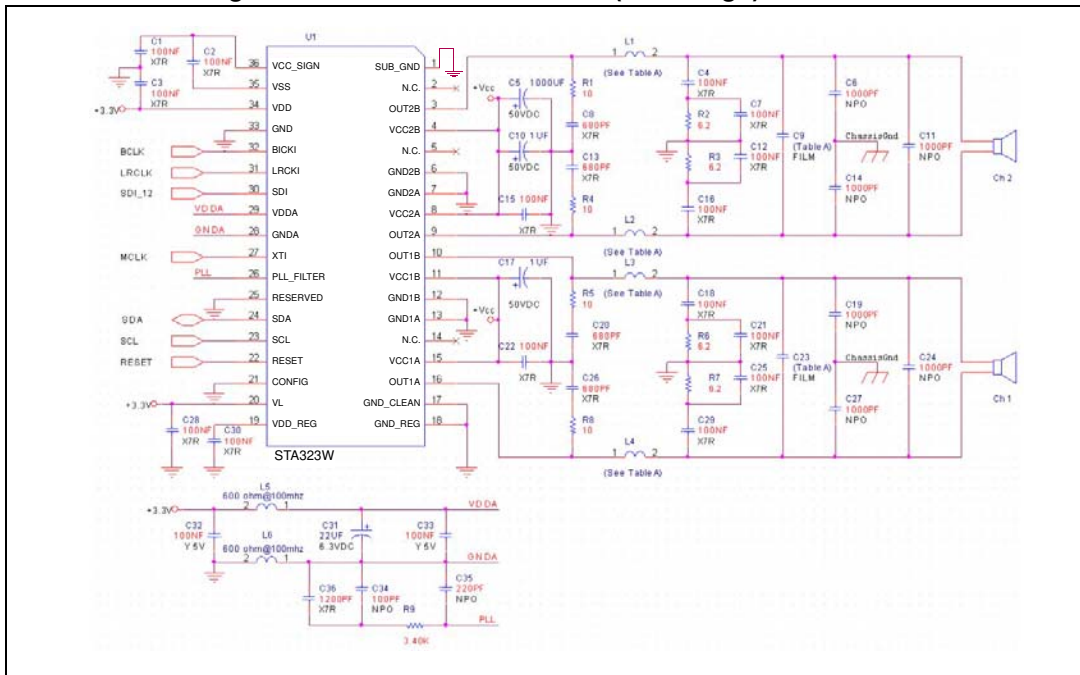
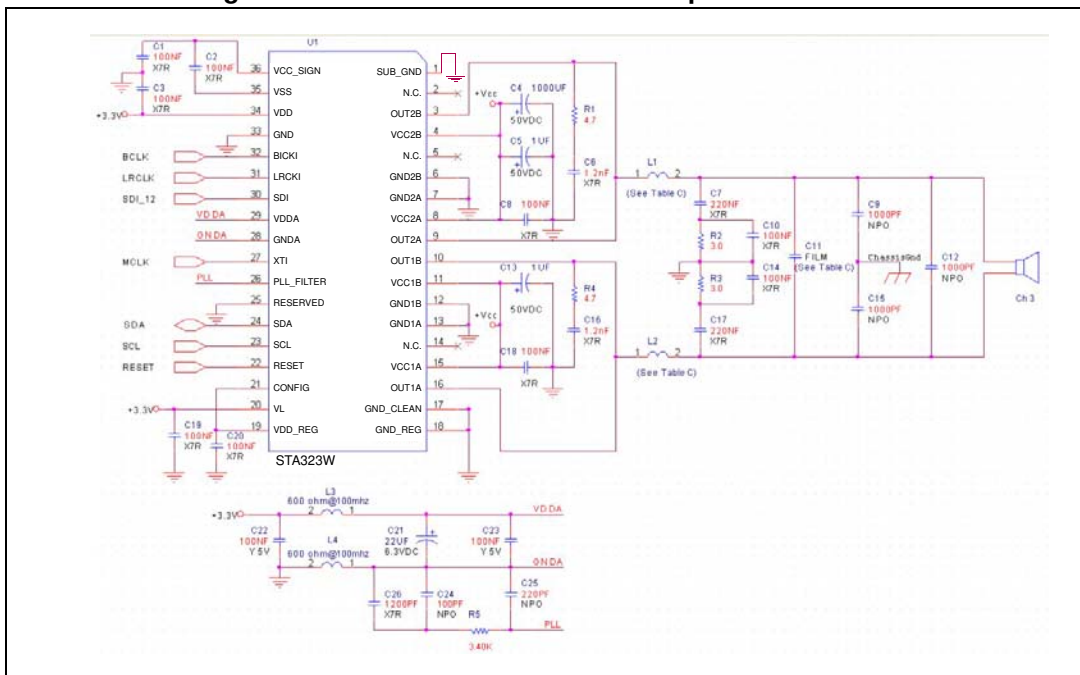


Figure 7. Power schematic for 1 mono parallel channel



3 Pin out

3.1 Pin numbering

Figure 8. Package pins (viewed from top of device)

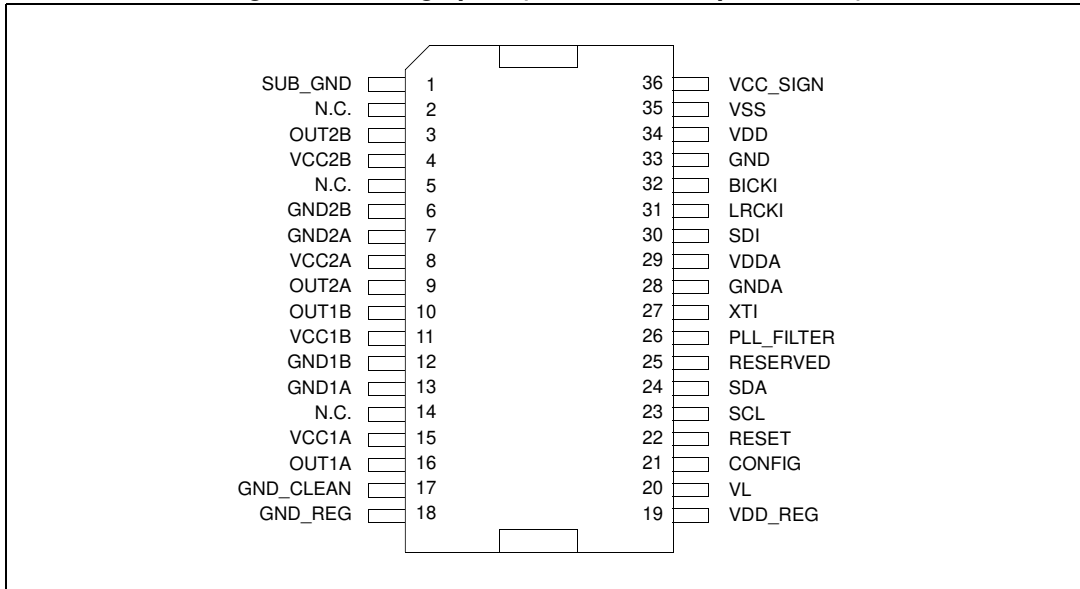


Table 5. Pin list

Pin	Type	Name	Description
1	I/O	SUB_GND	Ground
2	N.C.	N.C.	Not connected
3	O	OUT2B	Output half bridge 2B
4	I/O	VCC2B	Positive supply
5	N.C.	N.C.	Not connected
6	I/O	GND2B	Negative supply
7	I/O	GND2A	Negative supply
8	I/O	VCC2A	Positive supply
9	O	OUT2A	Output half bridge 2A
10	O	OUT1B	Output half bridge 1B
11	I/O	VCC1B	Positive supply
12	I/O	GND1B	Negative supply
13	I/O	GND1A	Negative supply
14	N.C.	N.C.	Not connected
15	I/O	VCC1A	Positive supply
16	O	OUT1A	Output half bridge 1A

Table 5. Pin list (continued)

Pin	Type	Name	Description
17	I/O	GND_CLEAN	Reference ground
18	I/O	GND_REG	Substrate ground
19	I/O	VDD_REG	Logic supply
20	I/O	VL	Logic supply to power section
21	I	CONFIG	Logic levels
22	I	RESET	Reset
23	I	SCL	I ² C serial clock
24	I/O	SDA	I ² C serial data
25	-	RESERVED	Reserved test pin must be connected to ground
26	I	PLL_FILTER	Connection to PLL filter
27	I	XTI	PLL input clock
28	I/O	GND_A	Analog ground
29	I/O	VDD_A	Analog supply 3.3
30	I	SDI_12	I ² S serial data channels 1 and 2
31	I/O	LRCKI	I ² S left/right clock,
32	I	BICKI	I ² S serial clock
33	I/O	GND	Digital ground
34	I/O	VDD	Digital supply 3.3 V
35	I/O	VSS	5 V regulator referred to Vcc
36	I/O	VCC_SIGN	5 V regulator referred to ground

3.2 Pin description

OUT1A, 1B, 2A and 2B (pins 16, 10, 9 and 3)

The half-bridge PWM outputs 1A, 1B, 2A and 2B provide the inputs signals to the speakers.

RESET (pin 22)

Driving RESET low sets all outputs low and returns all register settings to their default (reset) values. The reset is asynchronous to the internal clock.

SDA, SCL (pins 24, 23)

The SDA (I²C Data) and SCL (I²C Clock) pins operate according to the I²C specification (See [Chapter 6 on page 33](#).) Fast-mode (400 kB/s) I²C communication is supported.

VDDA, GNDA (pins 29,28)

The phase locked loop power is applied here. This +3.3V supply must be well decoupled and filtered for good noise immunity since the audio performance of the device depends upon the PLL circuit.

CLK (pin 27)

This is the master clock input used by the digital core. The master clock must be an integer multiple of the LR clock frequency. Typically, the master clock frequency is 12.288 MHz ($256 * f_s$) for a 48kHz sample rate; it is the default setting at power-up. Care must be taken to provide the device with the nominal system clock frequency; over-clocking the device may result in anomalous operation, such as inability to communicate.

PLL_FILTER (pin 26)

This is the connection for the external filter components for the PLL loop compensation. Refer to the schematic diagram [Figure 7: Power schematic for 1 mono parallel channel on page 13](#) for the recommended circuit.

BICKI (pin 32)

The serial or bit clock input is for framing each data bit. The bit clock frequency is typically $64 * f_s$ using I²S serial format.

SDI (pin 30)

This is the serial data input where PCM audio information enters the device. Six format choices are available including I²S, left or right justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

LRCKI (pin 31)

The left/right clock input is for data word framing. The clock frequency is at the input sample rate, f_s .

4 Electrical specifications

Table 6. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DD_3.3}	3.3 V I/O power supply	-0.5 to 4	V
V _i	Voltage on input pins	-0.5 to (V _{DD} +0.5)	V
V _o	Voltage on output pins	-0.5 to (V _{DD} +0.5)	V
T _{stg}	Storage temperature	-40 to +150	°C
T _{amb}	Ambient operating temperature	-40 to +85	°C
V _{CC}	DC supply voltage	40	V
V _{MAX}	Maximum voltage on pin 20	5.5	V

Table 7. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
R _{thj-case}	Thermal resistance junction to case (thermal pad)			2.5	°C/W
T _{j-SD}	Thermal shut-down junction temperature		150		°C
T _{WARN}	Thermal warning temperature		130		°C
T _{h-SD}	Thermal shut-down hysteresis		25		°C

Table 8. Recommended DC operating conditions

Symbol	Parameter	Value	Unit
V _{DD_3.3}	I/O power supply	3.0 to 3.6	V
T _j	Operating junction temperature	-40 to +125	°C

4.1 General interface specifications

Operating conditions V_{DD33} = 3.3 V ±0.3 V, T_{amb} = 25° C unless otherwise specified.

Table 9. General interface electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I _{il}	Leakage current: low level input, no pull-up	V _i = 0 V ⁽¹⁾			1	µA
I _{ih}	Leakage current: high level input, no pull-down	V _i = V _{DD33} ⁽¹⁾			2	µA
I _{oZ}	Leakage current: 3-state output without pull-up/down	V _i = V _{DD33} ⁽¹⁾			2	µA
V _{esd}	Electrostatic protection (human body model)	Leakage < 1µA	2000			V

1. The leakage currents are generally very small < 1 nA. The values given here are maximum after an electrostatic stress on the pin.

4.2 DC electrical specifications (3.3 V buffers)

Operating conditions $V_{DD33} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $T_{\text{amb}} = 25^\circ \text{ C}$ unless otherwise specified

Table 10. DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IL}	Low level Input voltage				0.8	V
V_{IH}	High level Input voltage		2.0			V
V_{hyst}	Schmitt trigger hysteresis		0.4			V
V_{ol}	Low level output	$I_{ol} = 2\text{mA}$			0.15	V
V_{oh}	High level output	$I_{oh} = -2\text{mA}$	$V_{DD} - 0.15$			V

4.3 Power electrical specifications

Operating conditions $V_{DD33} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_L = 3.3 \text{ V}$, $V_{CC} = 30 \text{ V}$, $T_{\text{amb}} = 25^\circ \text{ C}$ unless otherwise specified.

Table 11. Power electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{dsON}	Power Pchannel/Nchannel MOSFET R_{dsON}	$I_d = 1 \text{ A}$		200	270	$\text{m}\Omega$
I_{dss}	Power Pchannel/Nchannel leakage I_{dss}	$V_{CC} = 35 \text{ V}$			50	μA
g_N	Power Pchannel R_{dsON} matching	$I_d = 1 \text{ A}$	95			%
g_P	Power Nchannel R_{dsON} matching	$I_d = 1 \text{ A}$	95			%
Dt_s	Low current dead time (static)	See test circuits , Figure 9 and Figure 10		10	20	ns
t_{dON}	Turn-on delay time	Resistive load			100	ns
t_{dOFF}	Turn-off delay time	Resistive load			100	ns
t_r	Rise time	Resistive load, Figure 9 and Figure 10			25	ns
t_f	Fall time	Resistive load, Figure 9 and Figure 10			25	ns
V_{CC}	Supply voltage		8		36	V
V_L	Low logical state voltage	$V_L = 3.3 \text{ V}$	0.8			V
V_H	High logical state voltage	$V_L = 3.3 \text{ V}$			1.7	V
$I_{VCC-PWRDN}$	Supply current from V_{CC} in PWRDN	$PWRDN = 0$			3	mA
$I_{VCC-hiz}$	Supply current from V_{CC} in 3-state	$V_{CC} = 30 \text{ V}$, 3-state		22		mA

Table 11. Power electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{VCC}	Supply current from V_{CC} in operation (both channel switching)	Input pulse width = 50% duty, switching frequency = 384 kHz, no LC filters;		80		mA
I_{out-sh}	Overcurrent protection threshold (short circuit current limit)		4	6		A
V_{UV}	Under voltage protection threshold			7		V
t_{pw-min}	Output minimum pulse width	No Load	70		150	ns
P_o	Output power	THD = 10%, $R_L = 8 \Omega$, $V_{CC} = 18 V$		20		W
P_o	Output power	THD = 1%, $R_L = 8 \Omega$, $V_{CC} = 18 V$		16		W

4.4 Timing specifications

Table 12. Timing characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{RESET}	Hold time for RESET (pin 22)	Active low rest	100			ns
f_{VCO}	VCO free run frequency	No clock applied to XT1	18	28		MHz

Figure 9. Test circuit 1

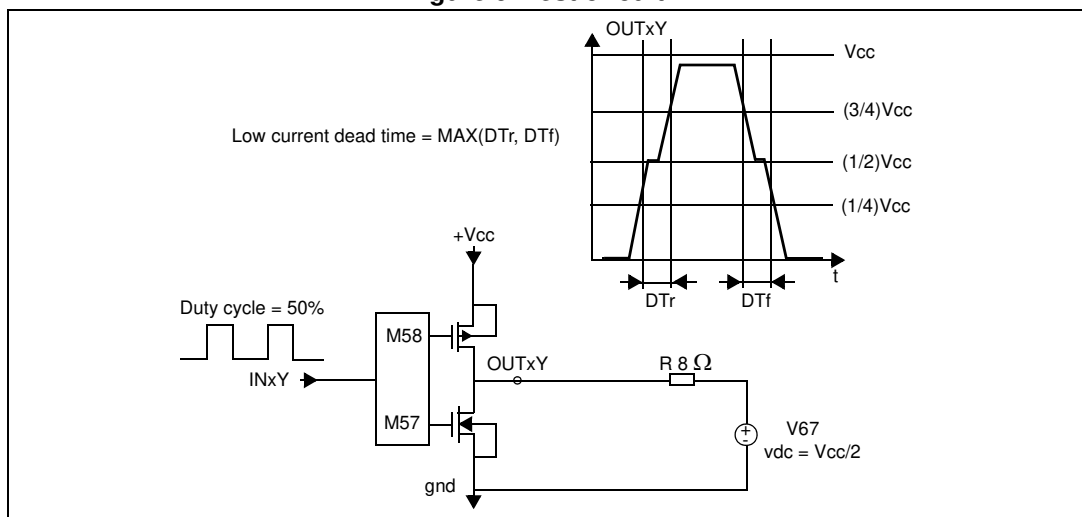
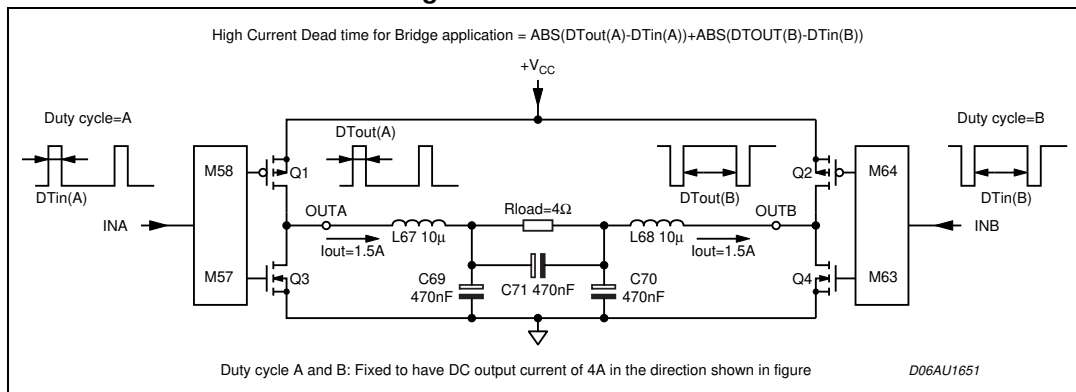


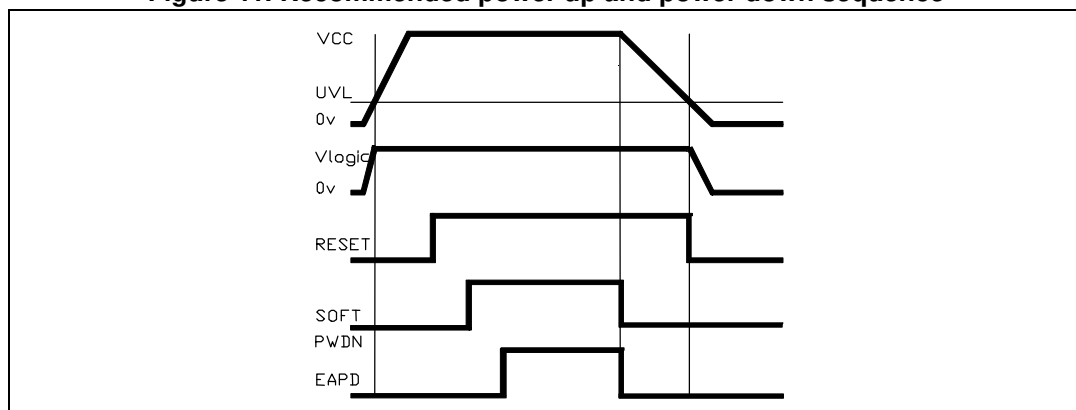
Figure 10. Test circuit 2



4.5 Power supply and control sequencing

Figure 11 shows the recommended power-up and power-down sequencing. The "time zero" reference point is taken where V_{CC} crosses the under voltage lockout threshold.

Figure 11. Recommended power up and power down sequence



5 Electrical characteristics curves

5.1 Output power against supply voltage

Figure 12. Stereo mode - output power vs. supply voltage, THD+N = 10%

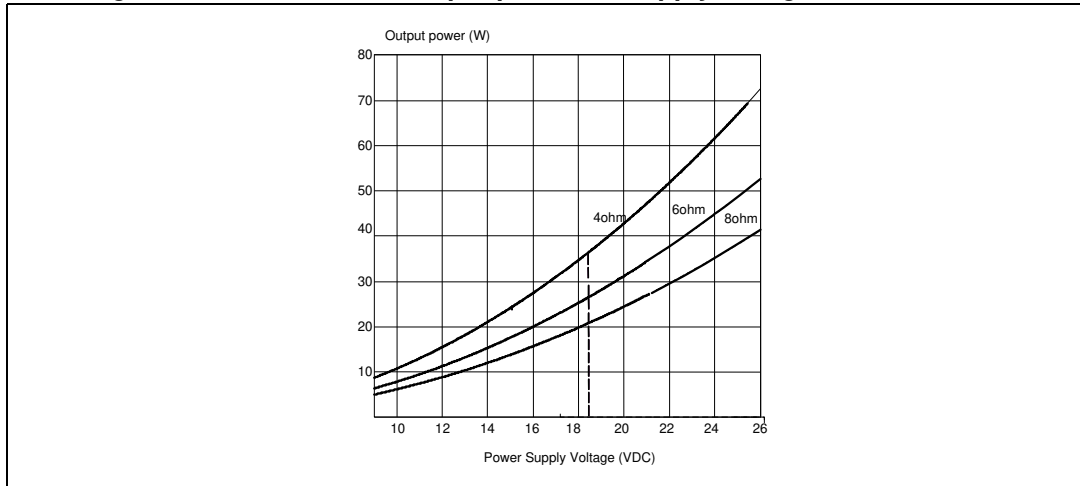


Figure 12 shows the full-scale output power (0 dBFS digital input with unity amplifier gain) as a function of power supply voltage for 4, 6, and 8 Ω loads in either DDX[®] mode or binary full bridge mode. Output power is constrained for higher impedance loads by the maximum voltage limit of the STA323W and by the over-current protection limit for lower impedance loads. The minimum threshold for the over-current protection circuit of the STA323W is 4 A (at 25° C) but the typical threshold is 6 A for the device. The solid curves shows the typical output power capability of the device. The dotted curves shows the output power capability constrained to the minimum current specification of the STA323W. The output power curves assume proper thermal management of the power device's internal dissipation.

Figure 13. Output power vs. supply for stereo bridge, THD+N=1%

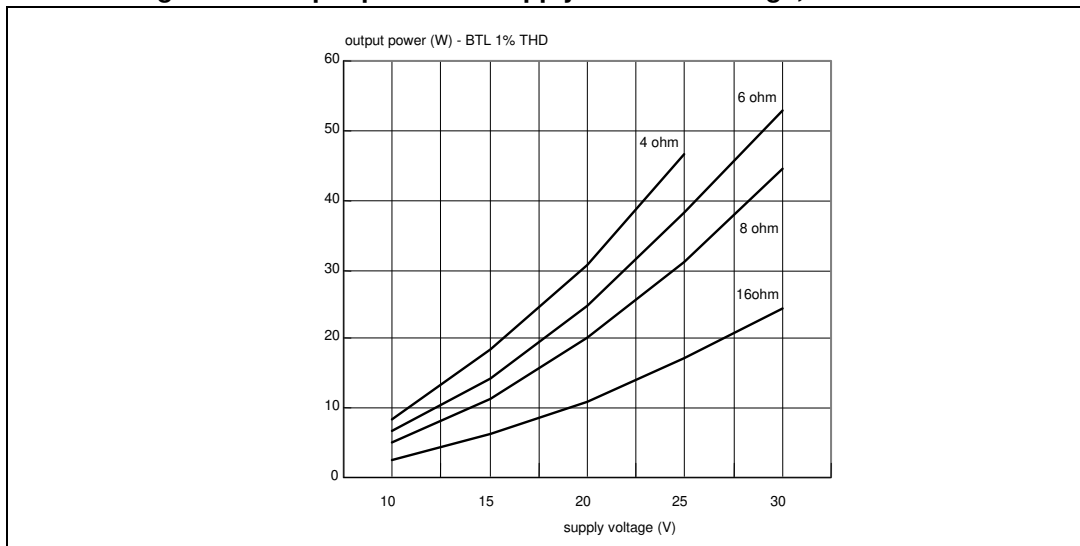


Figure 13 shows the mono mode output power as a function of power supply voltages for loads of 4, 6, 8 and 16 Ω. The same current limits as those given for Figure 12 apply, except output current is 8 A minimum, with 12 A typical in the mono-bridge configuration. The solid curves show typical performance and dashed curves depict the minimum current limit. The output power curves assume proper thermal management of the power device internal dissipation.

Figure 14. Half-bridge binary mode output power vs. supply, THD+N=10%

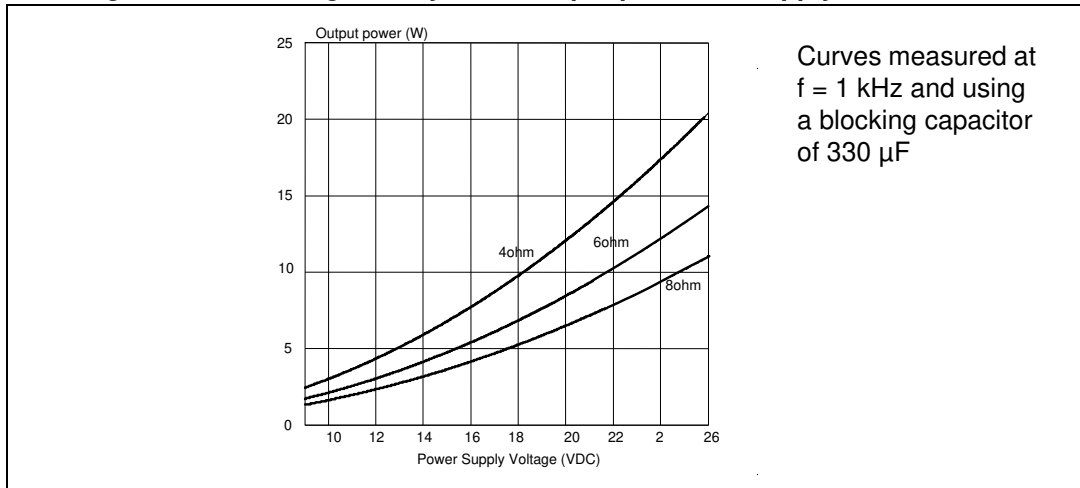
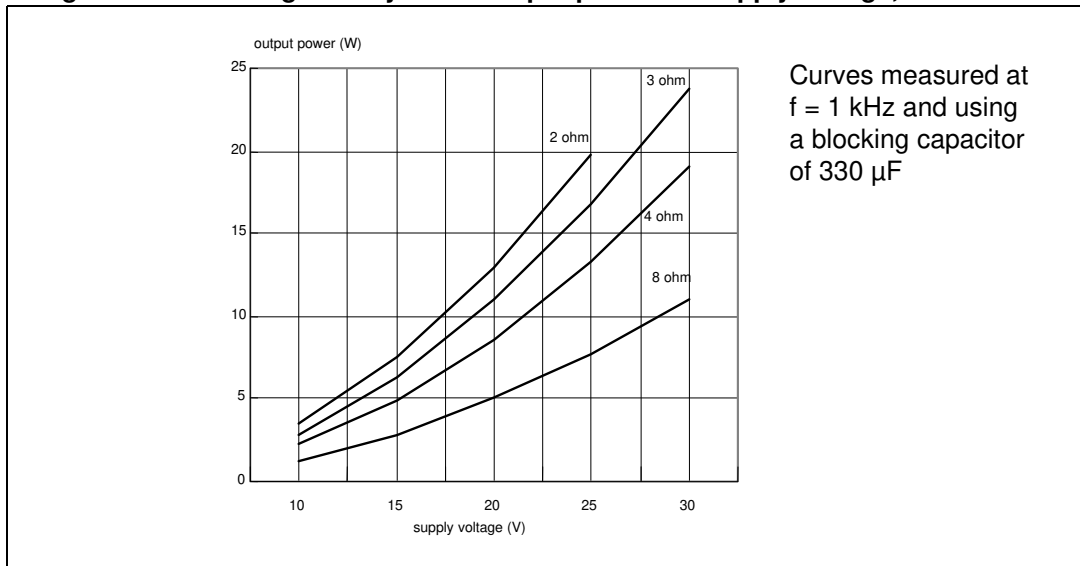


Figure 14 shows the output power as a function of power supply voltages for loads of 4, 6, and 8 Ω when the STA323W is operated in a half-bridge binary mode. The curves depict typical performance. Minimum current limit is not reached for these combinations of voltage and load impedance. The output power curves assume proper thermal management of the power device internal dissipation.

Figure 15. Half-bridge binary mode output power vs. supply voltage, THD+N=1%



5.2 Audio performance

5.2.1 Stereo mode, operation with $V_{CC} = 26\text{ V}$, $8\ \Omega$ load

Figure 16. Typical efficiency

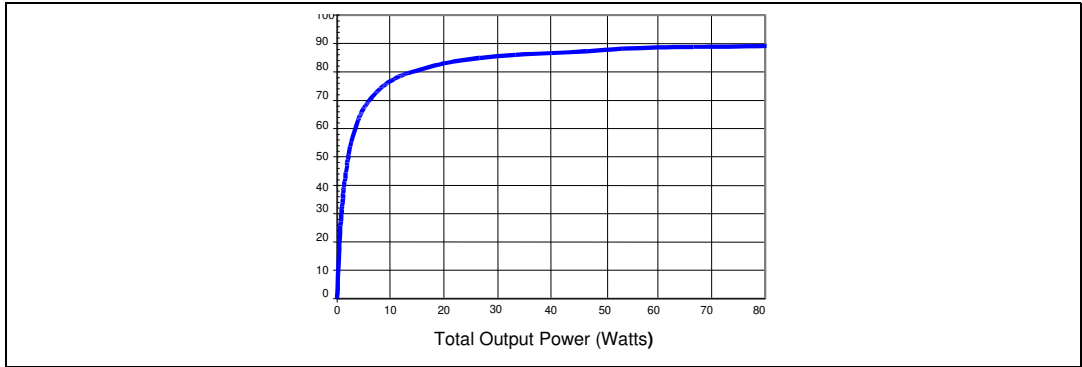


Figure 17. Typical frequency response

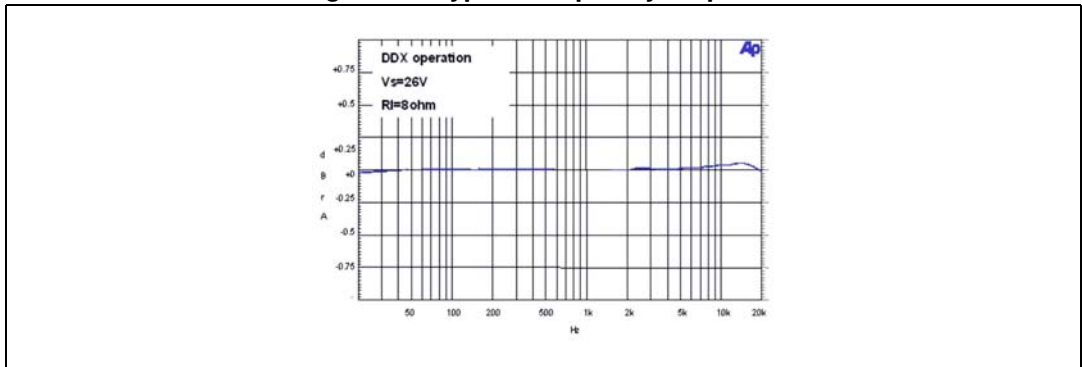


Figure 18. FFT -60 dB, 1 kHz output

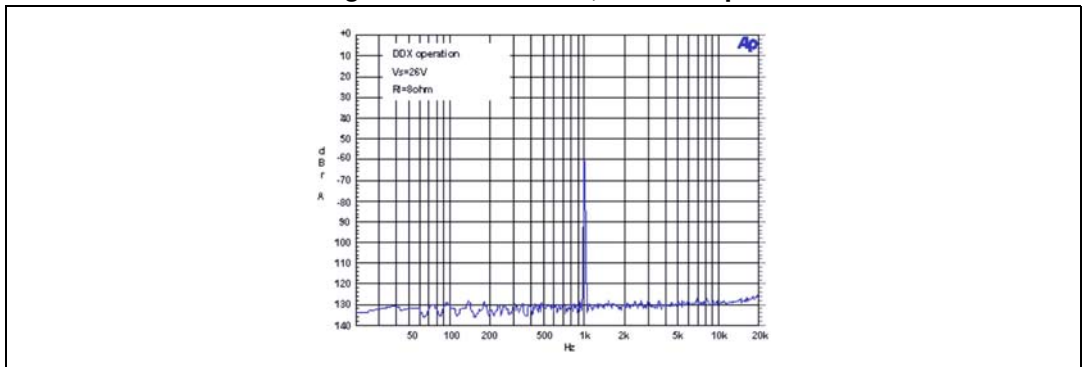
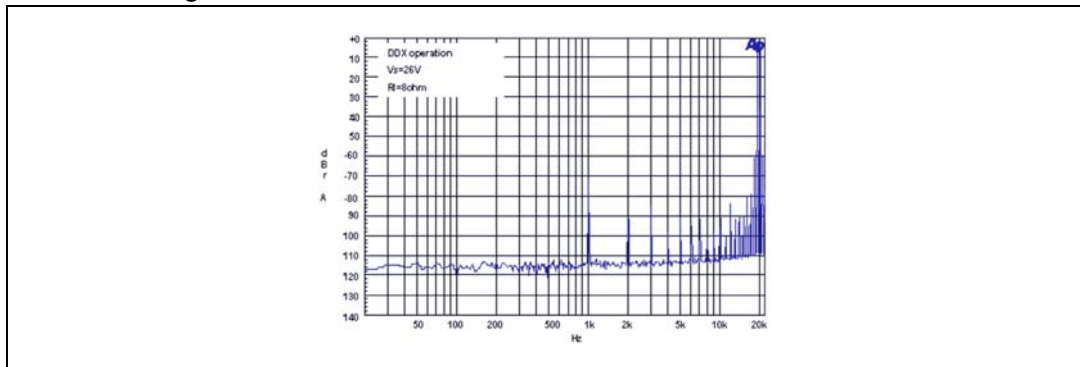


Figure 19. FFT inter-modulation distortion 19 kHz and 20 kHz



5.2.2 Stereo mode, operation with $V_{CC} = 18.5 V$

Figure 20. Frequency response, 1 W, BTL, 8 Ω

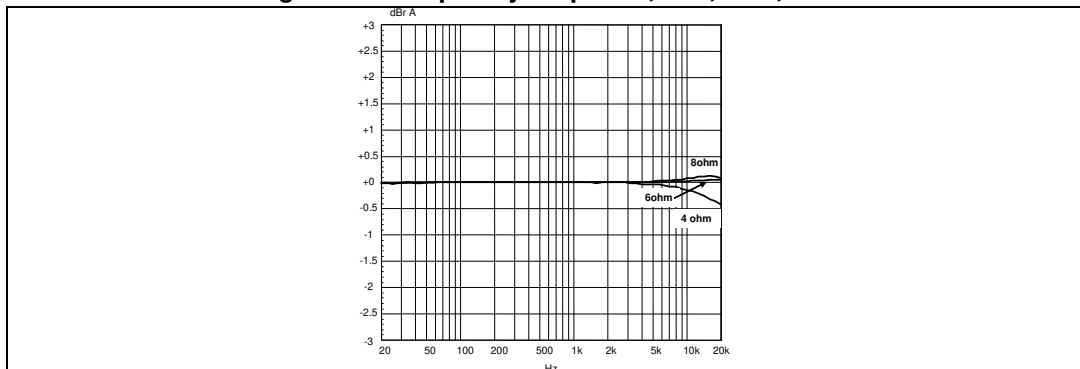


Figure 21. Channel separation, 1 W, BTL stereo mode

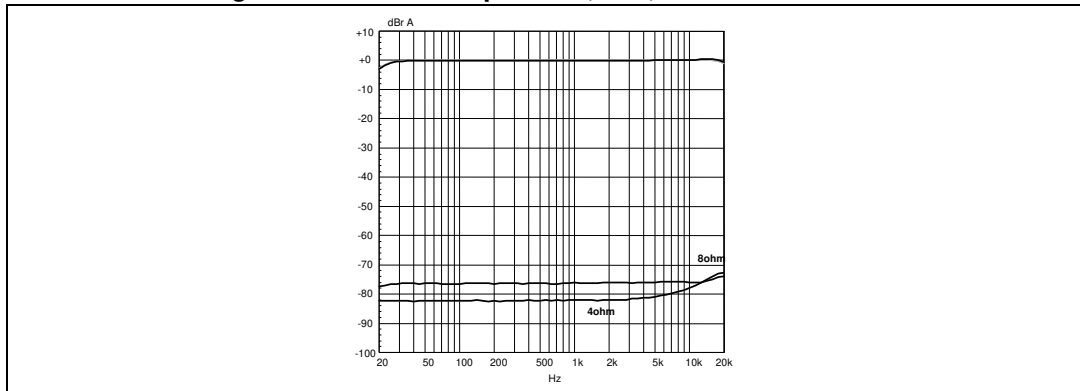


Figure 22. THD vs. output power, BTL, 1 kHz

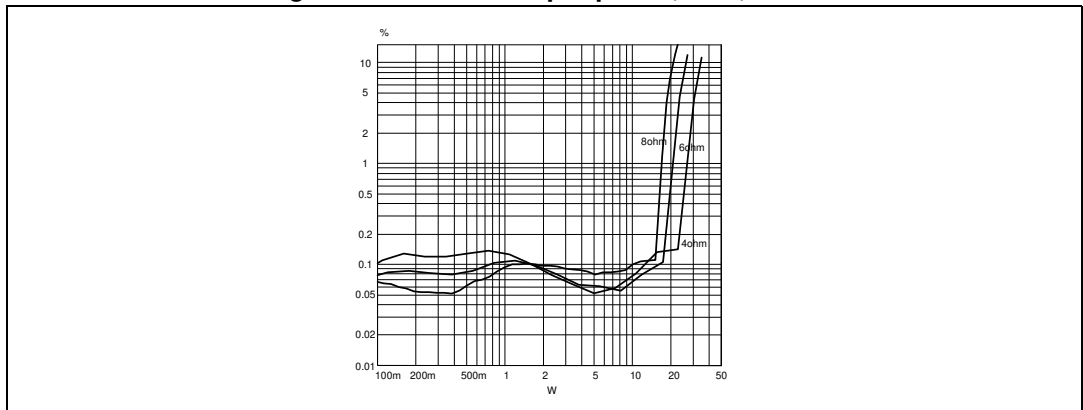


Figure 23. THD vs. frequency, 1 W output, stereo mode

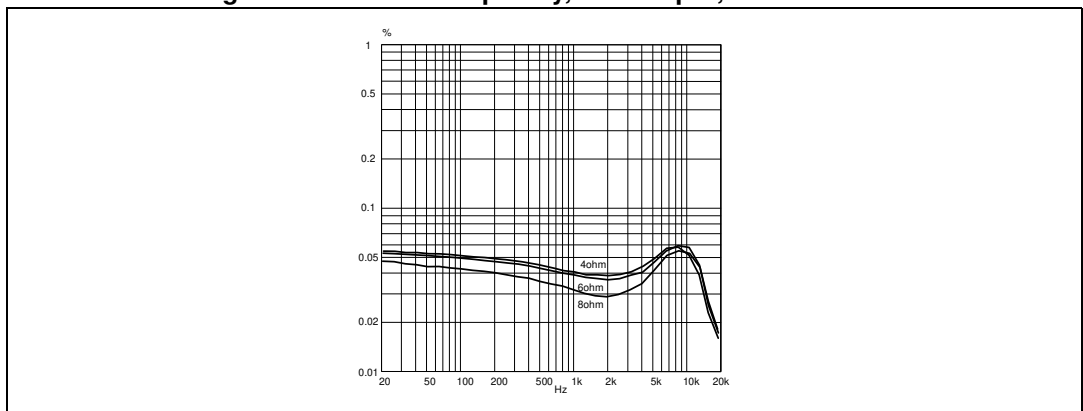


Figure 24. THD vs. frequency, BTL, 16 W output

