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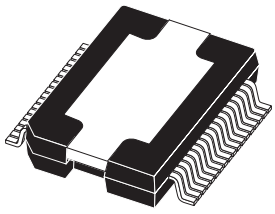
STA326

2.1-channel high-efficiency digital audio system

Datasheet - production data



PowerSO-36
with exposed pad up

Features

- Wide supply voltage range (10 V - 36 V)
- Three power output configurations
  - 2 x 40 W + 1 x 80 W
  - 2 x 80 W
  - 1 x 160 W
- PowerSO-36 package (exposed pad up (EPU))
- 2.1 channels of 24-bit DDX®
- 100-dB SNR and dynamic range
- 32 kHz to 192 kHz input sample rates
- Digital gain/attenuation +48 dB to -80 dB in 0.5-dB steps
- Four 28-bit user-programmable biquads (EQ) per channel
- I^2C control
- 2-channel I^2S input data interface
- Individual channel and master gain/attenuation
- Individual channel and master soft/hard mute
- Individual channel volume and EQ bypass
- Bass/treble tone control
- Dual independent programmable limiters/compressors
- Automodes
  - 32 preset EQ curves
  - 15 preset crossover settings
  - Auto volume-controlled loudness
  - 3 preset volume curves
  - 2 preset anti-clipping modes
  - Preset nighttime listening mode
  - Preset TV AGC
- Input and output channel mapping
- AM noise-reduction and PWM frequency-shifting modes
- Software volume update and muting
- Auto zero detect and invalid input detect muting
- Selectable DDX® ternary or binary PWM output + variable PWM speeds
- Selectable de-emphasis
- Post-EQ user-programmable mix with default 2.1 bass-management settings
- Variable max power correction for lower full-power THD
- Four output routing configurations
- Selectable clock input ratio
- 96 kHz internal processing sample rate, 24 to 28-bit precision
- Video application supports 576 * fs input mode

Table 1. Device summary

Order code	Package	Packaging
STA32613TR	PowerSO-36 EPU	Tape and reel

Contents

List of tables

List of figures

1 Description

The STA326 comprises digital audio processing, digital amplifier control and DDX® power output stage to create a high-power single-chip DDX® solution for high-quality, high-efficiency, all-digital amplification.

The STA326 power section consists of four independent half-bridges. These can be configured via digital control to operate in different modes. 2.1 channels can be provided by two half-bridges and a single full-bridge to give up to 2 x 40 W plus 1 x 80 W of power output. Two channels can be provided by two full-bridges to give up to 2 x 80 W of power. The IC can also be configured as a single parallel full-bridge capable of high-current operation and 1 x 160 W output.

Also provided in the STA326 is a full assortment of digital processing features. This includes up to four programmable 28-bit biquads (EQ) per channel and bass/treble tone control. Automodes enable a time-to-market advantage by substantially reducing the amount of software development needed for certain functions. This includes auto volume loudness, preset volume curves, preset EQ settings and new advanced AM radio-interference reduction modes.

The serial audio data input interface accepts all possible formats, including the popular I^2S format.

Three channels of DDX® processing are provided. This high-quality conversion from PCM audio to patented DDX® 3-state PWM switching provides over 100 dB of SNR and dynamic range.

Figure 1. Block diagram

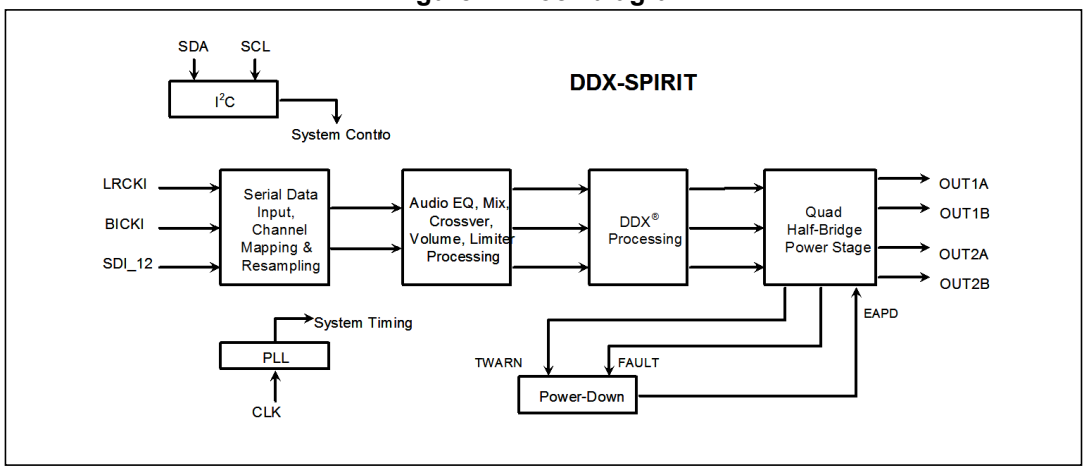
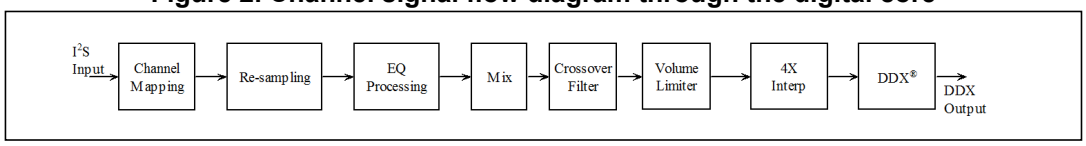


Figure 2. Channel signal flow diagram through the digital core



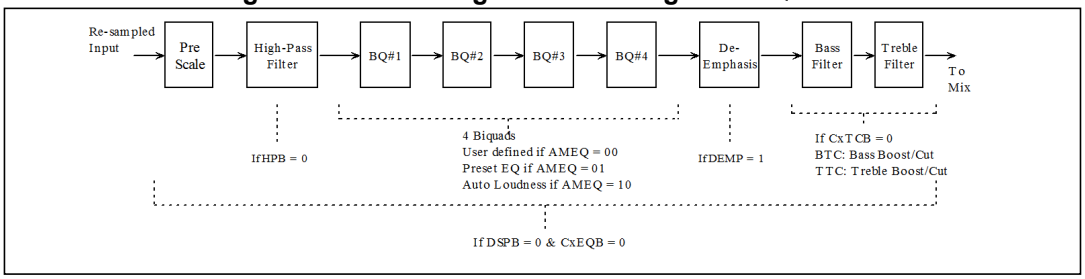
1.1 EQ processing

Two channels of input data (re-sampled if necessary) at 96 kHz are provided to the EQ processing block. In this block, up to four user-defined biquads can be applied to each of the two channels.

Prescaling, DC-blocking, high-pass, de-emphasis, bass, and tone control filters can also be applied based on various configuration parameter settings.

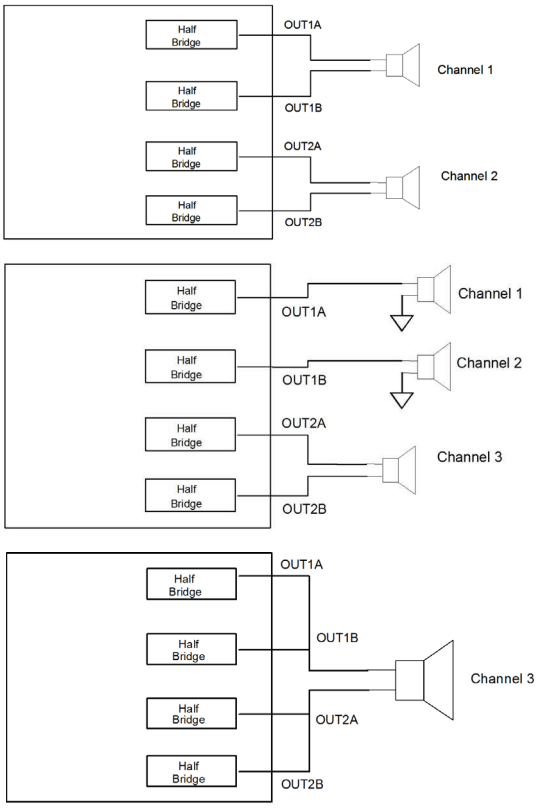
The entire EQ block can be bypassed for all channels simultaneously by setting the DSPB bit to 1. And the CxEQBP bits can be used to bypass the EQ function on a per channel basis. *Figure 3* shows the internal signal flow through the EQ block.

Figure 3. Channel signal flow through the EQ block



1.2 Output configurations

Figure 4. Output power-stage configurations



2-channel (full-bridge) configuration, register bits OCFG[1:0] = 00

2.1-channel configuration, register bits OCFG[1:0] = 01

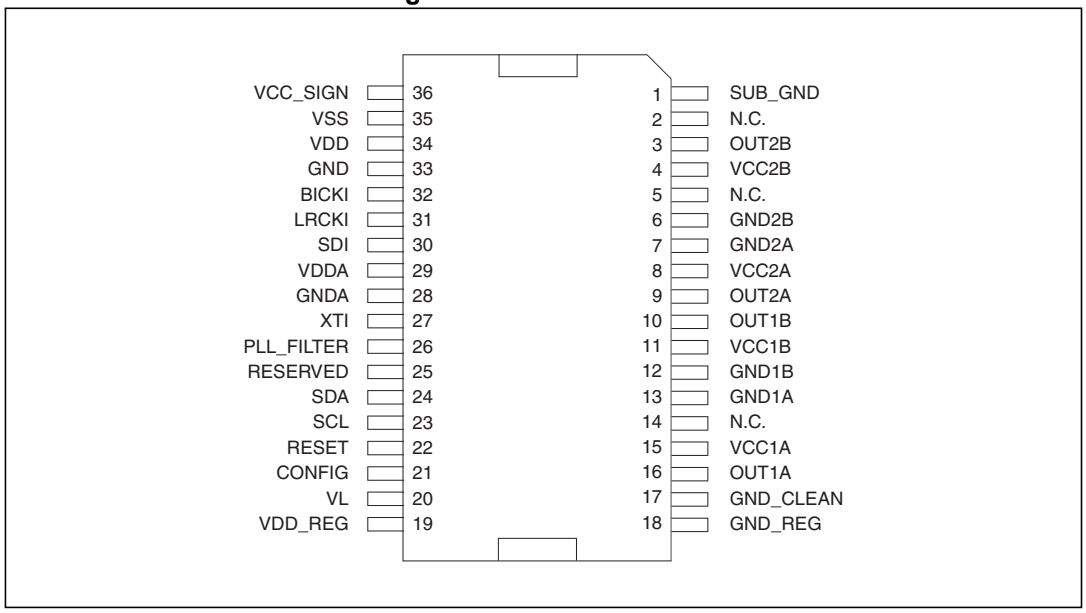
1-channel mono-parallel configuration, register bits OCFG[1:0] = 11

The setup register is *Configuration register F (addr 0x05) on page 34*

2 Pin out

2.1 Package pins

Figure 5. Pin connections



2.2 Pin list

Table 2. Pin list

Number	Type	Name	Description
1	I/O	SUB_GND	Substrate ground
2	N.C.	N.C.	Not connected
3	O	OUT2B	Output half bridge 2B
4	I/O	VCC2B	Positive supply
5	N.C.	N.C.	Not connected
6	I/O	GND2B	Negative supply
7	I/O	GND2A	Negative supply
8	I/O	VCC2A	Positive supply
9	O	OUT2A	Output half bridge 2A
10	O	OUT1B	Output half bridge 1B
11	I/O	VCC1B	Positive supply
12	I/O	GND1B	Negative supply
13	I/O.	GND1A	Negative supply
14	N.C.	N.C.	Not connected

Table 2. Pin list

Number	Type	Name	Description
15	I/O	VCC1A	Positive supply
16	O	OUT1A	Output half bridge 1A
17	I/O	GND_CLEAN	Logical ground
18	I/O	GND_REG	Regulated ground
19	I/O	VDD_REG	Logic supply
20	I/O	VL	Logic supply
21	I	CONFIG	Logic levels
22	I	RESET	Reset
23	I	SCL	I^2C serial clock
24	I/O	SDA	I^2C serial data
25	RES	RESERVED	This pin must be connected to GND
26	I	PLL_FILTER	Connection to PLL filter
27	I	XTI	PLL input clock
28	I/O	GNDA	Analog ground
29	I/O	VDDA	Analog supply, nominally 3.3 V
30	I	SDI	I^2S serial data channels 1 & 2
31	I/O	LRCKI	I^2S left/right clock,
32	I	BICKI	I^2S serial clock
33	I/O	GND	Digital ground
34	I/O	VDD	Digital supply, nominally 3.3 V
35	I/O	VSS	5 V regulator referred to +
36	I/O	VCC_SIGN	5 V regulator referred to ground

2.3 Pin description

OUT1A, 1B, 2A and 2B (pins 16, 10, 9 and 3)

Output half bridge PWM outputs 1A, 1B, 2A and 2B provide the input signals to the speakers.

CONFIG (pin 21)

The configuration input pin is normally connected to ground. Using the mono high power BTL configuration requires the CONFIG input pin to be shorted to VDD_REG.

RESET (pin 22)

Driving RESET low sets all outputs low and returns all register settings to their default (reset) values. The reset is asynchronous to the internal clock.

I^2C signals (pins 23 and 24)

The SDA (I^2C Data) and SCL (I^2C Clock) pins operate according to the I^2C specification (*Chapter 6 on page 19* gives more information). Fast-mode (400 kB/s) I^2C communication is supported.

GNDA and VDDA (pins 28 and 29)

This is the 3.3 V analog supply for the phase locked loop. It must be well decoupled and filtered for good noise immunity since the audio performance of the device depends upon the PLL circuit.

CLK (pin 27)

This is the master clock in used by the digital core. The master clock must be an integer multiple of the LR clock frequency. Typically, the master clock frequency is 12.288 MHz (256 * fs) for a 48 kHz sample rate; it is the default setting at power-up. Care must be taken to provide the device with the nominal system clock frequency; over-clocking the device may result in anomalous operation, such as inability to communicate.

FILTER_PLL (pin 26)

This is the connection for external filter components for the PLL loop compensation. The schematic diagram in *Figure 21 on page 57* shows the recommended circuit.

BICKI (pin 32)

The serial or bit clock input is for framing each data bit. The bit clock frequency is typically 64 * fs using I^2S serial format.

SDI_12 (pin 30)

This is the serial data input where PCM audio information enters the device. Six format choices are available including I^2S, left or right justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

LRCKI (pin 31)

The left/right clock input is for data word framing. The clock frequency is at the input sample rate, fs.

3 Electrical specifications

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD33}	3.3 V I/O power supply (pins VDDA, VDD)	-0.5 to 4	V
V_i	Voltage on input pins	-0.5 to (V_{DD33} + 0.5)	V
V_o	Voltage on output pins	-0.5 to (V_{DD33} + 0.5)	V
T_{stg}	Storage temperature	-40 to +150	°C
T_{amb}	Ambient operating temperature	-20 to +85	°C
	DC supply voltage (pins nA, nB)	40	V
V_{MAX}	Maximum voltage on VL (pin 20)	5.5	V

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{thj\text{-}case}$	Thermal resistance junction to case (thermal pad)	-	-	2.5	°C/W
$T_{j\text{-}SD}$	Thermal shut-down junction temperature	-	150	-	°C
T_{WARN}	Thermal warning temperature	-	130	-	°C
$T_{h\text{-}SD}$	Thermal shut-down hysteresis	-	25	-	°C

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{DD33}	I/O power supply	3.0 to 3.6	V
T_j	Operating junction temperature	-20 to +125	°C

3.1 General interface specifications

Operating conditions V_{DD33} = 3.3 V ±0.3 V, T_{amb} = 25° C unless otherwise specified

Table 6. General interface electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{il}	Low level input no pull-up	V_i = 0 V (1)	-	-	1	µA
I_{ih}	High level input no pull-down	$V_i = V_{DD33}$ (1)	-	-	2	µA
I_{OZ}	3-state output leakage without pull-up/down	$V_i = V_{DD33}$ (1)	-	-	2	µA
V_{esd}	Electrostatic protection (human-body model)	Leakage current < 1 µA	2000	-	-	V

1. The leakage currents are generally very small (< 1 nA). The values given here are the maximum values after an electrostatic stress on the pin.

3.2 DC electrical specifications (3.3 V buffers)

Operating conditions V_{DD33} = 3.3 V ±0.3 V, T_{amb} = 25° C unless otherwise specified

Table 7. DC electrical specifications

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	-	-	-	0.8	V
V_{IH}	High level input voltage	-	2.0	-	-	V
V_{hyst}	Schmitt trigger hysteresis	-	0.4	-	-	V
V_{ol}	Low level output	Iol = 2 mA	-	-	0.15	V
V_{oh}	High level output	Ioh = -2 mA	V_{DD33} - 0.15	-	-	V

3.3 Power electrical specifications

Operating conditions V_{DD33} = 3.3 V ±0.3 V, V_L = 3.3 V, = 30 V, T_{amb} = 25° C unless otherwise specified.

Table 8. Power electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{dsON}	Power Pchannel/Nchannel MOSFET RdsON	Id = 1A	-	200	270	mΩ
I_{dss}	Power Pchannel/Nchannel leakage Idss	= 35 V	-	-	50	µA
g_N	Power Pchannel RdsON matching	Id = 1 A	95	-	-	%
g_P	Power Nchannel RdsON matching	Id = 1 A	95	-	-	%
Dt_s	Low current dead time (static)	See test circuits, *Figure 6* and *Figure 7*	-	10	20	ns
$t_{d\ ON}$	Turn-on delay time	Resistive load	-	-	100	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load	-	-	100	ns
t_r	Rise time	Resistive load, *Figure 6* and *Figure 7*	-	-	25	ns
t_f	Fall time	Resistive load, *Figure 6* and *Figure 7*	-	-	25	ns
	Supply voltage	-	10	-	36	V
V_L	Low logical state voltage VL	V_L = 3.3 V	0.8	-	-	V
V_H	High logical state voltage VH	V_L = 3.3 V	-	-	1.7	V
I_{-PWRDN}	Supply current from in PWRDN	Pin PWRDN = 0 V	-	-	3	mA
I_{-hiz}	Supply current from in 3-state	= 30 V, 3-state	-	22	-	mA

Table 8. Power electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I	Supply current from in operation (both channel switching)	Input pulse width = 50% duty, switching frequency = 384 kHz, no LC filters	-	80	-	mA
I_{out-sh}	Overcurrent protection threshold (short circuit current limit)	-	4.5	6	-	A
V_{UV}	Undervoltage protection threshold	-	-	7	-	V
t_{pw-min}	Output minimum pulse width	No load	70		150	ns
P_o	Output power (refer to test circuit	THD = 10% R_L = 4 Ω = 21 V R_L = 8 Ω = 36 V	- -	50 80	- -	W
P_o	Output power (refer to test circuit	THD = 1% R_L = 4 Ω = 21 V R_L = 8 Ω = 36 V	- -	40 62	- -	W

Figure 6. Test circuit 1

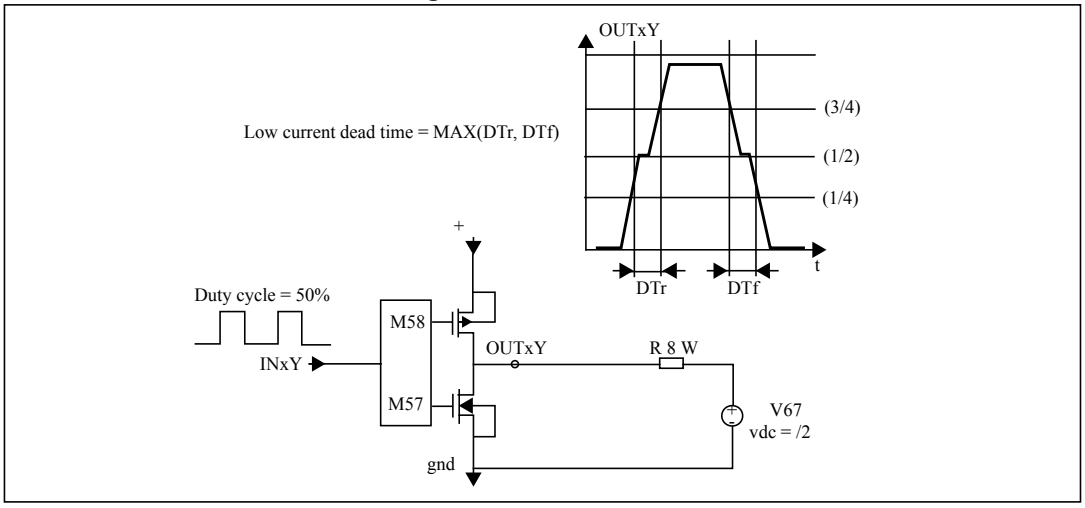
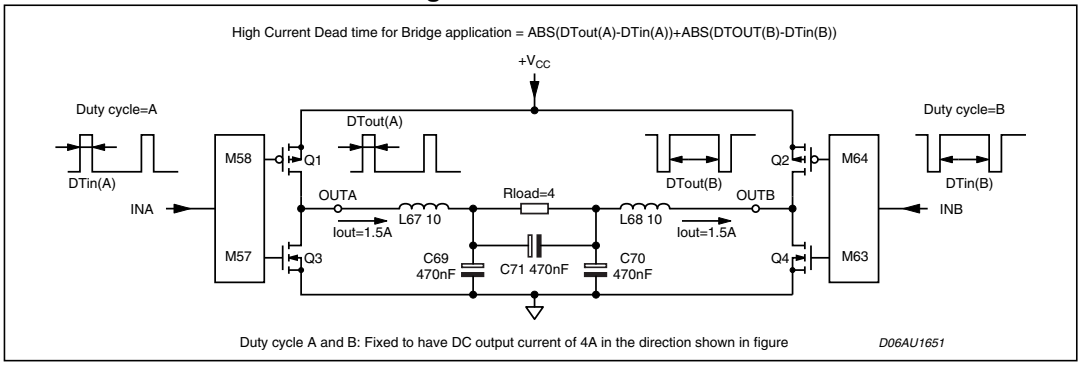


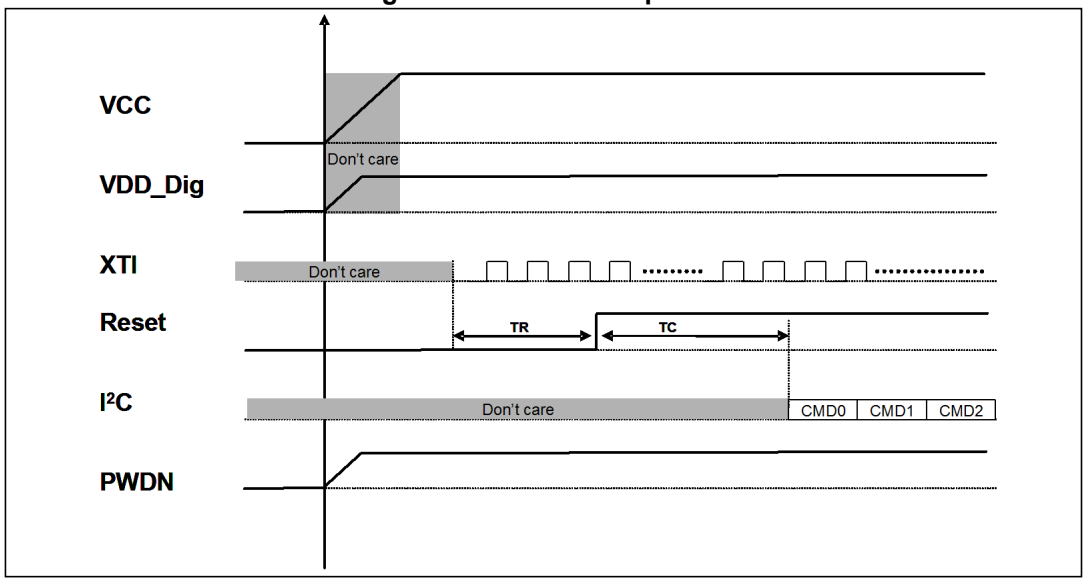
Figure 7. Test circuit 2



4 Power supply and control sequencing

The recommended power-on/off sequences are shown in *Figure 8* and *Figure 9*.

Figure 8. Power-on sequence



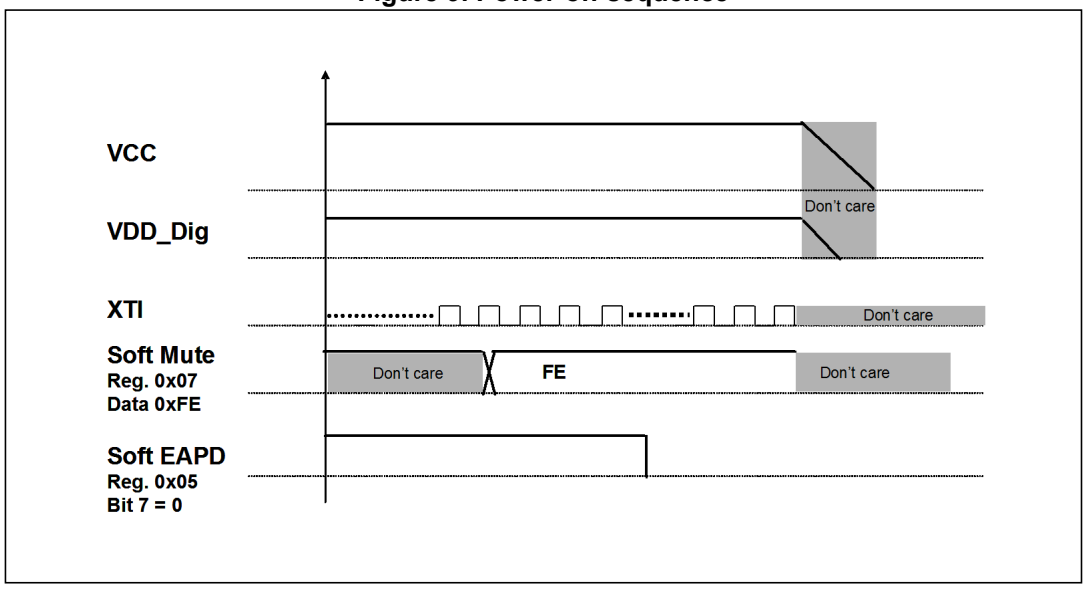
Note: 1. TR = minimum time between XTI master clock stable and Reset removal: 1 msec

2. TC = minimum time between Reset removal and I^2C program, sequence start: 1msec

3. A stable clock means: f_{max} - f_{min} < 1 MHz

4. No specific VCC and VDD_Dig turn–on sequence is required

Figure 9. Power-off sequence



5. No specific VCC and VDD_Dig turn–off sequence is required

6. This sequence ensures a pop-free turn-off

5 Characterization curves

Figure 10. Channel separation vs. frequency

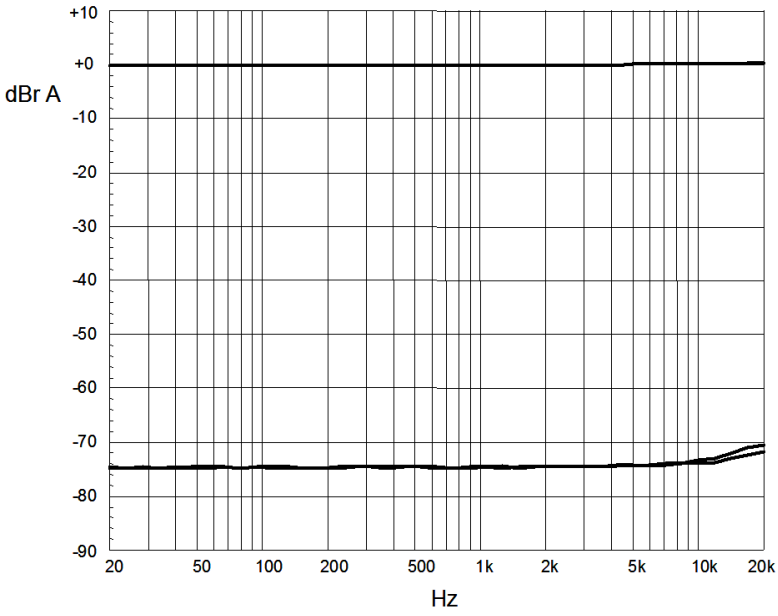


Figure 11. THD vs. output power - single ended

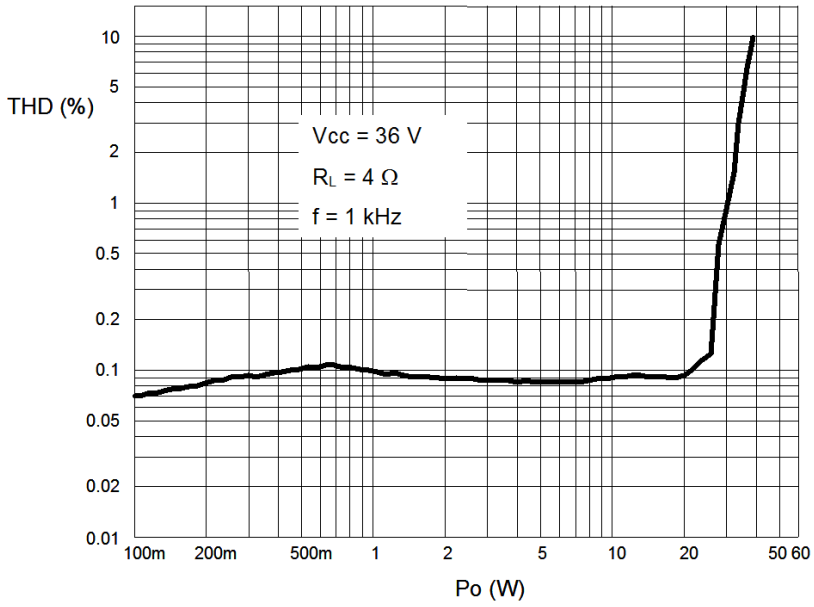


Figure 12. THD vs. output power - BTL

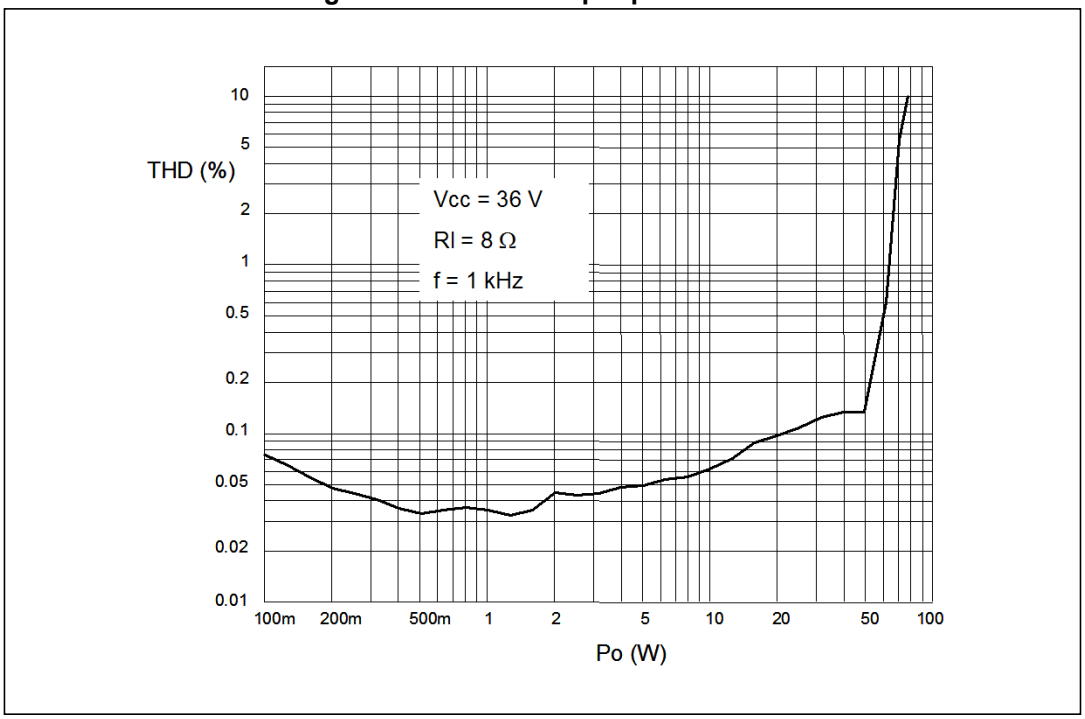
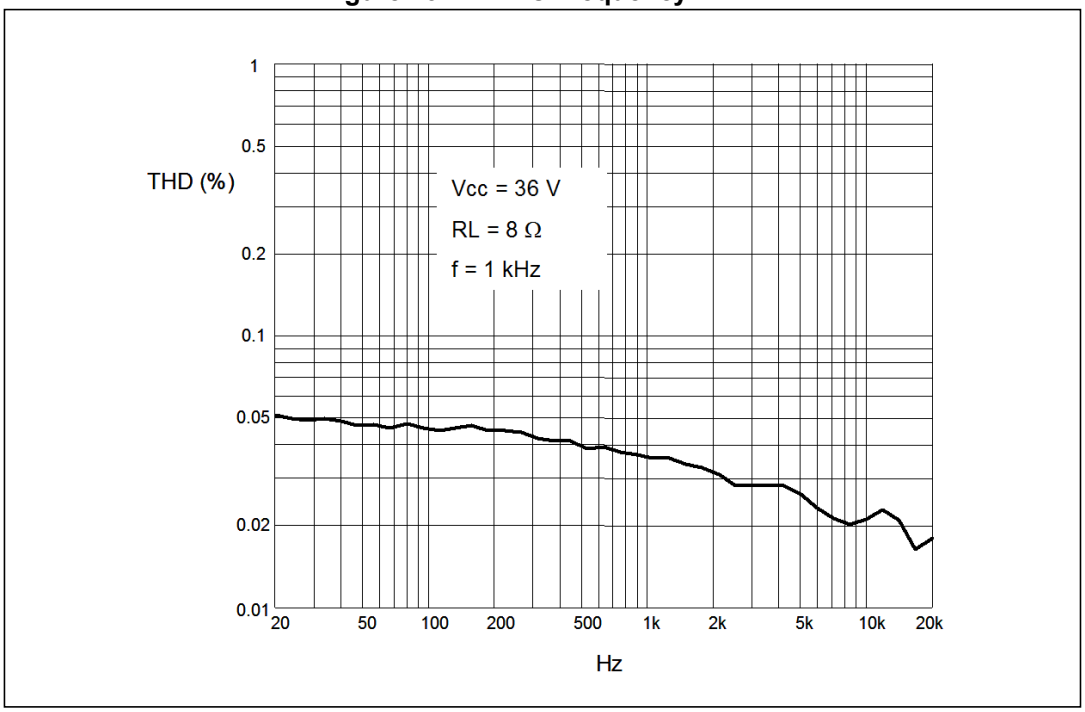


Figure 13. THD vs. frequency - BTL



6 I²C bus specification

The STA326 supports the I²C protocol. This protocol defines any device that sends data on to the I²C bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA326 is always a slave device in all of its communications.

6.1 Communication protocol

Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

Start condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

Stop condition

STOP is identified by a low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between STA326 and the bus master.

Data input

During the data input the STA326 samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

6.2 Device addressing

To start communication between the master and the STA326, the master must initiate with a start condition. Following this, the master sends 8 bits (MSB first) onto the SDA line corresponding to the device select address and read or write mode.

The 7 MSBs are the device address identifiers, corresponding to the I²C bus definition. The STA326 device address is 0x34.

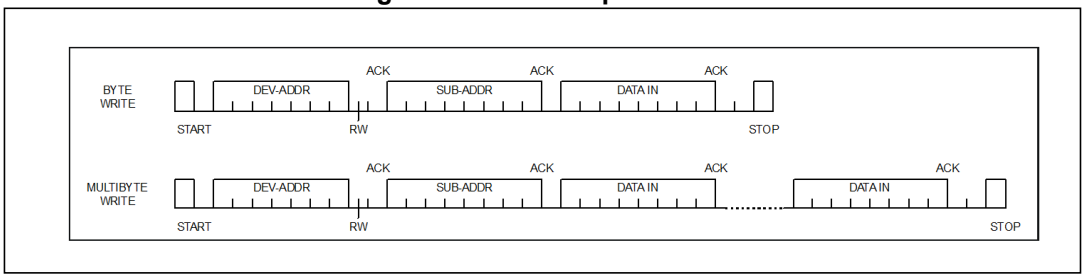
The 8th bit (LSB) identifies read or write operation, RW. This bit is set to 1 in read mode and 0 for write mode. After a START condition the STA326 identifies the device address on the bus. If a match is found, it acknowledges the identification on the SDA bus during the 9th bit time. The byte following the device identification byte is the internal space address.

6.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA326 acknowledges this and then the master writes the internal address byte.

After receiving the internal byte address the STA326 again responds with an acknowledgement.

Figure 14. I²C write procedure



Byte write

In the byte write mode the master sends one data byte. This is acknowledged by the STA326. The master then terminates the transfer by generating a STOP condition.

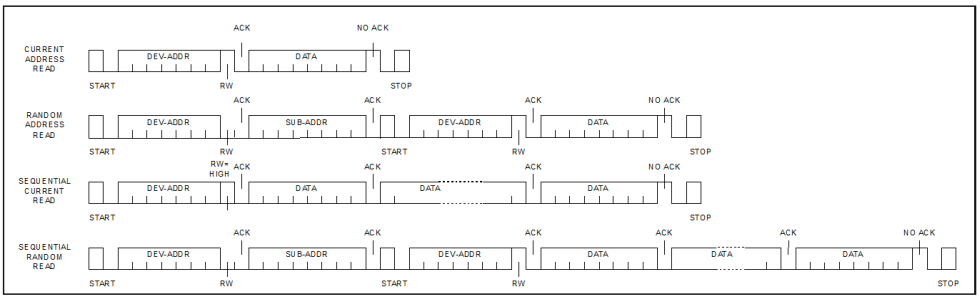
Multi-byte write

The multi-byte write modes can start from any internal address. Sequential data byte writes will be written to sequential addresses within the STA326.

The master generating a STOP condition terminates the transfer.

6.4 Read operation

Figure 15. I²C read procedure



Current address byte read

Following the START condition the master sends a device select code with the RW bit set to 1. The STA326 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes will be read from sequential addresses within the STA326. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

Random address byte read

Following the START condition the master sends a device select code with the RW bit set to 0. The STA326 acknowledges this and then the master writes the internal address byte. After receiving, the internal byte address the STA326 again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA326 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

Random address multi-byte read

The multi-byte read modes could start from any internal address. Sequential data bytes will be read from sequential addresses within the STA326. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

7 Register description

You must not reprogram the register bits marked “Reserved”. It is important that these bits keep their default reset values.

Table 9. Register summary

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	CONFA	FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0x01	CONFB	C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	CONFC	Reserved	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x03	CONFD	MME	ZDE	DRC	BQL	PSL	DSPB	DEMP	HPB
0x04	CONFE	SVE	ZCE	Reserved	PWMS	AME	Reserved	MPC	MPCV
0x05	CONFF	EAPD	PWDN	ECLE	Reserved	BCLE	IDE	OCFG1	OCFG0
0x06	MMUTE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MMUTE
0x07	MVOL	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x08	C1VOL	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x09	C2VOL	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0A	C3VOL	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0x0B	AUTO1	AMPS	Reserved	AMGC1	AMGC0	AMV1	AMV0	AMEQ1	AMEQ0
0x0C	AUTO2	XO3	XO2	XO1	XO1	AMAM2	AMAM1	AMAM0	AMAME
0x0D	AUTO3	Reserved	Reserved	Reserved	PEQ4	PEQ3	PEQ2	PEQ1	PEQ0
0x0E	C1CFG	C1OM1	C1OM0	C1LS1	C1LS0	C1BO	C1VBP	C1EQBP	C1TCB
0x1F	C2CFG	C2OM1	C2OM0	C2LS1	C2LS0	C2BO	C2VBP	C2EQBP	C2TCB
0x10	C3CFG	C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VBP	Reserved	Reserved
0x11	TONE	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0x12	L1AR	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x13	L1ATRT	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0x14	L2AR	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0x15	L2ATRT	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0x16	CFADDR2	CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0x17	B1CF1	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0x18	B1CF2	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0x19	B1CF3	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0x1A	B2CF1	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0x1B	B2CF2	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0x1C	B2CF3	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0x1D	A1CF1	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16

Table 9. Register summary (continued)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x1E	A1CF2	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0x1F	A1CF3	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0x20	A2CF1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0x21	A2CF2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0x22	A2CF3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0x23	B0CF1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0x24	B0CF2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0x25	B0CF3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0x26	CFUD	Reserved	Reserved	Reserved	Reserved	RA	R1	WA	W1
0x27	MPCC1	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x28	MPCC2	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x29	Reserved	1	1	1	1	0	0	1	1
0x2A	Reserved	0	0	1	1	0	0	1	1
0x2B	FDRC1	FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0x2C	FDRC2	FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0x2D	Status	PLLUL	Reserved	Reserved	Reserved	Reserved	Reserved	FAULT	TWARN

7.1 Configuration register A (addr 0x00)

D7	D6	D5	D4	D3	D2	D1	D0
FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0	1	1	0	0	0	1	1

Table 10. Master clock select

Bit	R/W	RST	Name	Description
0	RW	1	MCS0	Master clock select: Selects the ratio between the input I^2S sample frequency and the input clock.
1	RW	1	MCS1	-
2	RW	0	MCS2	-

The STA326 will support sample rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz and 192 kHz. Therefore the internal clock will be:

- 32.768 MHz for 32 kHz
- 45.1584 MHz for 44.1 kHz, 88.2 kHz, and 176.4 kHz
- 49.152 MHz for 48 kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency (fs). The correlation between the input clock and the input sample rate is determined by the status of the MCSx bits and the IR (input rate) register bits. The MCSx

bits determine the PLL factor generating the internal clock and the IR bit determines the oversampling ratio used internally.

Table 11. IR and MCS settings for input sample rate and clock rate

Input sample rate *fs* (kHz)	IR	MCS[2:0]					
		000	001	010	011	100	101
32, 44.1, 48	00	768 fs	512 fs	384 fs	256 fs	128 fs	576 fs
88.2, 96	01	384 fs	256 fs	192 fs	128 fs	64 fs	-
176.4, 192	1X	384 fs	256 fs	192 fs	128 fs	64 fs	-

Table 12. Interpolation ratio select

Bit	R/W	RST	Name	Description
4:3	RW	00	IR[1:0]	Interpolation ratio select: selects internal interpolation ratio based on input I^2S sample frequency

The STA326 has variable interpolation (re-sampling) settings such that internal processing and DDX® output rates remain consistent. The first processing block interpolates by either 2 times or 1 time (pass-through) or provides a downsample by a factor of 2.

The IR bits determine the re-sampling ratio of this interpolation.

Table 13. IR bit settings as a function of input sample rate

Input sample rate fs (kHz)	IR[1,0]	1st stage interpolation ratio
32	00	2 times oversampling
44.1	00	2 times oversampling
48	00	2 times oversampling
88.2	01	Pass-through
96	01	Pass-through
176.4	10	Downsampling by 2
192	10	Downsampling by 2

Table 14. Thermal warning recovery bypass

Bit	R/W	RST	Name	Description
5	RW	1	TWRB	Thermal warning recovery bypass: 0: thermal warning recovery enabled 1: thermal warning recovery disabled

If the thermal warning adjustment is enabled (TWAB = 0), then the thermal warning recovery will determine if the adjustment is removed when thermal warning is negative. If TWRB = 0 and TWAB = 0, then when a thermal warning disappears the gain adjustment determined by the thermal warning postscale (default = -3 dB) will be removed and the gain will be added back to the system. If TWRB = 1 and TWAB = 0, then when a thermal warning

disappears the thermal warning postscale gain adjustment will remain until TWRB is changed to zero or the device is reset.

Table 15. Thermal warning adjustment bypass

Bit	R/W	RST	Name	Description
6	RW	1	TWAB	Thermal warning adjustment bypass: 0: thermal warning adjustment enabled 1: thermal warning adjustment disabled

The on-chip STA326 power output block provides feedback to the digital controller using inputs to the power control block. The TWARN input is used to indicate a thermal warning condition. When TWARN is asserted (set to 0) for a period greater than 400 ms, the power control block will force an adjustment to the modulation limit in an attempt to eliminate the thermal warning condition. Once the thermal warning volume adjustment is applied, whether the gain is reapplied when TWARN is de-asserted is dependent on the TWRB bit.

Table 16. Fault detect recovery bypass

Bit	R/W	RST	Name	Description
7	RW	0	FDRB	Fault detector recovery bypass: 0: fault detector recovery enabled 1: fault detector recovery disabled

The DDX® power block can provide feedback to the digital controller using inputs to the power control block. The FAULT input is used to indicate a fault condition (either over-current or thermal). When FAULT is asserted (set to 0), the power control block will attempt a recovery from the fault by asserting the 3-state output (setting it to 0 which directs the power output block to begin recovery). It holds it at 0 for period of time in the range of 0.1 ms to 1 s as defined by the fault-detect recovery constant register (FDRC registers 0x29 to 0x2A), then toggle it back to 1. This sequence is repeated as log as the fault indication exists. This feature is enabled by default but can be bypassed by setting the FDRB control bit to 1.