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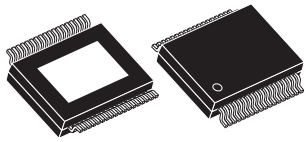
STA333W

2 channel high-efficiency digital audio system Sound Terminal™

Datasheet - production data



PowerSSO-36 package
with exposed pad down (EPD)

Features

- Wide supply-voltage range (4.5 V - 20 V)
- 2 power output configurations
  - 2 channels of binary PWM (stereo mode)
  - 2 channels of ternary PWM (stereo mode)
- PowerSSO-36 with exposed pad down
- 2 channels of 24-bit DDX®
- 100-dB SNR and dynamic range
- Selectable 32- to 192-kHz input sample rates
- I²C control with selectable device address
- Digital gain -80 dB to +48 dB in 0.5-dB steps
- Software volume update
- Individual channel and master gain/attenuation
- Individual channel and master software and hardware mute
- Independent channel volume bypass
- Automatic zero-detect mute
- Automatic invalid input detect mute
- 2-channel I²S input data Interface
- Selectable clock input ratio
- Input channel mapping
- Automatic volume control for limiting maximum power
- 96-kHz internal processing sample rate, 24-bit precision
- Advanced AM interference frequency switching and noise suppression modes
- Thermal-overload and short-circuit protection embedded
- Video application: 576 * f_S input mode support

Applications

- LCD
- DVD
- Cradle
- Digital speaker
- Wireless-speaker cradle

Description

The STA333W is an integrated circuit comprising digital audio processing, digital amplifier control and DDX® power output stage to create a high-power, single-chip DDX® solution for all-digital amplification with high quality and high efficiency.

The STA333W power section consists of four independent half-bridges stages. These can be configured via digital control to operate in different modes. 2 channels can be provided by two full bridges, providing up to 20 W + 20 W of power.

Also provided in the STA333W are new advanced AM radio interference reduction modes. The serial audio data input interface accepts all possible formats, including the popular I²S format. Three channels of DDX® processing are provided.

The STA333W is part of the Sound Terminal™ family that provides full digital audio streaming to the speaker offering cost effectiveness, low power dissipation and sound enrichment.

Table 1. Device summary

Order code	Package	Packaging
STA333W13TR	PowerSSO-36 EPD	Tape and reel

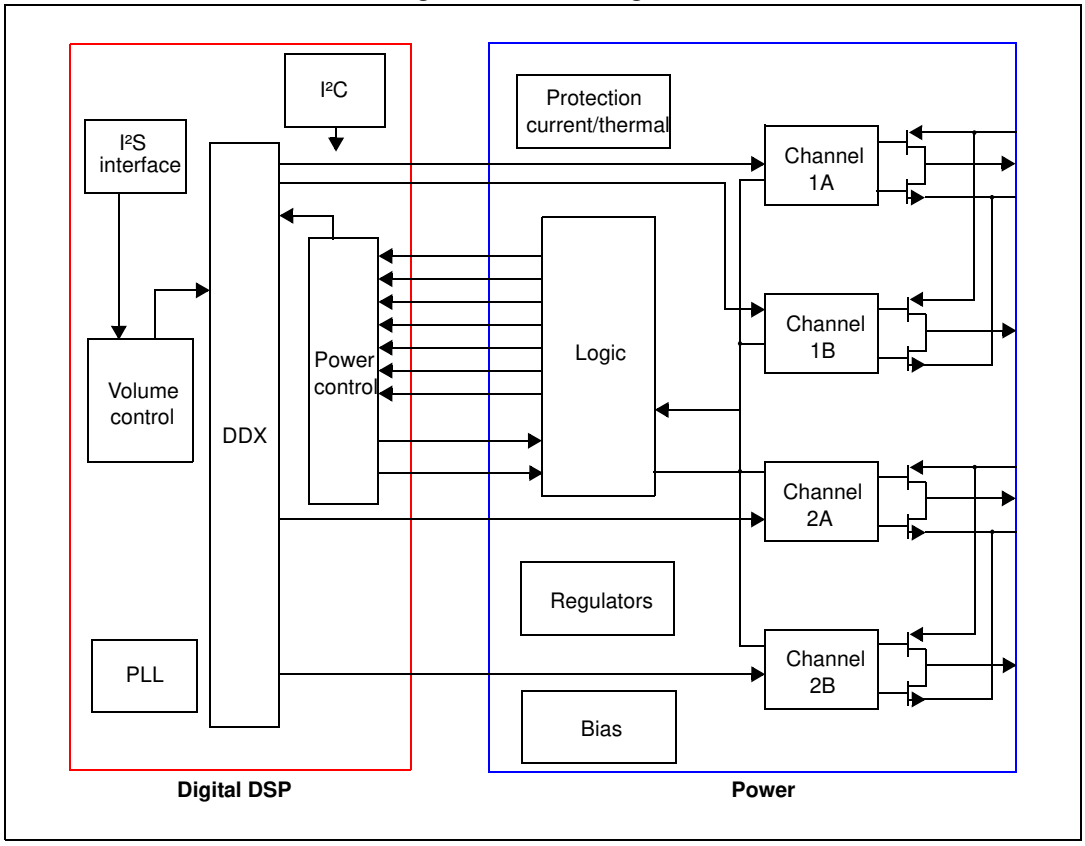
Contents

List of tables

List of figures

1 Block diagram

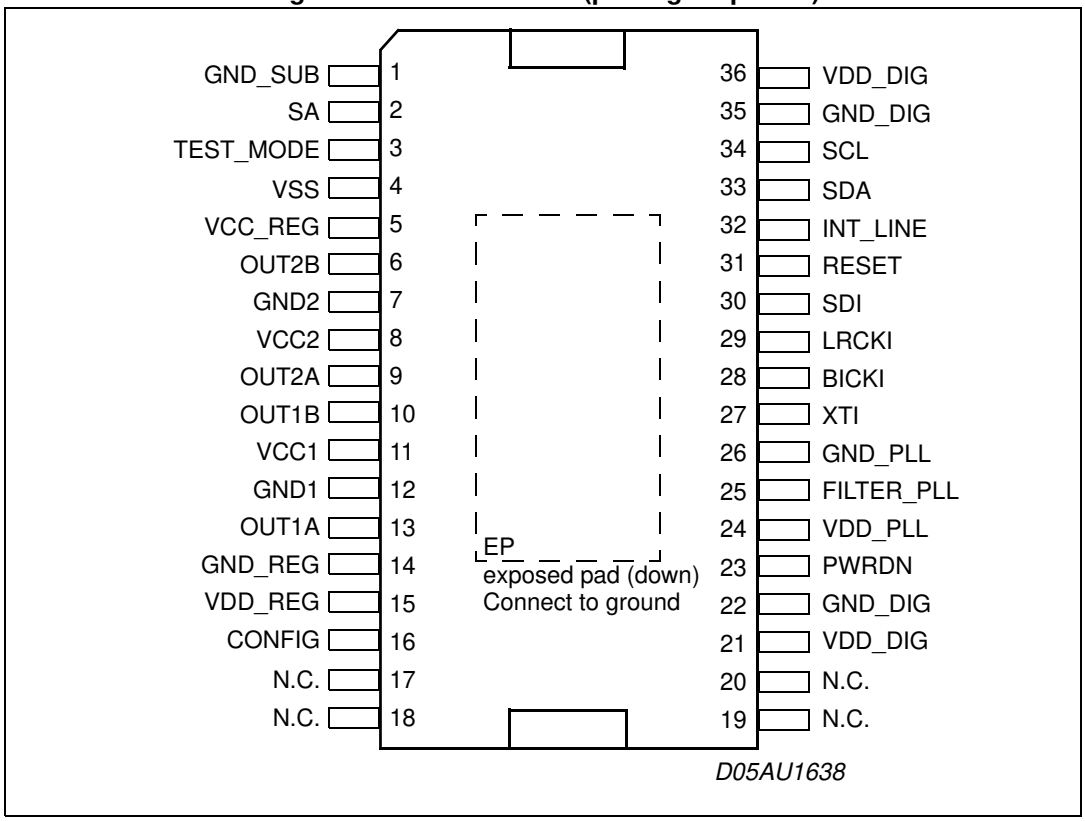
Figure 1. Block diagram



2 Pin description

2.1 Pin out

Figure 2. Pin connection (package top view)



2.2 Pin list

Table 2. Pin description

Number	Type	Name	Description
1	PWR	GND_SUB	Substrate ground
2	I	SA	I²CI²C select address
3	I	TEST_MODE	This pin must be connected to ground
4	I/O	VSS	Internal reference at V_{CC} - 3.3 V
5	I/O	VCC_REG	Internal V_{CC} reference
6	O	OUT2B	Output half bridge 2B
7	PWR	GND2	Power negative supply
8	PWR	VCC2	Power positive supply
9	O	OUT2A	Output half bridge 2A

Table 2. Pin description (continued)

Number	Type	Name	Description
10	O	OUT1B	Output half bridge 1B
11	PWR	VCC1	Power positive supply
12	PWR	GND1	Power negative supply
13	O	OUT1A	Output half bridge 1A
14	PWR	GND_REG	Internal ground reference
15	PWR	VDD_REG	Internal 3.3-V reference voltage
16	I	CONFIG	Paralleled mode command
17	-	N.C.	No internal connection
18	-	N.C.	No internal connection
19	-	N.C.	No internal connection
20	-	N.C.	No internal connection
21	PWR	VDD_DIG	Positive supply digital
22	PWR	GND_DIG	Digital ground
23	I	PWRDN	Power down: 0: power stage is switched off then the PLL is also switched off (this operation take 13 million clock cycles) 1: normal operation
24	PWR	VDD_PLL	Positive supply for PLL
25	I	FILTER_PLL	Connection to PLL filter
26	PWR	GND_PLL	Negative supply for PLL
27	I	XTI	PLL input clock, 256 * f_S, or 384 * f_S
28	I	BICKI	I²S serial clock
29	I	LRCKI	I²S left/right clock
30	I	SDI	I²S serial data channel
31	I	RESET	Reset: 0: reset state, power stage is switched off, all registers are set to default value 1: normal operation
32	O	INT_LINE	Fault interrupt
33	I/O	SDA	I²C serial data, used as SDA_OUT
34	I	SCL	I²C serial clock
35	PWR	GND_DIG	Digital ground
36	PWR	VDD_DIG	Digital supply
-	-	EP	Exposed pad for ground-plane heatsink, to be connected to GND

2.3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{Th(j\text{-}case)}$	Thermal resistance junction to case (thermal pad)	-	1.5	2.0	°C/W
T_{sd}	Thermal-shutdown junction temperature	140	150	160	°C
T_w	Thermal-warning temperature	-	130	-	°C
T_{hsd}	Thermal-shutdown hysteresis	18	20	22	°C

3 Electrical specification

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Analog supply voltage (pins VCCx)	-	-	23	V
V_{DD}	Digital supply voltage (pins VDD_DIG)	-	-	4.0	V
I_L	Logic input interface	-0.3	-	4.0	V
T_{op}	Operating junction temperature	0	-	150	°C
T_{stg}	Storage temperature	-40	-	150	°C

Warning: **Stresses beyond those listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in *Table 5: Recommended operating conditions* are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, a power supply with nominal value rated within the limits of the recommended operating conditions, may experience some rising beyond the maximum operating conditions for a short time when no or very low current is being sinked (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum ratings are not exceeded.**

3.2 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Analog supply voltage (VCCx)	4.5	-	20.0	V
V_{DD}	Digital supply voltage (VDD_DIG)	2.7	3.3	3.6	V
I_L	Logic input interface	2.7	3.3	3.6	V
T_{amb}	Ambient temperature	0	-	70	°C

3.3 Electrical specifications - digital section

Table 6. Electrical characteristics for digital section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Input current, no pull-up or pull-down resistor	V_i = 0 V	-	-	±10	µA
I_{ih}		$V_i = V_{DD}$ = 3.6 V	-	-	±10	µA
V_{il}	Low-level input voltage	-	-	-	0.2 * V_{DD}	V
V_{ih}	High-level input voltage	-	0.8 * V_{DD}	-	-	V
V_{ol}	Low-level output voltage	I_{ol} = 2 mA	-	-	0.4 * V_{DD}	V
V_{oh}	High-level output voltage	I_{oh} = 2 mA	0.8 * V_{DD}	-	-	V
I_{pu}	Pull-up current	-	25	66	125	µA
R_{pu}	Equivalent pull-up resistance	-	-	50	-	kΩ

3.4 Electrical specifications - power section

The specifications in *Table 7* below are given for the conditions V_{CC} = 18 V, V_{DD} = 3.3 V, f_{SW} = 384 kHz, T_{amb} = 25 °C and R_L = 8 Ω, unless otherwise specified.

Table 7. Electrical specifications for power section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Po	Output power BTL	THD = 1%	-	16	-	W
		THD = 10%	-	20	-	
R_{dsON}	Power P-channel/N-channel MOSFET (total bridge)	Id = 1 A	-	180	250	mΩ
I_{dss}	Power P-channel/N-channel leakage	V_{CC} = 18 V	-	-	10	µA
gP	Power P-channel R_{dsON} matching	Id = 1 A	95	-	-	%
gN	Power N-channel R_{dsON} matching	Id = 1 A	95	-	-	%
I_{LDT}	Low-current dead time (static)	Resistive load, refer to *Figure 5*	-	5	10	ns
I_{HDT}	High-current dead time (dynamic)	Refer to *Figure 6*	-	10	20	ns
t_r	Rise time	Resistive load, refer to *Figure 5*	-	8	10	ns

Table 7. Electrical specifications for power section (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	Fall time	Resistive load, refer to *Figure 5*	-	8	10	ns
V_{CC}	Supply voltage	-	4.5	-	20	V
I_{VCC}	Supply current from V_{CC} in power down	PWRDN = 0	30	60	200	µA
	Supply current from V_{CC} in operation	PCM input signal = -60 dBfs Switching frequency = 384 kHz No LC filters	-	30	50	mA
I_{VDD_DIG}	Supply current for DDX processing (reference only)	Internal clock = 49.152 MHz	10	30	50	mA
	Supply current in standby	-	8	11	25	mA
I_{LIM}	Overcurrent limit	Non-linear output (1)	2.2	3.5	4.3	A
I_{SCP}	Short-circuit protection	High-impedance output (2)	2.7	3.8	5.0	A
V_{UVP}	Undervoltage protection threshold	-	-	3.5	4.3	V
t_{min}	Output minimum pulse width	No load	20	30	60	ns
THD+N	Total harmonic distortion and noise	DXX stereo mode, Po = 1 W, f = 1 kHz	-	0.05	0.2	%
DR	Dynamic range	-	-	100	-	dB
SNR	Signal to noise ratio in ternary mode	A-weighted	-	100	-	dB
	Signal to noise ratio in binary mode	A-weighted	-	90	-	
PSRR	Power supply rejection ratio	DXX stereo mode, < 5 kHz, V_{RIPPLE} = 1 V RMS audio input = dither only	-	80	-	dB
X_{TALK}	Crosstalk	DXX stereo mode, < 5 kHz, One channel driven at 1 W the other channel measured	-	80	-	dB
η	Peak efficiency in DXX mode	Po = 2 x 20 W into 8 Ω	-	90	-	%

1. The I_{LIM} data is for 1 channel of BTL configuration, thus, 2 * I_{LIM} drives the 2-channel BTL configuration. The current limit is active when OCRB = 0 (see *Table 23: Overcurrent warning detect adjustment bypass on page 28*. When OCRB = 1 then I_{SC} applies.
2. The I_{SCP} current limit data is for 1 channel of BTL configuration, thus, 2 * I_{SCP} drives the 2-channel BTL configuration. The short-circuit current is applicable when OCRB = 1 (see *Table 23: Overcurrent warning detect adjustment bypass on page 28*.

3.5 Power-on/off sequences

The power-on/off sequences shown in *Figure 3* and *Figure 4* below ensure a pop-free turn on and turn off.

Figure 3. Power-on sequence

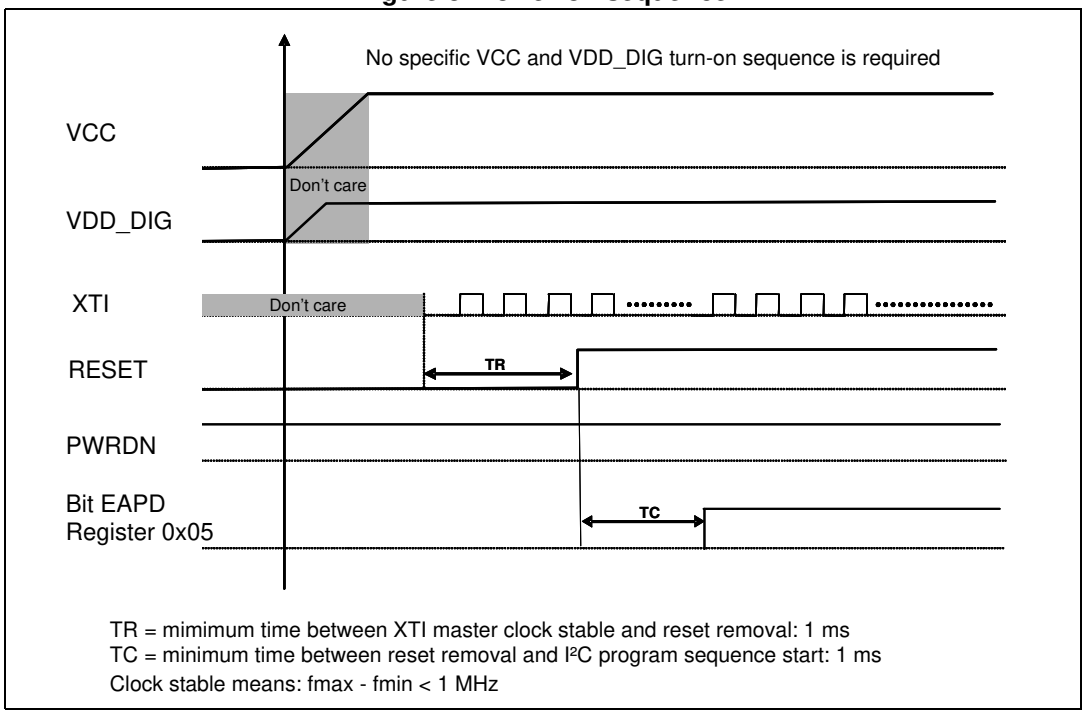
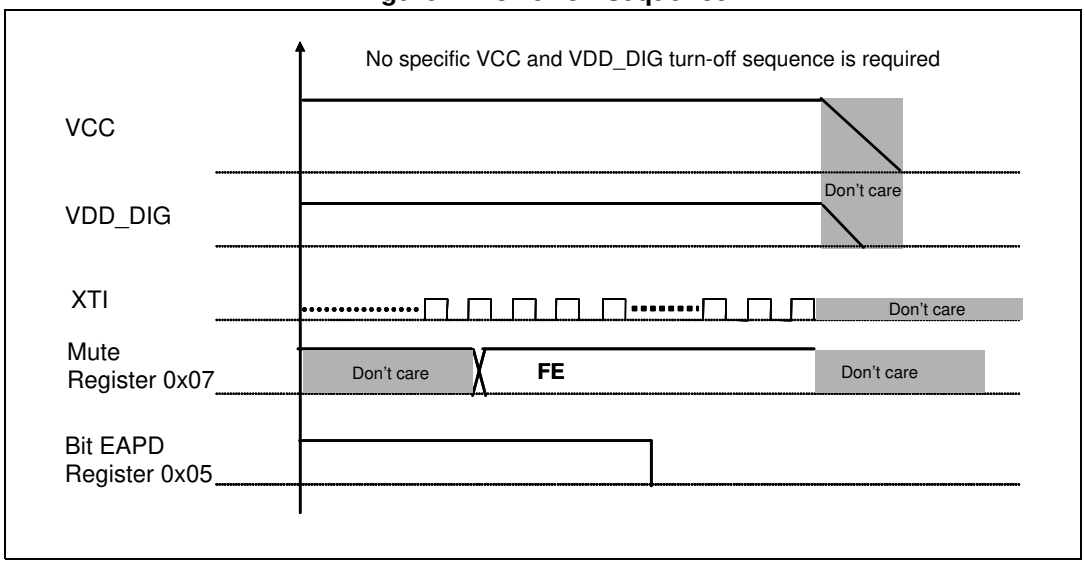


Figure 4. Power-off sequence



3.6 Testing

Figure 5. Test circuit

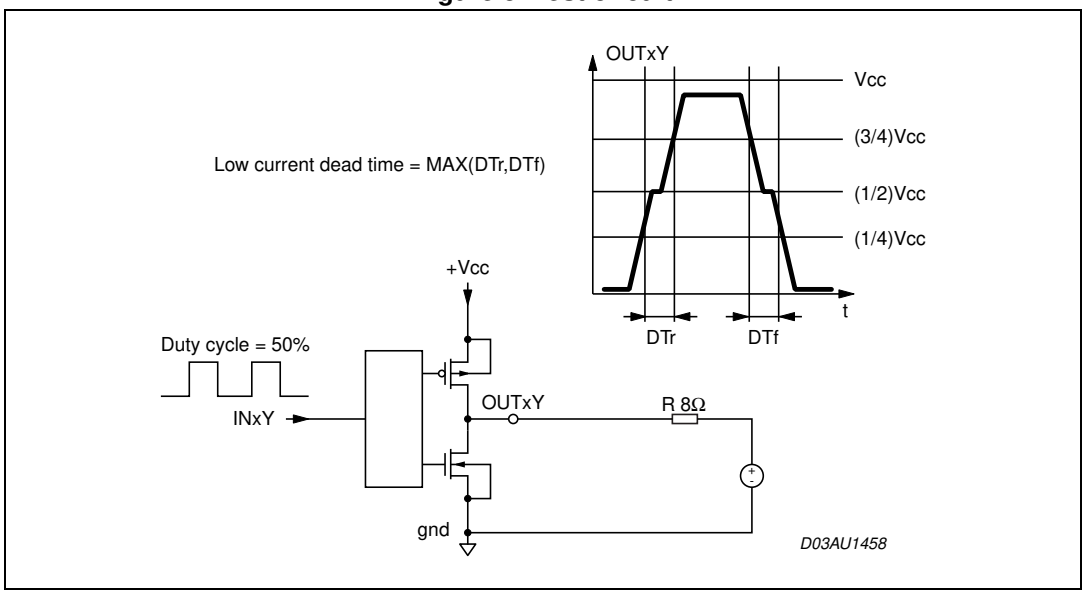
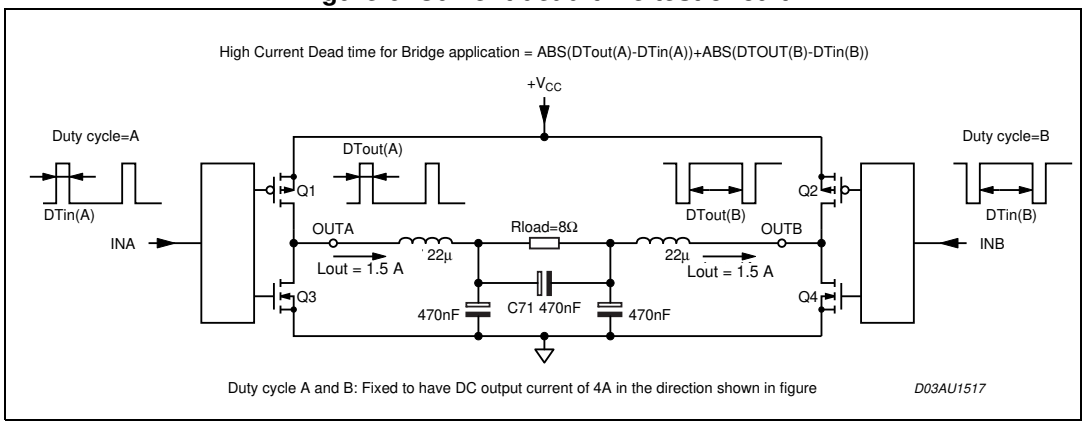


Figure 6. Current dead-time test circuit



4 Functional description

4.1 Functional pins

4.1.1 Power-down function

Pin PWRDN (23) is used to power down the STA333W.

PWRDN = 0 (0 V): power-down state.

PWRND = 1 (V_{DD}): νορμαλ οπερατιον.

During the power-down sequence the output begins to mute. After the mute condition is reached the power stage is switched off and the output becomes high impedance. Then the master clock to all internal hardware blocks is gated off. The PLL is also switched off. The complete power-down sequence takes 13 million cycles.

4.1.2 Reset function

Pin RESET (31) is used to reset the STA333W.

RESET = 0 (0 V): reset state.

RESET = 1 (V_{DD}): normal operation.

When pin RESET is forced to 0 the power stage is switched off (with high-impedance output) and the master clock to all internal hardware blocks is gated off.

Note: Reset has a higher priority than power down.

4.2 Serial audio interface description

4.2.1 Serial audio interface protocols

The STA333W serial audio input was designed to interface with standard digital audio components and to accept serial data formats. The STA333W always acts as a slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using 3 input pins: left/right clock LRCKI (pin 29), serial clock BICKI (pin 28), and serial data SDI (pin 30).

The available formats are showed in *Table 7* and *Table 8*, and set through register CONFB *on page 24*.

Figure 7. I²S

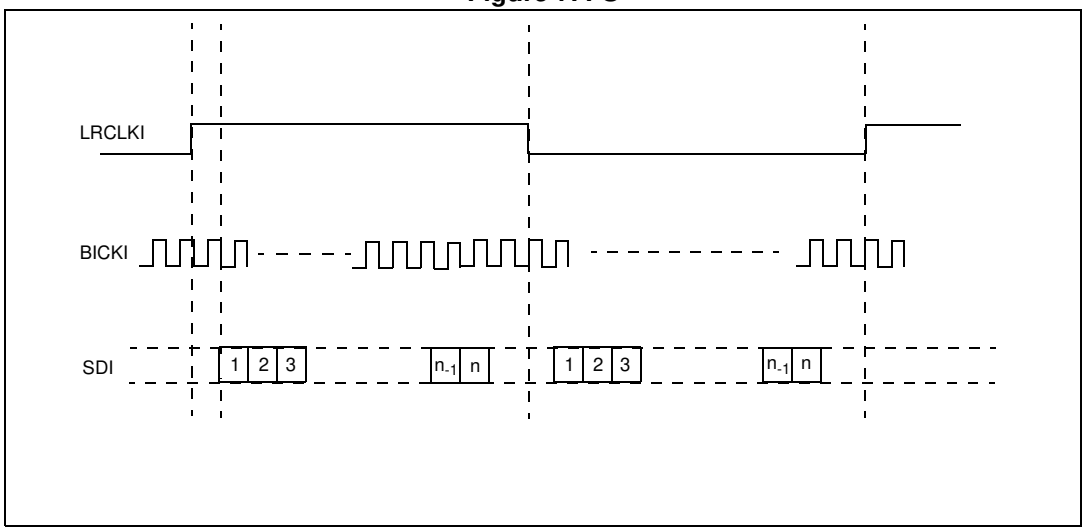
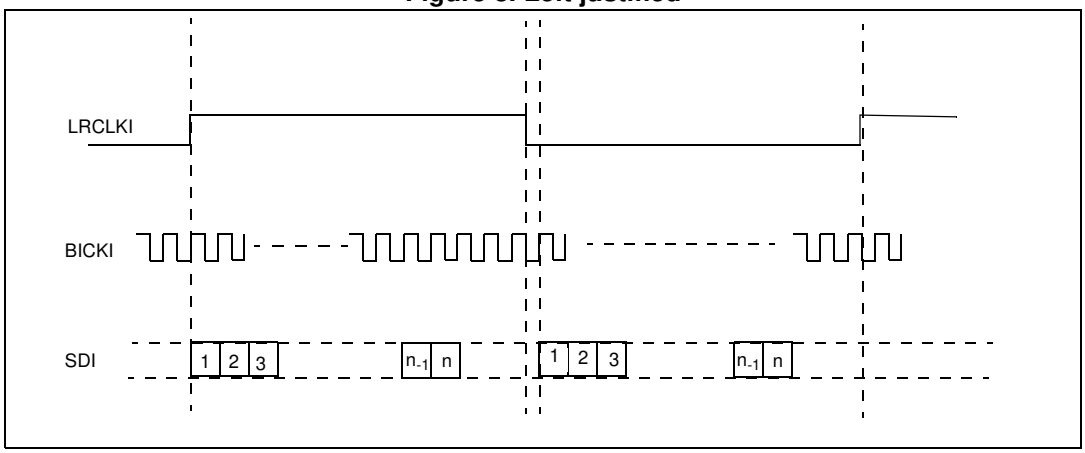


Figure 8. Left justified



5 I²C bus specification

The STA333W supports the I²C protocol via the input ports SCL and SDA. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA333W is always a slave device in all of its communications. It supports up to 400 kb/s (fast-mode bit rate).

5.1 Communication protocol

5.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

5.1.2 Start condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

5.1.3 Stop condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between STA333W and the bus master.

5.1.4 Data input

During the data input the STA333W samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

5.2 Device addressing

To start communication between the master and the STA333W, the master must initiate a start condition. Following this, the master sends onto the SDA line 8 bits (MSB first) corresponding to the device-select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA333W the I²C interface has two device addresses depending on the SA port configuration, 0x38 when SA = 0, and 0x3A when SA = 1.

The 8th bit (LSB) identifies read or write operation RW, this bit is set to 1 for read mode and 0 for write mode. After a START condition the STA333W identifies the device address on the SDA bus and if a match is found, acknowledges the identification during the 9th bit time. The byte following the device identification byte is the internal space address.

5.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA333W acknowledges this and then waits for the byte of internal address. After receiving the internal byte address the STA333W again responds with an acknowledgement.

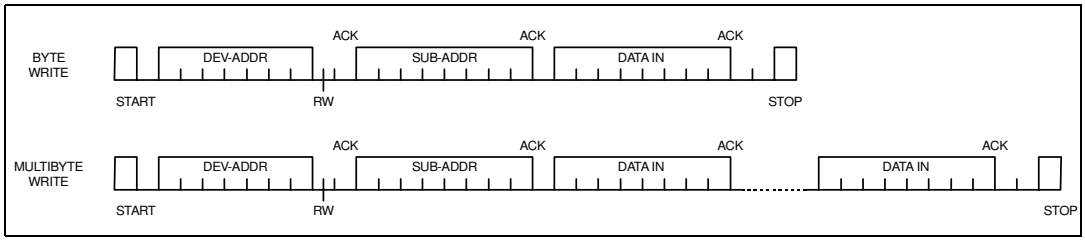
5.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by the STA333W. The master then terminates the transfer by generating a STOP condition.

5.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 9. Write-mode sequence



5.4 Read operation

5.4.1 Current address byte read

Following the START condition the master sends a device select code with the RW bit set to 1. The STA333W acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

5.4.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA333W. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

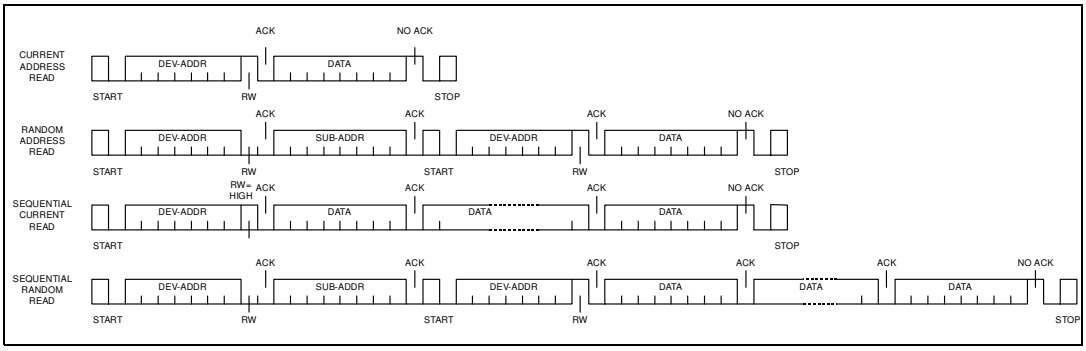
5.4.3 Random address byte read

Following the START condition the master sends a device select code with the RW bit set to 0. The STA333W acknowledges this and then the master writes the internal address byte. After receiving, the internal byte address the STA333W again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA333W acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

5.4.4 Random address multi-byte read

The multi-byte read modes could start from any internal address. Sequential data bytes are read from sequential addresses within the STA333W. The master acknowledges each data byte read and then generates a STOP condition to terminate the transfer.

Figure 10. Read-mode sequence



6 Register description

Table 8. Register summary

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	CONFA	FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0x01	CONFB	C2IM	C1IM	Reserved	SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	CONFC	OCRB	Reserved	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x03	CONFD	Reserved	ZDE	Reserved					
0x04	CONFE	SVE	ZCE	DCCV	PWMS	AME	NSBW	MPC	MPCV
0x05	CONFF	EAPD	PWDN	ECLE	LDTE	BCLE	IDE	Reserved	
0x06	MUTE	Reserved					C2M	C1M	MMUTE
0x07	MVOL	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x08	C1VOL	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x09	C2VOL	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0C	AUTO	Reserved				AMAM2	AMAM1	AMAM0	AMAME
0x0E	C1CFG	Reserved					C1VBP	Reserved	
0x0F	C2CFG	Reserved					C2VBP	Reserved	
0x27	MPCC1	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x28	MPCC2	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x29	DCC1	DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
0x2A	DCC2	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0x2B	FDRC1	FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0x2C	FDRC2	FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0x2D	STATUS	PLLUL	FAULT	UVFAULT	Reserved	OCFAULT	OCWARN	TFAULT	TWARN
0x2E	BIST1	Reserved		RO1BACT	R5BACT	R4BACT	R3BACT	R2BACT	R1BACT
0x2F	BIST2	Reserved		R01BEND	R5BEND	R4BEND	R3BEND	R2BEND	R1BEND
0x30	BIST3	Reserved			R5BBAD	R4BBAD	R3BBAD	R1BBAD	R1BBAD
0x31	TSTCTL	Reserved							
0x32	C1PS	C1PS7	C1PS6	C1PS5	C1PS4	C1PS3	C1PS2	C1PS1	C1PS0
0x33	C2PS	C2PS7	C2PS6	C2PS5	C2PS4	C2PS3	C2PS2	C2PS1	C2PS0
0x34	OLIM	OLIM7	OLIM6	OLIM5	OLIM4	OLIM3	OLIM2	OLIM1	OLIM0

6.1 Configuration registers (addr 0x00 to 0x05)

6.1.1 Configuration register A (addr 0x00)

D7	D6	D5	D4	D3	D2	D1	D0
FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0	1	1	0	0	0	1	1

Master clock select

Table 9. Master clock select

Bit	R/W	RST	Name	Description
0	R/W	1	MCS0	Master clock select: Selects the ratio between the input I²S sample frequency and the input clock.
1	R/W	1	MCS1	
2	R/W	0	MCS2	

The STA333W supports sample rates of 32 kHz, 44.1 kHz, 48 KHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz. Therefore the internal clock is:

- 32.768 MHz for 32 kHz
- 45.1584 MHz for 44.1 kHz, 88.2 kHz, and 176.4 kHz
- 49.152 MHz for 48 kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency (f_S).

The relationship between the input clock and the input sample rate is determined by both the MCSx and the IR (input rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IR bit determines the oversampling ratio used internally.

Table 10. MCS bits

Input sample rate f_S (kHz)	IR	MCS[2:0]					
		101	100	011	010	001	000
32, 44.1, 48	00	576 * f_S	128 * f_S	256 * f_S	384 * f_S	512 * f_S	768 * f_S
88.2, 96	01	NA	64 * f_S	128 * f_S	192 * f_S	256 * f_S	384 * f_S
176.4, 192	1X	NA	32 * f_S	64 * f_S	96 * f_S	128 * f_S	192 * f_S

Interpolation ratio select

Table 11. Interpolation ratio select

Bit	R/W	RST	Name	Description
4:3	R/W	00	IR [1:0]	Interpolation ratio select: Selects internal interpolation ratio based on input I²SI²S sample frequency.

The STA333W has variable interpolation (oversampling) settings such that internal processing and DDX output rates remain consistent. The first processing block interpolates by either 2 times or 1 time (pass-through) or provides a 2-times downsample. The oversampling ratio of this interpolation is determined by the IR bits.

Table 12. IR bit settings as a function of input sample rate

Input sample rate f_S (kHz)	IR	1st stage interpolation ratio
32	00	2-times oversampling
44.1	00	2-times oversampling
48	00	2-times oversampling
88.2	01	Pass-through
96	01	Pass-through
176.2	10	2-times downsampling
192	10	2-times downsampling

Thermal warning recovery bypass

Table 13. Thermal warning recovery

Bit	R/W	RST	Name	Description
5	R/W	1	TWRB	Thermal warning recovery bypass: 0: thermal warning recovery enabled 1: thermal warning recovery disabled

If the thermal warning adjustment is enabled (TWAB = 0), then the thermal warning recovery determines if the -3 dB output limit is removed when thermal warning is negative.

If TWRB = 0 and TWAB = 0, then when a thermal warning disappears the -3 dB output limit is removed and the gain is added back to the system. If TWRB = 1 and TWAB = 0, then when a thermal warning disappears the -3 dB output limit remains until TWRB is changed to zero or the device is reset.

Thermal warning adjustment bypass

Table 14. Thermal warning adjustment

Bit	R/W	RST	Name	Description
6	R/W	1	TWAB	Thermal warning adjustment bypass: 0: thermal warning adjustment enabled 1: thermal warning adjustment disabled

The on-chip STA333W power output block provides feedback to the digital controller using inputs to the power control block. The TWARN input is used to indicate a thermal warning condition. When TWARN is asserted (set to 0) for a period of time greater than 400 ms, the power control block will force a -3dB output limit (determined by TWOCL in coefficient RAM) to the modulation limit in an attempt to eliminate the thermal warning condition. Once the thermal warning output limit adjustment is applied, it remains in this state until reset, unless FDRB = 0.

Fault detect recovery bypass

Table 15. Fault detect recovery

Bit	R/W	RST	Name	Description
7	R/W	0	FDRB	Fault detect recovery bypass: 0: fault detect recovery enabled 1: fault detect recovery disabled

The on-chip STA333W power output block provides feedback to the digital controller using inputs to the power control block. The FAULT input is used to indicate a fault condition (either overcurrent or thermal). When FAULT is asserted (set to 0), the power control block attempts a recovery from the fault by asserting the 3-state output (setting it to 0 which directs the power output block to begin recovery), holding it at 0 for period of time in the range of 0.1 ms to 1 second as defined by the fault detect recovery constant register (FDRC registers 0x2B, 0x2C), then toggling it back to 1. This sequence is repeated as log as the fault indication exists. This feature is enabled by default but can be bypassed by setting the FDRB control bit to 1.

6.1.2 Configuration register B (addr 0x01)

D7	D6	D5	D4	D3	D2	D1	D0
C2IM	C1IM	Reserved	SAIFB	SAI3	SAI2	SAI1	SAI0
1	0	0	0	0	0	0	0

Serial audio input interface format

Table 16. Serial audio input interface format

Bit	R/W	RST	Name	Description
0	R/W	0	SAI0	Determines the interface format of the input serial digital audio interface.
1	R/W	0	SAI1	
2	R/W	0	SAI2	
3	R/W	0	SAI3	

Serial data interface

The STA333W audio serial input interfaces with standard digital audio components and accepts a number of serial data formats. STA333W always acts a slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using three inputs: left/right clock LRCKI, serial clock BICKI, and serial data SDI.

Bits SAI and bit SAIFB are used to specify the serial data format. The default serial data format is I²S, MSB first. Available formats are shown in the tables and figure that follow.

Serial data first bit

Table 17. Serial data first bit

SAIFB	Format
0	MSB-first
1	LSB-first

Table 18. Support serial audio input formats for MSB first (SAIFB = 0)

BICKI	SAI [3:0]	SAIFB	Interface format
32 * f_S	0000	0	I²S 15-bit data
	0001	0	Left/right justified 16-bit data
48* f_S	0000	0	I²S 16- to 23-bit data
	0001	0	Left justified 16- to 24-bit data
	0010	0	Right justified 24-bit data
	0110	0	Right justified 20-bit data
	1010	0	Right justified 18-bit data
	1110	0	Right justified 16-bit data
64* f_S	0000	0	I²S 16- to 24-bit data
	0001	0	Left justified 16- to 24-bit data
	0010	0	Right justified 24-bit data
	0110	0	Right justified 20-bit data
	1010	0	Right justified 18-bit data
	1110	0	Right justified 16-bit data