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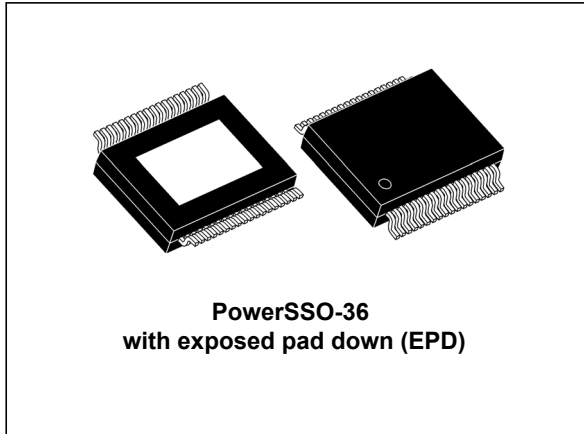
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## 2.1-channel 40-watt high-efficiency digital system Sound Terminal<sup>®</sup>

Datasheet - production data



### Features

- Wide-range supply voltage, 4.5 V to 21.5 V
- Three power output configurations:
  - 2 channels of ternary PWM (2 x 20 W into 8 Ω at 18 V) + PWM output
  - 2 channels of ternary PWM (2 x 20 W into 8 Ω at 18 V) + ternary stereo line-out
  - 2.1 channels of binary PWM (left, right, LFE) (2 x 9 W into 4 Ω + 1 x 20 W into 8 Ω at 18 V)
- FFX with 100-dB SNR and dynamic range
- Scalable FFX modulation index
- Selectable 32- to 192-kHz input sample rates
- I<sup>2</sup>C control with selectable device address
- Digital gain/attenuation +48 dB to -80 dB with 0.5-dB/step resolution
- Soft volume update with programmable ratio
- Individual channel and master gain/attenuation
- Two independent DRCs configurable as a dual-band anticlipper (B<sup>2</sup>DRC) or as independent limiters/compressors
- EQ-DRC for DRC based on filtered signals
- Dedicated LFE processing for bass boosting
- Audio presets:
  - 15 preset crossover filters
  - 5 preset anticlipping modes
  - Preset nighttime listening mode
- Individual channel soft/hard mute
- Independent channel volume and DSP bypass
- I<sup>2</sup>S input data interface
- Input and output channel mapping
- Automatic invalid input-detect mute
- Up to 8 user-programmable biquads/channel
- Three coefficient banks for storing EQ presets with fast recall via I<sup>2</sup>C interface
- Bass/treble tones and de-emphasis control
- Selectable high-pass filter for DC blocking
- Advanced AM interference frequency switching and noise suppression modes
- Selectable high- or low-bandwidth noise-shaping topologies
- Selectable clock input ratio
- 96-kHz internal processing sample rate
- Thermal overload and short-circuit protection technology
- Video apps: 576 x f<sub>S</sub> input mode supported
- Pin and SW compatible with STA333BW, STA339BW, STA559BW and STA559BWS

**Table 1. Device summary**

Order code	Package	Packaging
STA339BWS	PowerSSO-36 EPD	Tube
STA339BWS13TR	PowerSSO-36 EPD	Tape and reel

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# 1 Description

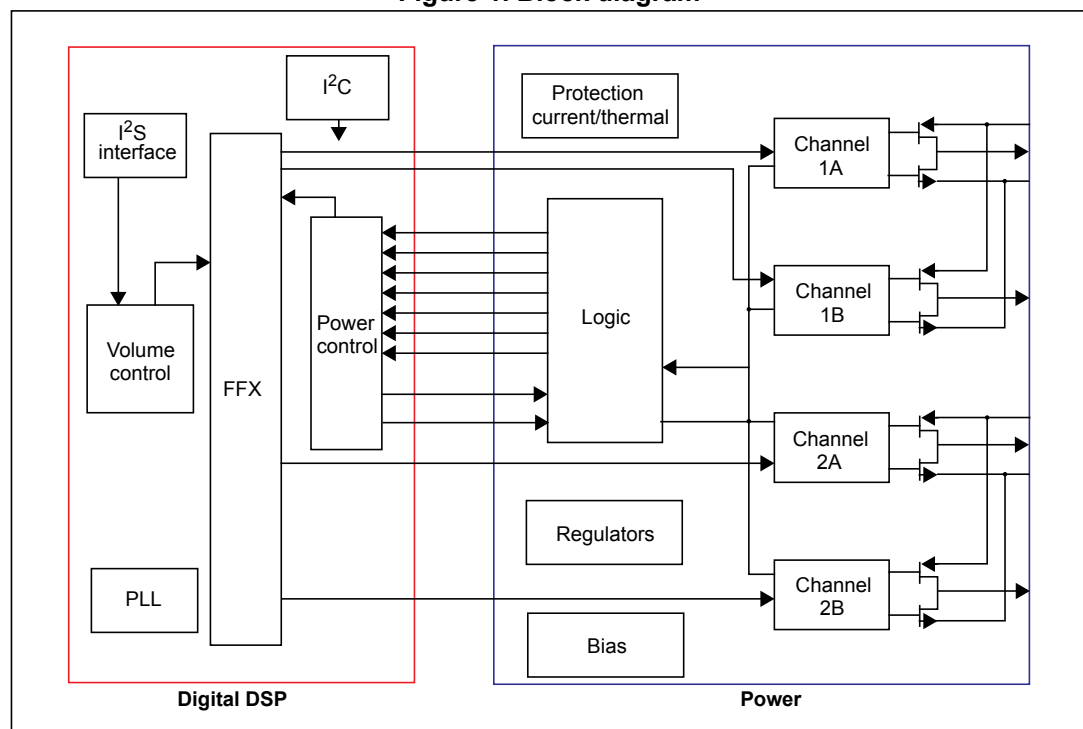
The STA339BWS is an integrated solution of digital audio processing, digital amplifier controls and power output stage to create a high-power single-chip FFX digital amplifier with high quality and high efficiency. Three channels of FFX processing are provided. The FFX processor implements the ternary, binary and binary differential processing capabilities of the full FFX processor.

The STA339BWS is part of the Sound Terminal<sup>®</sup> family that provides full digital audio streaming to the speakers and offers cost effectiveness, low power dissipation and sound enrichment.

Also provided in the STA339BWS are a full assortment of digital processing features. This includes up to 8 programmable biquads (EQ) per channel. Available presets enable a time-to-market advantage by substantially reducing the amount of software development needed for functions such as audio preset volume loudness, preset volume curves and preset EQ settings. There are also new advanced AM radio interference reduction modes. Dual-band DRC dynamically equalizes the system to provide linear frequency speaker response regardless of output power level. This feature separates the audio frequency band into two sub-bands independently processed to provide better sound clarity and to avoid speaker saturation.

The serial audio data input interface accepts all possible formats, including the popular I<sup>2</sup>S format. The high-quality conversion from PCM audio to FFX PWM switching provides over 100 dB of SNR and of dynamic range.

Figure 1. Block diagram



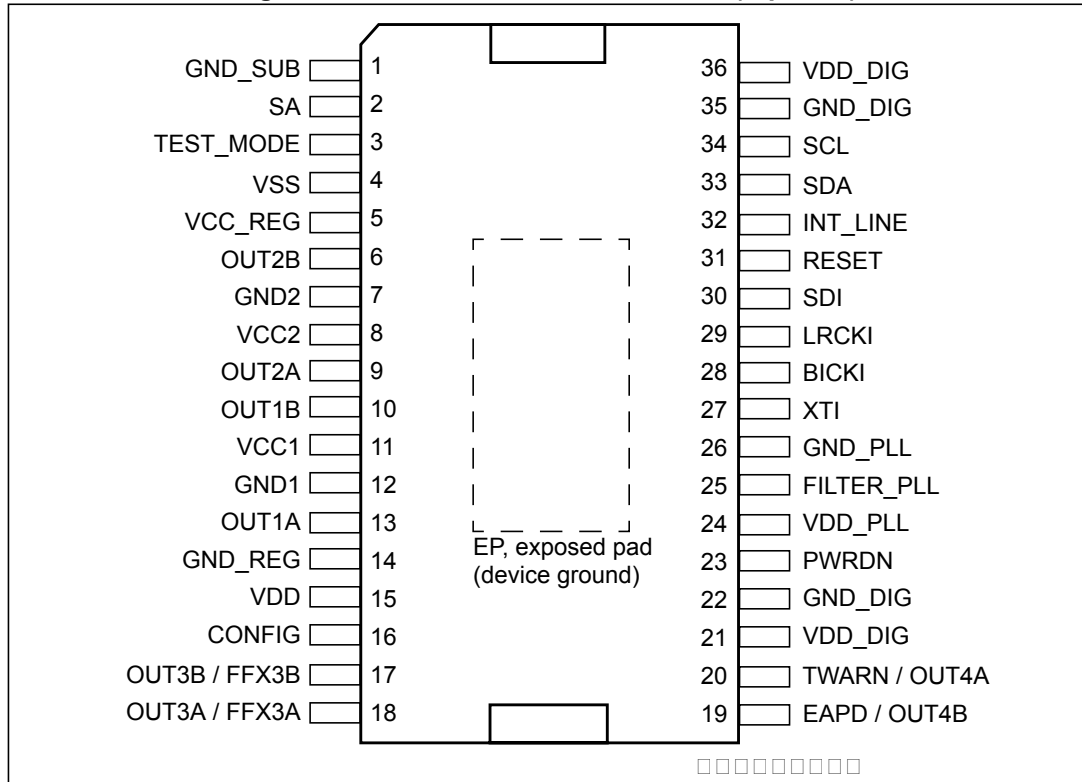
The power section consists of four independent half-bridges. These can be configured via digital control to operate in different modes.

- 2.1 channels can be provided by two half bridges and a single full bridge, supplying up to  $2 \times 9 \text{ W} + 1 \times 20 \text{ W}$  of output power.
- Two channels can be provided by two full-bridges, supplying up to  $2 \times 20 \text{ W}$  of output power.
- The IC can also be configured as 2.1 channels with  $2 \times 20 \text{ W}$  supplied by the device plus a drive for an external FFX power amplifier, such as STA533WF or STA515W.
- One channel can be provided by parallel BTL to obtain  $1 \times 40 \text{ W}$  of output power. In this configuration the CONFIG pin must be connected to VDD.

## 2 Pin connections

### 2.1 Connection diagram

Figure 2. Pin connection PowerSSO-36 (top view)



### 2.2 Pin description

Table 2. Pin description

Pin	Type	Name	Description
1	GND	GND_SUB	Substrate ground
2	I	SA	I <sup>2</sup> C select address (pull-down)
3	I	TEST_MODE	This pin must be connected to ground (pull-down)
4	I/O	VSS	Internal reference at V <sub>CC</sub> - 3.3 V
5	I/O	VCC_REG	Internal V <sub>CC</sub> reference
6	O	OUT2B	Output half-bridge channel 2B
7	GND	GND2	Power negative supply
8	Power	VCC2	Power positive supply
9	O	OUT2A	Output half-bridge channel 2A
10	O	OUT1B	Output half-bridge channel 1B

Table 2. Pin description (continued)

Pin	Type	Name	Description
11	Power	VCC1	Power positive supply
12	GND	GND1	Power negative supply
13	O	OUT1A	Output half-bridge channel 1A
14	GND	GND_REG	Internal ground reference
15	Power	VDD	Internal 3.3 V reference voltage
16	I	CONFIG	Parallel mode command
17	O	OUT3B / FFX3B	PWM out channel 3B / external bridge driver
18	O	OUT3A / FFX3A	PWM out channel 3A / external bridge driver
19	O	EAPD / OUT4B	Power down for external bridge / PWM out channel 4B
20	I/O	TWARN / OUT4A	Thermal warning from external bridge (pull-up when input) / PWM out channel 4A
21	Power	VDD_DIG	Digital supply voltage
22	GND	GND_DIG	Digital ground
23	I	PWRDN	Power down (pull-up)
24	Power	VDD_PLL	Positive supply for PLL
25	I	FILTER_PLL	Connection to PLL filter
26	GND	GND_PLL	Negative supply for PLL
27	I	XTI	PLL input clock
28	I	BICKI	I <sup>2</sup> S serial clock
29	I	LRCKI	I <sup>2</sup> S left/right clock
30	I	SDI	I <sup>2</sup> S serial data channels 1 and 2
31	I	RESET	Reset (pull-up)
32	O	INT_LINE	Fault interrupt
33	I/O	SDA	I <sup>2</sup> C serial data
34	I	SCL	I <sup>2</sup> C serial clock
35	GND	GND_DIG	Digital ground
36	Power	VDD_DIG	Digital supply voltage
-	-	EP	Exposed pad for PCB heatsink, to be connected to GND

## 3 Electrical specifications

### 3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Power supply voltage (pins VCCx)	-0.3	-	24	V
V <sub>DD</sub>	Digital supply voltage (pins VDD_DIG)	-0.3	-	4.0	V
V <sub>DD</sub>	PLL supply voltage (pin VDD_PLL)	-0.3	-	4.0	V
T <sub>op</sub>	Operating junction temperature	-20	-	150	°C
T <sub>stg</sub>	Storage temperature	-40	-	150	°C

**Warning:** Stresses beyond those listed in [Table 3](#) above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended operating conditions” are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, power supplies with nominal values rated within the recommended operating conditions, may experience some rising beyond the maximum operating conditions for a short time when no or very low current is sunk (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum ratings are not exceeded.

### 3.2 Thermal data

Table 4. Thermal data

	Parameter	Min	Typ	Max	Unit
R <sub>th j-case</sub>	Thermal resistance junction-case (thermal pad)	-	-	1.5	°C/W
T <sub>th_sdj</sub>	Thermal shut-down junction temperature	-	150	-	°C
T <sub>th_warn</sub>	Thermal warning temperature	-	130	-	°C
T <sub>th_sdh</sub>	Thermal shut-down hysteresis	-	20	-	°C
R <sub>th j-amb</sub>	Thermal resistance junction-ambient <sup>(1)</sup>	-	24	-	°C/W

1. See [Chapter 9: Package thermal characteristics on page 75](#) for details.



### 3.3 Recommended operating conditions

**Table 5. Recommended operating condition**

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Power supply voltage (VCCxA, VCCxB)	4.5	-	21.5	V
V <sub>DD_DIG</sub>	Digital supply voltage	2.7	3.3	3.6	V
V <sub>DD_PLL</sub>	PLL supply voltage	2.7	3.3	3.6	V
T <sub>amb</sub>	Ambient temperature	-20	-	70	°C

### 3.4 Electrical specifications for the digital section

**Table 6. Electrical specifications - digital section (T<sub>amb</sub> = 25 °C)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>il</sub>	Low level input current without pull-up/down device	V <sub>i</sub> = 0 V	-	-	1	µA
I <sub>ih</sub>	High level input current without pull-up/down device	V <sub>i</sub> = V <sub>DD_DIG</sub> = 3.6 V	-	-	1	µA
V <sub>il</sub>	Low level input voltage	-	-	-	0.2 * V <sub>DD_DIG</sub>	V
V <sub>ih</sub>	High level input voltage	-	0.8 * V <sub>DD_DIG</sub>	-	-	V
V <sub>ol</sub>	Low level output voltage	I <sub>ol</sub> = 2 mA	-	-	0.4 * V <sub>DD_DIG</sub>	V
V <sub>oh</sub>	High level output voltage	I <sub>oh</sub> = 2 mA	0.8 * V <sub>DD_DIG</sub>	-	-	V
R <sub>pu</sub>	Equivalent pull-up/down resistance	-	-	50	-	kΩ

### 3.5 Electrical specifications for the power section

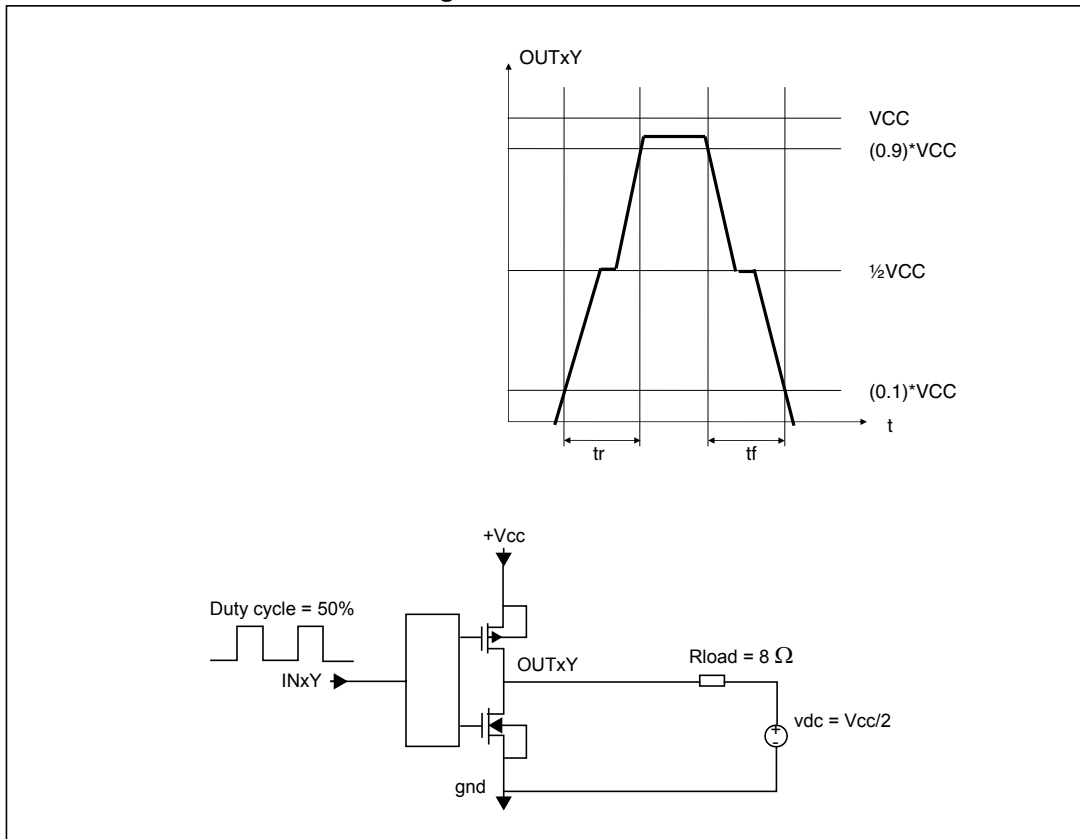
The specifications given in this section are valid for the operating conditions:  $V_{CC} = 18\text{ V}$ ,  $f = 1\text{ kHz}$ ,  $f_{sw} = 384\text{ kHz}$ ,  $T_{amb} = 25\text{ °C}$  and  $R_L = 8\text{ }\Omega$ , unless otherwise specified.

**Table 7. Electrical specifications - power section**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Po	Output power BTL	THD = 1%	-	16	-	W
		THD = 10%	-	20	-	
	Output power SE	THD = 1%, $R_L = 4\text{ }\Omega$	-	7	-	W
		THD = 10%, $R_L = 4\text{ }\Omega$	-	9	-	
R <sub>dsON</sub>	Power P-channel or N-channel MOSFET	$I_d = 0.75\text{ A}$	-	-	250	m $\Omega$
gP	Power P-channel RdsON matching	$I_d = 0.75\text{ A}$	-	100	-	%
gN	Power N-channel RdsON matching	$I_d = 0.75\text{ A}$	-	100	-	%
I <sub>dss</sub>	Power P-channel/N-channel leakage	$V_{CC} = 20\text{ V}$	-	-	1	$\mu\text{A}$
t <sub>r</sub>	Rise time	Resistive load, see <i>Figure 3</i> below	-	-	10	ns
t <sub>f</sub>	Fall time		-	-	10	ns
I <sub>VCC</sub>	Supply current from $V_{CC}$ in power down	PWRDN = 0	-	0.3	-	$\mu\text{A}$
	Supply current from $V_{CC}$ in operation	PWRDN = 1	-	15	-	mA
I <sub>VDD</sub>	Supply current FFX processing	Internal clock = 49.152 MHz	-	55	-	mA
I <sub>LIM</sub>	Overcurrent limit	(1)	2.5	3.0	-	A
I <sub>SCP</sub>	Short -circuit protection	$R_L = 0\text{ }\Omega$	3.0	3.6	-	A
V <sub>UVP</sub>	Undervoltage protection	-	-	-	4.3	V
t <sub>min</sub>	Output minimum pulse width	No load	20	40	60	ns
DR	Dynamic range	-	-	100	-	dB
SNR	Signal to noise ratio, ternary mode	A-Weighted	-	100	-	dB
	Signal to noise ratio binary mode	-	-	90	-	dB
THD+N	Total harmonic distortion + noise	FFX stereo mode, $P_o = 1\text{ W}$ $f = 1\text{ kHz}$	-	0.2	-	%
X <sub>TALK</sub>	Crosstalk	FFX stereo mode, <5 kHz One channel driven at 1 W, other channel measured	-	80	-	dB
$\eta$	Peak efficiency, FFX mode	$P_o = 2 \times 20\text{ W}$ into $8\text{ }\Omega$	-	90	-	%
	Peak efficiency, binary modes	$P_o = 2 \times 9\text{ W}$ into $4\text{ }\Omega$ + $1 \times 20\text{ W}$ into $8\text{ }\Omega$	-	87	-	

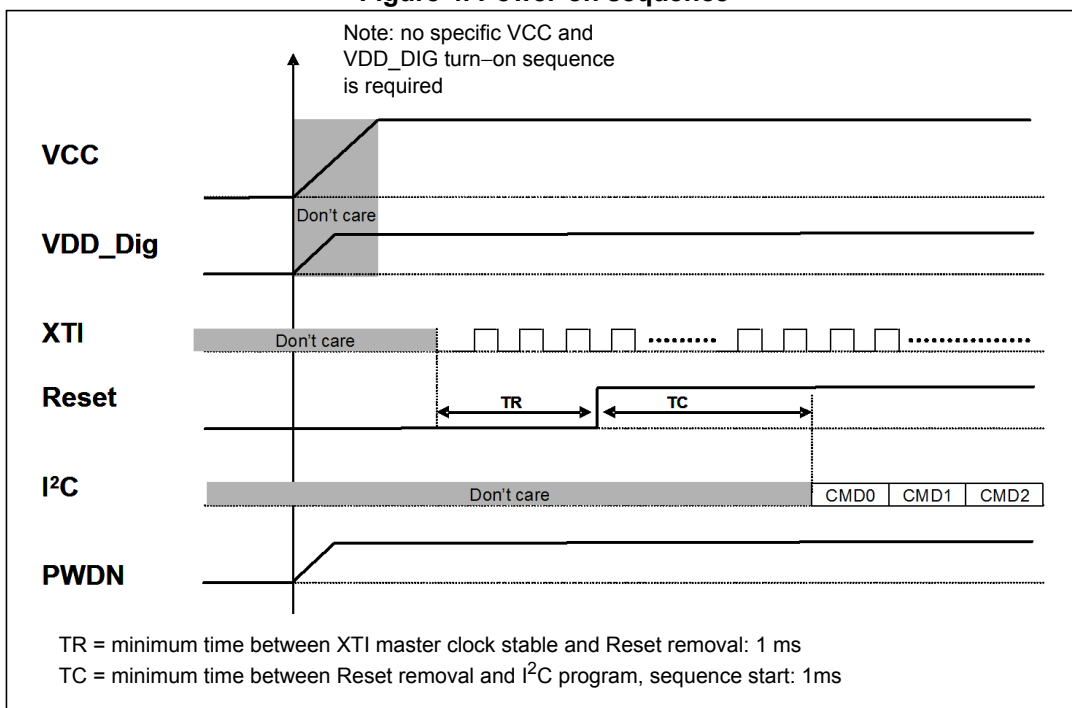
1. Limit the current if overcurrent warning detect adjustment bypass is enabled (register bit CONF.CORB on page 31).  
When disabled refer to the I<sub>SCP</sub>

Figure 3. Test circuit



### 3.6 Power on/off sequence

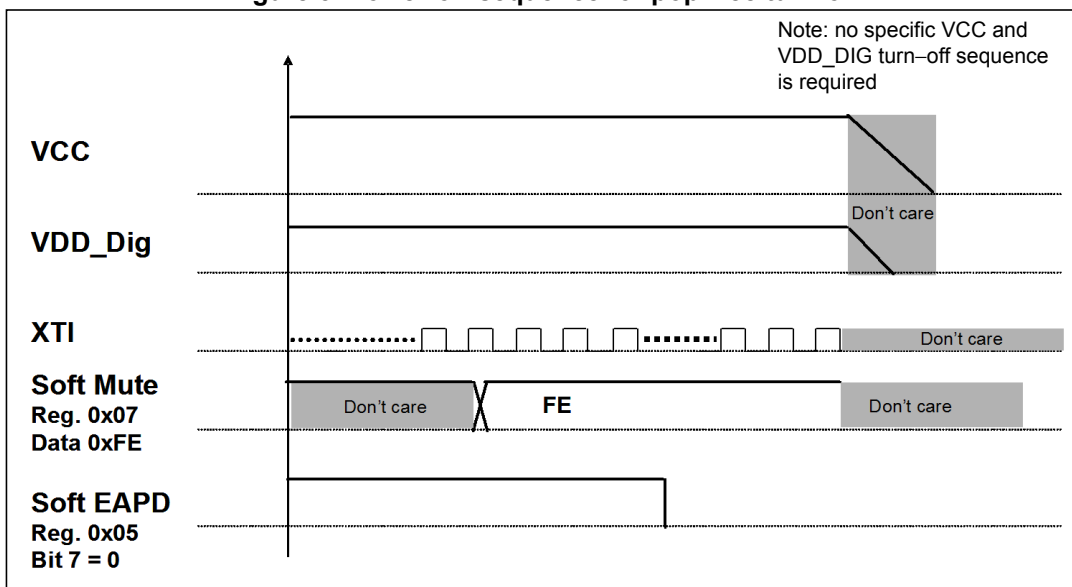
Figure 4. Power-on sequence



Note: The definition of a stable clock is when  $f_{max} - f_{min} < 1 \text{ MHz}$ .

Section [Serial audio input interface format on page 27](#) gives information on setting up the I²S interface.

Figure 5. Power-off sequence for pop-free turn-off



## 4 Serial audio interface

The STA339BWS audio serial input interface was designed to interface with standard digital audio components and to accept a number of serial data formats. The STA339BWS always acts as the slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using three inputs: left/right clock LRCKI, serial clock BICKI, and serial data SDI12.

The SAI bit and the SAIFB bit are used to specify the serial data format. The default serial data format is I<sup>2</sup>S, MSB-first.

### 4.0.1 Timings

In the STA339BWS the BICKI and LRCKI pins are configured as inputs and they must be supplied by the external peripheral.

Figure 6. Timing diagram for SAI interface

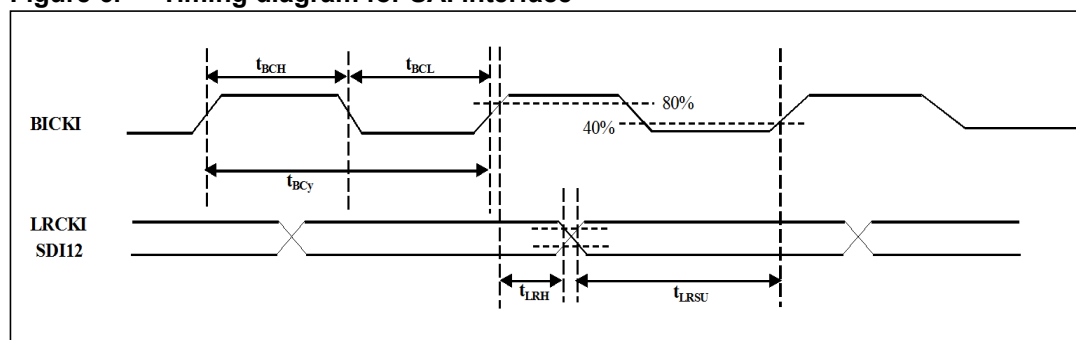


Table 8. Timing parameters for slave mode

Symbol	Parameter	Min	Typ	Max	Unit
t <sub>BCy</sub>	BICK cycle time	80	-	-	ns
t <sub>BCH</sub>	BICK pulse width high	40	-	-	ns
t <sub>BCL</sub>	BICK pulse width low	40	-	-	ns
t <sub>LRSU</sub>	LRCKI setup time to BICKI strobing edge	40	-	-	ns
t <sub>LRH</sub>	LRCKI hold time to BICKI strobing edge	40	-	-	ns
t <sub>LRJT</sub>	LRCKI Jitter Tolerance			40	ns

### 4.0.2 Delay serial clock enable

To tolerate anomalies in some I<sup>2</sup>S master devices, a PLL clock cycle delay can be added to the BICKI signal before the SAI interface.

### 4.0.3 Channel input mapping

Each channel received via I<sup>2</sup>S can be mapped to any internal processing channel via the channel input mapping registers. This allows for flexibility in processing. The default settings of these registers map each I<sup>2</sup>S input channel to its corresponding processing channel.



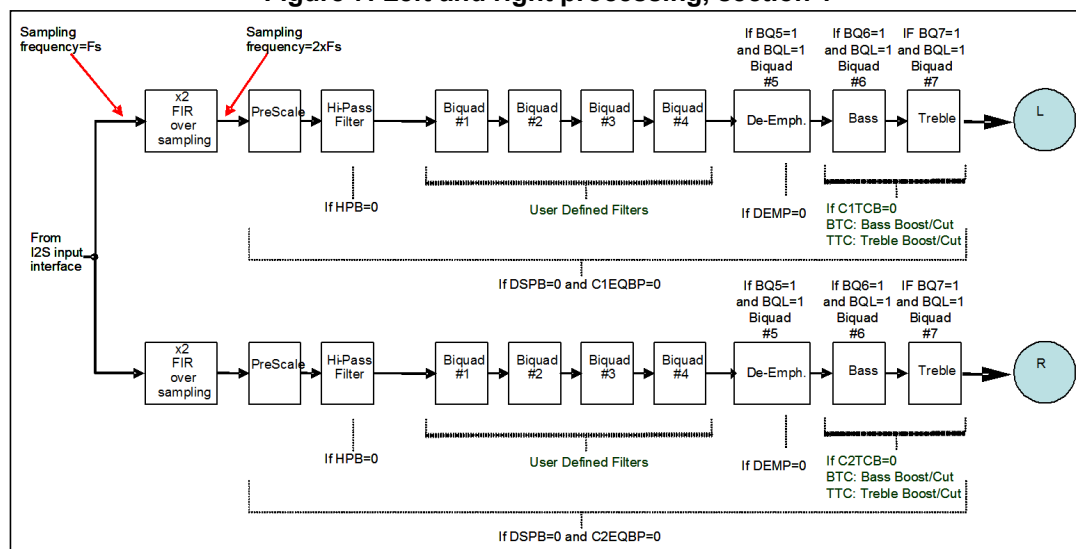
## 5 Processing data paths

Figure 7 and Figure 8 below show the data processing paths inside STA339BWS. The whole processing chain is composed of two consecutive sections. In the first one, dual-channel processing is implemented and in the second section each channel is fed into the post-mixing block either to generate a third channel (typically used in 2.1 output configuration and with crossover filters enabled) or to have the channels processed by the dual-band DRC block (2.0 output configuration with crossover filters used to define the cut-off frequency of the two bands).

The first section, Figure 7, begins with a 2x oversampling FIR filter providing  $2 * f_s$  audio processing. Then a selectable high-pass filter removes the DC level (enabled if HPB = 0). The left and right channel processing paths can include up to 8 filters, depending on the selected configuration (bits BQL, BQ5, BQ6, BQ7 and XO[3:0]). By default, four user programmable, independent filters per channel are enabled, plus the preconfigured de-emphasis, bass and treble controls (BQL = 0, BQ5 = 0, BQ6 = 0, BQ7 = 0).

If the coefficient sets for the two channels are linked (BQL = 1) it is possible to use the de-emphasis, bass and treble filters in a user defined configuration (provided the relevant BQx bits are set). In this case both channels use the same processing coefficients and can have up to seven filters each. If BQL = 0 the BQx bits are ignored and the fifth, sixth and seventh filters are configured as de-emphasis, bass and treble controls, respectively.

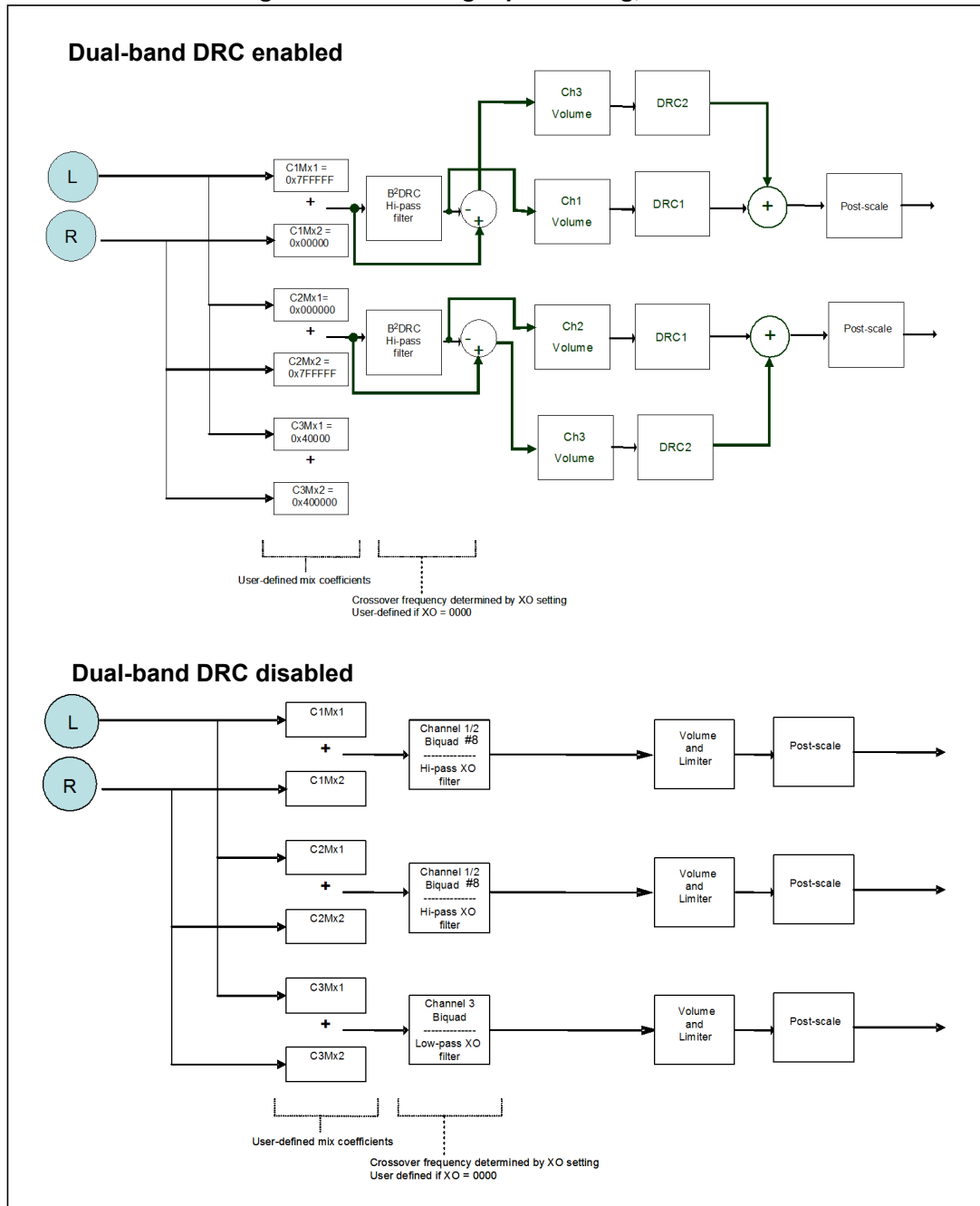
Figure 7. Left and right processing, section 1



Moreover, the common 8th filter can be available on both channels provided the predefined crossover frequencies are not used, XO[3:0] = 0, and the dual-band DRC is not used.

In the second section, Figure 8, mixing and crossover filters are available. If B<sup>2</sup>DRC is not enabled they are fully user-programmable and allow the generation of a third channel (2.1 outputs). Alternatively, in mode B<sup>2</sup>DRC, these blocks are used to split the sub-band and define the cut-off frequencies of the two bands. A prescaler and a final postscaler allow full control over the signal dynamics before and after the filtering stages. A mixer function is also available.

Figure 8. Left and right processing, section 2



## 6 I<sup>2</sup>C bus specification

The STA339BWS supports the I<sup>2</sup>C protocol via the input ports SCL and SDA\_IN (master to slave) and the output port SDA\_OUT (slave to master). This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA339BWS is always a slave device in all of its communications. It supports up to 400 kb/s (fast-mode bit rate).

For correct operation of the I<sup>2</sup>C interface ensure that the master clock generated by the PLL has a frequency at least 10 times higher than the frequency of the applied SCL clock.

### 6.1 Communication protocol

#### 6.1.1 Data transition or change

Data changes on the SDA line must only occur when the clock SCL is low. A SDA transition while the clock is high is used to identify a START or STOP condition.

#### 6.1.2 Start condition

START is identified by a high to low transition of the data bus, SDA, while the clock, SCL, is stable in the high state. A START condition must precede any command for data transfer.

#### 6.1.3 Stop condition

STOP is identified by low to high transition of SDA while SCL is stable in the high state. A STOP condition terminates communication between STA339BWS and the bus master.

#### 6.1.4 Data input

During the data input the STA339BWS samples the SDA signal on the rising edge of SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

### 6.2 Device addressing

To start communication between the master and the STA339BWS, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode bit.

The seven most significant bits are the device address identifiers, corresponding to the I<sup>2</sup>C bus definition. In the STA339BWS the I<sup>2</sup>C interface has two device addresses depending on the SA pin configuration, 0x38 when SA = 0, and 0x3A when SA = 1.

The eighth bit (LSB) identifies a read or write operation (R/W); this is set to 1 for read and to 0 for write. After a START condition the STA339BWS identifies the device address on the SDA bus and if a match is found, acknowledges the identification during the 9th bit time frame. The byte following the device identification is the address of a device register.

### 6.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA339BWS acknowledges this and then waits for the byte of internal address. After receiving the internal byte address the STA339BWS again responds with an acknowledgement.

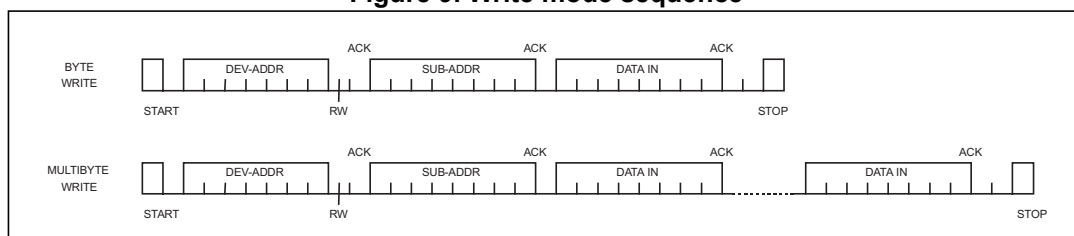
#### 6.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by the STA339BWS. The master then terminates the transfer by generating a STOP condition.

#### 6.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 9. Write mode sequence



### 6.4 Read operation

#### 6.4.1 Current address byte read

Following the START condition the master sends a device select code with the RW bit set to 1. The STA339BWS acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

#### 6.4.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA339BWS. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

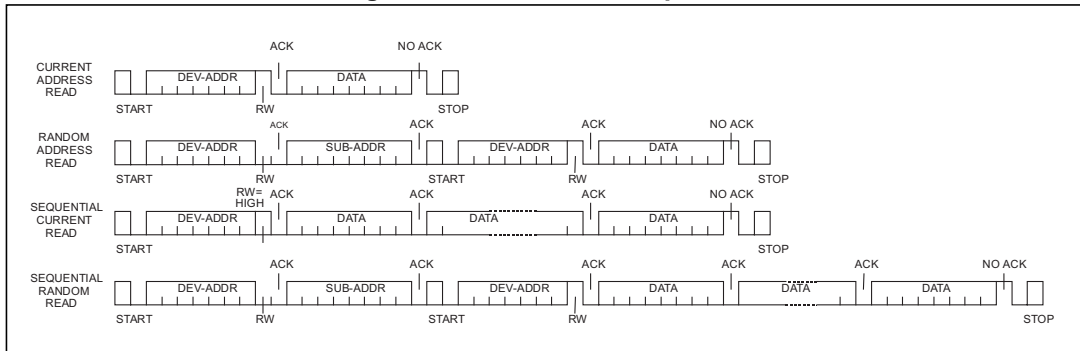
#### 6.4.3 Random address byte read

Following the START condition the master sends a device select code with the RW bit set to 0. The STA339BWS acknowledges this and then the master writes the internal address byte. After receiving, the internal byte address the STA339BWS again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA339BWS acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

### 6.4.4 Random address multi-byte read

The multi-byte read modes could start from any internal address. Sequential data bytes are read from sequential addresses within the STA339BWS. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

Figure 10. Read mode sequence





# 7 Register description

Note: Addresses exceeding the maximum address number must not be written.

**Table 9. Register summary**

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	CONFA	FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0x01	CONFB	C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	CONFC	OCRB	Reserved	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x03	CONFD	SME	ZDE	DRC	BQL	PSL	DSPB	DEMP	HPB
0x04	CONFE	SVE	ZCE	DCCV	PWMS	AME	NSBW	MPC	MPCV
0x05	CONFF	EAPD	PWDN	ECLE	LDTE	BCLE	IDE	OCFG1	OCFG0
0x06	MUTELOC	LOC1	LOC0	Reserved	Reserved	C3M	C2M	C1M	Reserved
0x07	MVOL	MVOL[7:0]							
0x08	C1VOL	C1VOL[7:0]							
0x09	C2VOL	C2VOL[7:0]							
0x0A	C3VOL	C3VOL[7:0]							
0x0B	AUTO1	Reserved	Reserved	AMGC[1:0]		Reserved	Reserved	Reserved	Reserved
0x0C	AUTO2	XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0x0D	AUTO3	Reserved							
0x0E	C1CFG	C10M1	C10M0	C1LS1	C1LS0	C1BO	C1VBP	C1EQBP	C1TCB
0x0F	C2CFG	C20M1	C20M0	C2LS1	C2LS0	C2BO	C2VBP	C2EQBP	C2TCB
0x10	C3CFG	C30M1	C30M0	C3LS1	C3LS0	C3BO	C3VBP	Reserved	Reserved
0x11	TONE	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0x12	L1AR	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x13	L1ATRT	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0x14	L2AR	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0x15	L2ATRT	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0x16	CFADDR	Reserved	Reserved	CFA[5:0]					
0x17	B1CF1	C1B[23:16]							
0x18	B1CF2	C1B[15:8]							
0x19	B1CF3	C1B[7:0]							
0x1A	B2CF1	C2B[23:16]							
0x1B	B2CF2	C2B[15:8]							
0x1C	B2CF3	C2B[7:0]							
0x1D	A1CF1	C3B[23:16]							
0x1E	A1CF2	C3B[15:8]							



Table 9. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x1F	A1CF3	C3B[7:0]							
0x20	A2CF1	C4B[23:16]							
0x21	A2CF2	C4B[15:8]							
0x22	A2CF3	C4B[7:0]							
0x23	B0CF1	C5B[23:16]							
0x24	B0CF2	C5B[15:8]							
0x25	B0CF3	C5B[7:0]							
0x26	CFUD	Reserved				RA	R1	WA	W1
0x27	MPCC1	MPCC[15:8]							
0x28	MPCC2	MPCC[7:0]							
0x29	DCC1	DCC[15:8]							
0x2A	DCC2	DCC[7:0]							
0x2B	FDRC1	FDRC[15:8]							
0x2C	FDRC2	FDRC[7:0]							
0x2D	STATUS	PLLUL	FAULT	UVFAULT	Reserved	OCFAULT	OCWARN	TFAULT	TWARN
0x2E	Reserved	Reserved							
0x2F	Reserved	Reserved							
0x30	Reserved	Reserved							
0x31	EQCFG	XOB	Reserved	Reserved	AMGC[3:2]		Reserved	SEL[1:0]	
0x32	EATH1	EATHEN1	EATH1[6:0]						
0x33	ERTH1	ERTHEN1	ERTH1[6:0]						
0x34	EATH2	EATHEN2	EATH2[6:0]						
0x35	ERTH2	ERTHEN2	ERTH2[6:0]						
0x36	CONFX	MDRC[1:0]		PS48DB	XAR1	XAR2	BQ5	BQ6	BQ7
0x37	SVCA	Reserved	Reserved	SVUPE	SVUP[4:0]				
0x38	SVCB	Reserved	Reserved	SVDWE	SVDW[4:0]				
0x39	RMS0A	R_C0[23:16]							
0x3A	RMS0B	R_C0[15:8]							
0x3B	RMS0C	R_C0[7:0]							
0x3C	RMS1A	R_C1[23:16]							
0x3D	RMS1B	R_C1[15:8]							
0x3E	RMS1C	R_C1[7:0]							

## 7.1 Configuration registers (addr 0x00 to 0x05)

### 7.1.1 Configuration register A (addr 0x00)

D7	D6	D5	D4	D3	D2	D1	D0
FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0	1	1	0	0	0	1	1

#### Master clock select

Table 10. Master clock select

Bit	R/W	RST	Name	Description
0	R/W	1	MCS0	Selects the ratio between the input I <sup>2</sup> S sample frequency and the input clock.
1	R/W	1	MCS1	
2	R/W	0	MCS2	

The STA339BWS supports sample rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz. Therefore the internal clock is:

- 32.768 MHz for 32 kHz
- 45.1584 MHz for 44.1 kHz, 88.2 kHz, and 176.4 kHz
- 49.152 MHz for 48 kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency ( $f_s$ ).

The relationship between the input clock and the input sample rate is determined by both the MCSx and the IR (input rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IR bit determines the oversampling ratio used internally.

Table 11. Input sampling rates

Input sample rate $f_s$ (kHz)	IR	MCS[2:0]					
		101	100	011	010	001	000
32, 44.1, 48	00	576 * $f_s$	128 * $f_s$	256 * $f_s$	384 * $f_s$	512 * $f_s$	768 * $f_s$
88.2, 96	01	NA	64 * $f_s$	128 * $f_s$	192 * $f_s$	256 * $f_s$	384 * $f_s$
176.4, 192	1X	NA	32 * $f_s$	64 * $f_s$	96 * $f_s$	128 * $f_s$	192 * $f_s$

#### Interpolation ratio select

Table 12. Internal interpolation ratio

Bit	R/W	RST	Name	Description
4:3	R/W	00	IR [1:0]	Selects internal interpolation ratio based on input I <sup>2</sup> S sample frequency