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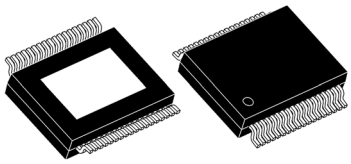
STA339BW

2.1-channel high-efficiency digital audio system

Datasheet - production data



PowerSSO-36 (slug down)

Features

- Wide voltage supply range
  - 5 V to 26 V (operating range)
  - 30 V (absolute maximum rating)
- 3 power output configurations
  - 2 channels of ternary PWM (stereo mode) (2 x 20 W into 8 Ω at 18 V)
  - 3 channels - left, right using binary and LFE using ternary PWM (2.1 mode) (2 x 9 W + 1 x 20 W into 2 x 4 Ω, 1 x 8 Ω at 18 V)
  - 2 channels of ternary PWM (2 x 20 W) + stereo lineout ternary
- 2.1 channels of 24-bit FFX® 100 dB SNR and dynamic range
- Selectable 32 to 192 kHz input sample rates
- I^2C control with selectable device address
- Digital gain/attenuation +48 dB to -80 dB with 0.5 dB/step resolution
- Soft volume update with programmable ratio
- Individual channel and master gain/attenuation
- Two independent DRC configurable as a dual-band anti-clipper (B^2DRC) or as independent limiters/compressors
- EQ-DRC for DRC based on filtered signals
- Dedicated LFE processing for bass boosting with 0.5 dB/step resolution
- Audio presets:
  - 15 preset crossover filters
  - 5 preset anti-clipping modes
  - Preset night-time listening mode
- Individual channel and master soft/hard mute
- Independent channel volume and DSP bypass
- Automatic zero-detect mute
- Automatic invalid input-detect mute
- 2-channel I^2S input data interface
- Input and output channel mapping
- Up to 8 user-programmable biquads per channel with 28-bit resolution
- 3 coefficient banks for EQ presets storing with fast recall via I^2C interface
- Bass/treble tones and de-emphasis control
- Selectable high-pass filter for DC blocking
- Advanced AM interference frequency switching and noise suppression modes
- Selectable high- or low-bandwidth noise-shaping topologies
- Variable max power correction for lower full-power THD
- Selectable clock input ratio
- 96 kHz internal processing sample rate, 24 to 28-bit precision
- Thermal overload and short-circuit protection embedded
- Video apps: 576 * f_S input mode supported
- Fully compatible with STA339BWS.

Table 1. Device summary

Order code	Package	Packaging
STA339BWTR	PowerSSO-36 slug down	Tape and reel

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1 Description

The STA339BW is an integrated solution of digital audio processing, digital amplifier control, and FFX-power output stage, thereby creating a high-power single-chip FFX® solution comprising high-quality, high-efficiency, all digital amplification.

STA339BW is based on FFX (fully flexible amplification) processor, an STMicroelectronics proprietary technology. FFX is the evolution and the enlargement of the ST ternary technology: the new processor can be configured to work in ternary, binary, binary differential and phase shift PWM modulation schemes.

STA339BW contains the ternary, binary and binary differential implementations, a subset of the full capability of the FFX processor.

The STA339BW is part of the Sound Terminal® family that provides full digital audio streaming to the speaker, offering cost effectiveness, low power dissipation and sound enrichment.

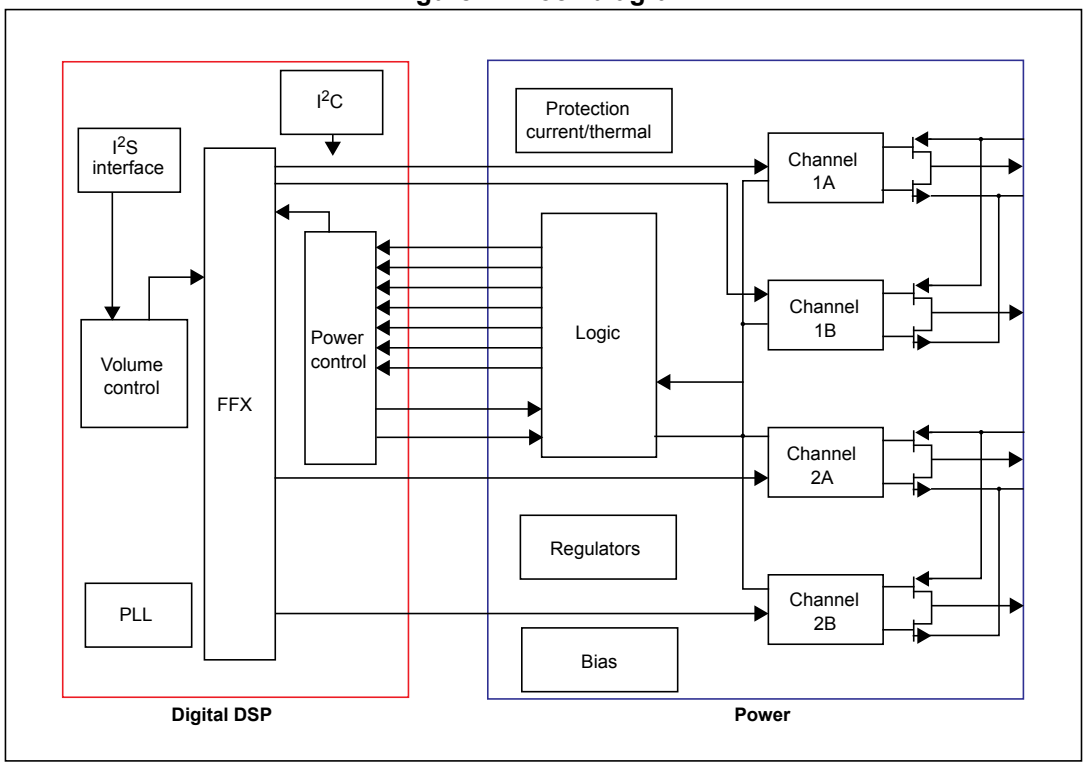
The STA339BW power section consists of four independent half bridges. These can be configured via digital control to operate in different modes. 2.1 channels can be provided by two half bridges and a single full bridge, providing up to 2 x 9 W + 1 x 20 W of power output. Two channels can be provided by two full bridges, providing up to 2 x 20 W of power. The IC can also be configured as 2.1 channels with 2 x 20 W provided by the device and external power for FFX power drive.

Also provided in the STA339BW are a full assortment of digital processing features. This includes up to 8 programmable 28-bit biquads (EQ) per channel and bass/treble tone control. Available presets enable a time-to-market advantage by substantially reducing the amount of software development needed for certain functions. This includes audio preset volume loudness, preset volume curves and preset EQ settings. There are also new advanced AM radio interference reduction modes. Dual-band DRC dynamically equalizes the system to provide speaker linear frequency response regardless of the output power level. This feature independently processes the two bands, controlling dynamically the output power level in each band and so providing better sound quality.

The serial audio data input interface accepts all possible formats, including the popular I^2S format. Three channels of FFX processing are provided. This high-quality conversion from PCM audio to FFX PWM switching waveform provides over 100 dB SNR and dynamic range.

1.1 Block diagram

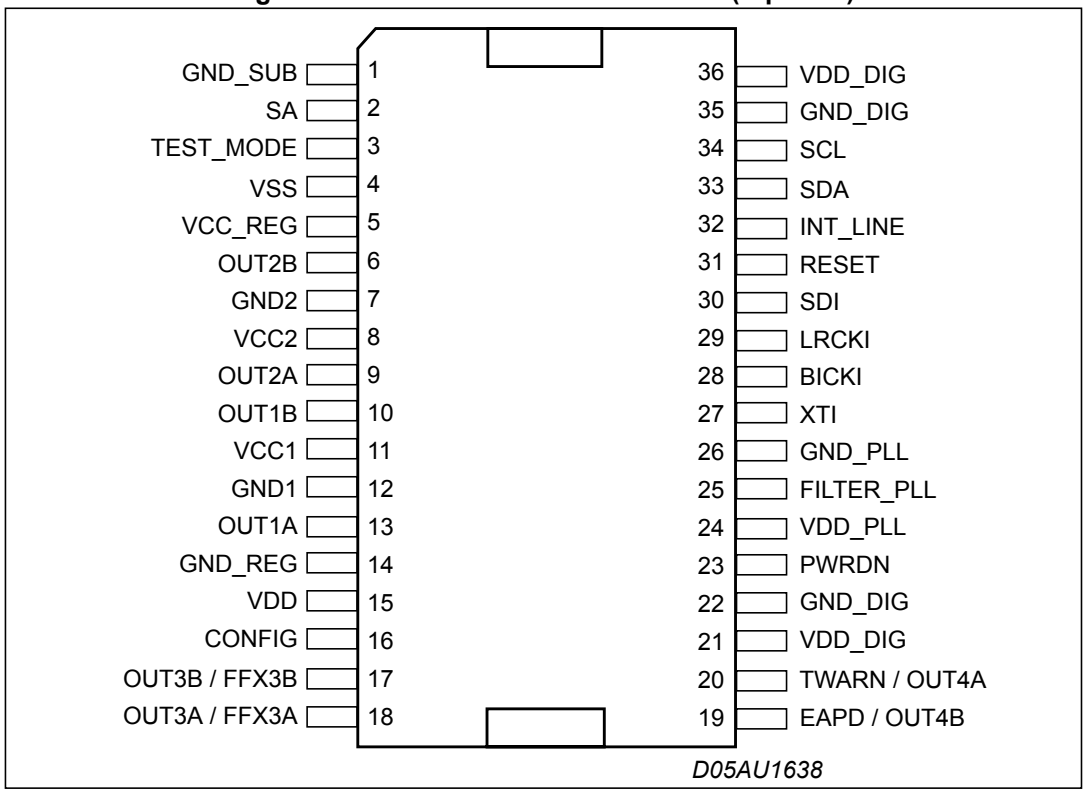
Figure 1. Block diagram



2 Pin connections

2.1 Connection diagram

Figure 2. Pin connection PowerSSO-36 (top view)



2.2 Pin description

Table 2. Pin description

Pin	Type	Name	Description
1	GND	GND_SUB	Substrate ground
2	I	SA	I^2C select address (pull-down)
3	I	TEST_MODE	This pin must be connected to ground (pull-down)
4	I/O	VSS	Internal reference at V_{CC} - 3.3 V
5	I/O	VCC_REG	Internal V_{CC} reference
6	O	OUT2B	Output half bridge 2B
7	GND	GND2	Power negative supply
8	Power	VCC2	Power positive supply
9	O	OUT2A	Output half bridge 2A
10	O	OUT1B	Output half bridge 1B

Table 2. Pin description (continued)

Pin	Type	Name	Description
11	Power	VCC1	Power positive supply
12	GND	GND1	Power negative supply
13	O	OUT1A	Output half bridge 1A
14	GND	GND_REG	Internal ground reference
15	Power	VDD	Internal 3.3 V reference voltage
16	I	CONFIG	Paralleled mode command
17	O	OUT3B / FFX3B	PWM out Ch3B / external bridge driver
18	O	OUT3A / FFX3A	PWM out Ch3A / external bridge driver
19	O	EAPD / OUT4B	Power down for external bridge / PWM out Ch4B
20	I/O	TWARN / OUT4A	Thermal warning from external bridge (pull-up when input) / PWM out Ch4A
21	Power	VDD_DIG	Digital supply voltage
22	GND	GND_DIG	Digital ground
23	I	PWRDN	Power down (pull-up)
24	Power	VDD_PLL	Positive supply for PLL
25	I	FILTER_PLL	Connection to PLL filter
26	GND	GND_PLL	Negative supply for PLL
27	I	XTI	PLL input clock
28	I	BICKI	I^2S serial clock
29	I	LRCKI	I^2S left/right clock
30	I	SDI	I^2S serial data channels 1 and 2
31	I	RESET	Reset (pull-up)
32	O	INT_LINE	Fault interrupt
33	I/O	SDA	I^2C serial data
34	I	SCL	I^2C serial clock
35	GND	GND_DIG	Digital ground
36	Power	VDD_DIG	Digital supply voltage

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power supply voltage (VCCxA, VCCxB)	-0.3	-	30	V
VDD_DIG	Digital supply voltage	-0.3	-	4	V
VDD_PLL	PLL supply voltage	-0.3	-	4	V
T_{op}	Operating junction temperature	-20	-	150	°C
T_{stg}	Storage temperature	-40	-	150	°C

Warning: **Stresses beyond those listed in *Table 3* above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended operating conditions" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, power supplies with nominal values rated within the recommended operating conditions, may experience some rising beyond the maximum operating conditions for a short time when no or very low current is sinked (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum ratings are not exceeded.**

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-case (thermal pad)	-	-	1.5	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient (1)	-	-	-	°C/W
$T_{th\text{-}sdj}$	Thermal shut-down junction temperature	-	150	-	°C
$T_{th\text{-}w}$	Thermal warning temperature	-	130	-	°C
$T_{th\text{-}sdh}$	Thermal shut-down hysteresis	-	20	-	°C

1. See *Section 9: Package thermal characteristics on page 74* for details.

3.3 Recommended operating conditions

Table 5. Recommended operating condition

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power supply voltage (VCCxA, VCCxB)	5	-	26	V
VDD_DIG	Digital supply voltage	2.7	3.3	3.6	V
VDD_PLL	PLL supply voltage	2.7	3.3	3.6	V
T_{amb}	Ambient temperature	-20	-	70	°C

3.4 Electrical specifications for the digital section

Table 6. Electrical specifications - digital section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Low-level input current without pull-up/down device	Vi = 0 V	-10	1	10	µA
I_{ih}	High-level input current without pull-up/down device	Vi = VDD_DIG = 3.6 V	-10	1	10	µA
V_{il}	Low-level input voltage	-	-	-	0.2 * VDD_DIG	V
V_{ih}	High-level input voltage	-	0.8 * VDD_DIG	-	-	V
V_{ol}	Low-level output voltage	Iol = 2 mA	-	-	0.4 * VDD_DIG	V
V_{oh}	High-level output voltage	Ioh = 2 mA	0.8 * VDD_DIG	-	-	V
I_{pu}	Pull-up/down current	-	25	66	125	µA
R_{pu}	Equivalent pull-up/down resistance	-	-	50	-	kΩ

3.5 Electrical specifications for the power section

The specifications given in this section are valid for the operating conditions: V_{CC} = 18 V, f = 1 kHz, f_{sw} = 384 kHz, T_{amb} = 25° C and R_L = 8 Ω, unless otherwise specified.

Table 7. Electrical specifications - power section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Po	Output power BTL	THD = 1%	-	16	-	W
		THD = 10%	-	20	-	
	Output power SE	THD = 1%	-	4	-	W
		THD = 10%	-	5	-	
R_{dsON}	Power Pchannel/Nchannel MOSFET (total bridge)	I_d = 1.5 A	-	180	250	mΩ
gP	Power Pchannel RdsON matching	I_d = 1.5 A	95	-	-	%
gN	Power Nchannel RdsON matching	I_d = 1.5 A	95	-	-	%
Idss	Power Pchannel/Nchannel leakage	V_{CC} = 20 V	-	-	10	µA
I_{LDT}	Low current dead time (static)	Resistive load(1)	-	8	15	ns
I_{HDT}	High current dead time (dynamic)	Iload = 1.5 A(1)	-	15	30	ns
t_r	Rise time	Resistive load(1)	-	10	18	ns
t_f	Fall time	Resistive load(1)	-	10	18	ns
V_{CC}	Supply voltage operating voltage	-	5	-	26	V
I_{vcc}	Supply current from V_{CC} in power down	PWRDN = 0	-	0.1	1	mA
	Supply current from V_{CC} in operation	PCM input signal = -60 dBfs, Switching frequency = 384 kHz, No LC filters	-	52	60	mA
I_{vdd}	Supply current FFX processing (reference only)	Internal clock = 49.152 MHz	-	55	70	mA
I_{lim}	Overcurrent limit	(2)	3.0	3.8(3)	-	A
I_{sc}	Short-circuit protection	Hi-Z output	3.8	4.8	-	A
UVL	Undervoltage protection	-	-	3.5	4.3	V
t_{min}	Output minimum pulse width	No load	20	30	60	ns
DR	Dynamic range	-	-	100	-	dB
SNR	Signal-to-noise ratio, ternary mode	A-weighted	-	100	-	dB
	Signal-to-noise ratio binary mode	-	-	90	-	dB
PSSR	Power supply rejection ratio	FFX stereo mode, <5 kHz V_{RIPPLE} = 1 V RMS Audio input = dither only	-	80	-	dB

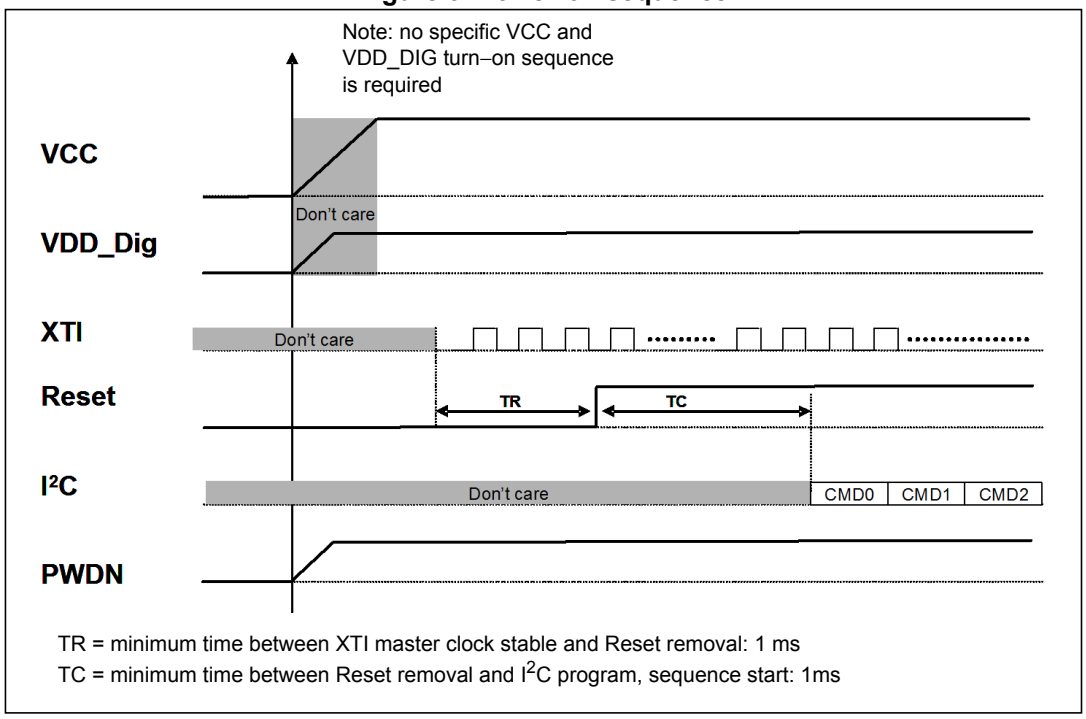
Table 7. Electrical specifications - power section (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD+N	Total harmonic distortion + noise	FFX stereo mode, Po = 1 W f = 1 kHz	-	0.2	-	%
X_{TALK}	Crosstalk	FFX stereo mode, <5 kHz One channel driven at 1 W Other channel measured	-	80	-	dB
η	Peak efficiency, FFX mode	Po = 2 x 20 W into 8 Ω	-	90	-	%
	Peak efficiency,binary modes	Po = 2 x 9 W into 4 Ω + 1 x 20 W into 8 Ω	-	87	-	

1. Refer to *Figure 5: Test circuit 1*.
2. Limit current if the register (OCRB par 6.1.3.3) overcurrent warning detect adjustment bypass is enabled. When disabled, refer to I_{sc}.
3. I_{lim} typical value is $0.8*I_{sc}$.

3.6 Power on/off sequence

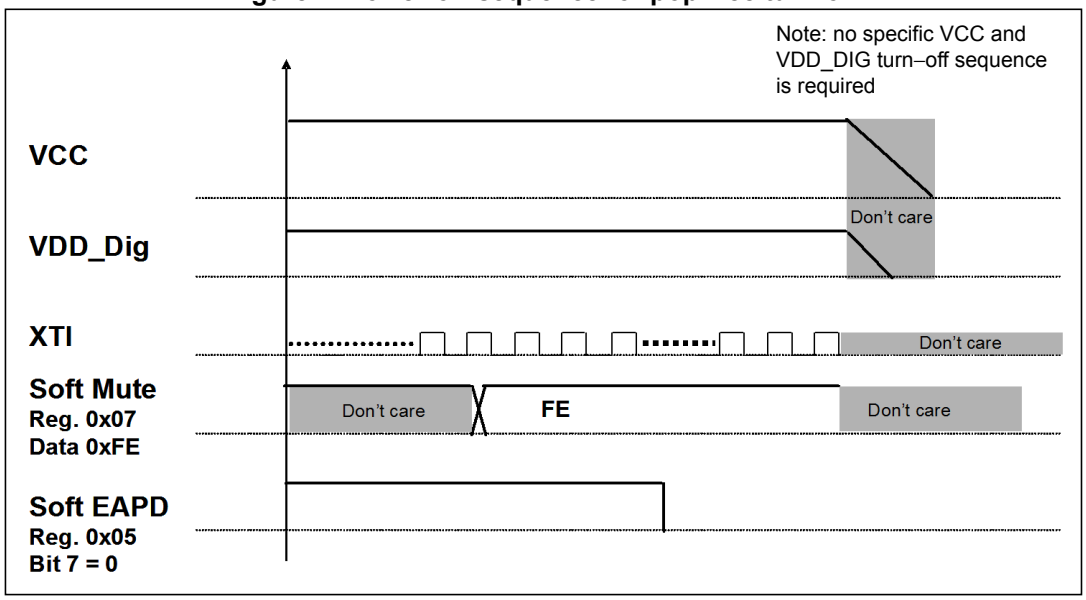
Figure 3. Power-on sequence



Note: The definition of a stable clock is when f_{max} - f_{min} < 1 MHz.

Section 7.2.3 on page 31 gives information on setting up the I²S interface.

Figure 4. Power-off sequence for pop-free turn-off



3.7 Testing

3.7.1 Functional pin definition

Table 8. Functional pin definition

Pin name	Number	Logic value	IC status
PWRDN	23	0	Low consumption
		1	Normal operation
TWARN	20	0	A temperature warning is indicated by the external power stage
		1	Normal operation
EAPD	19	0	Low consumption for power stage All internal regulators are switched off
		1	Normal operation

Figure 5. Test circuit 1

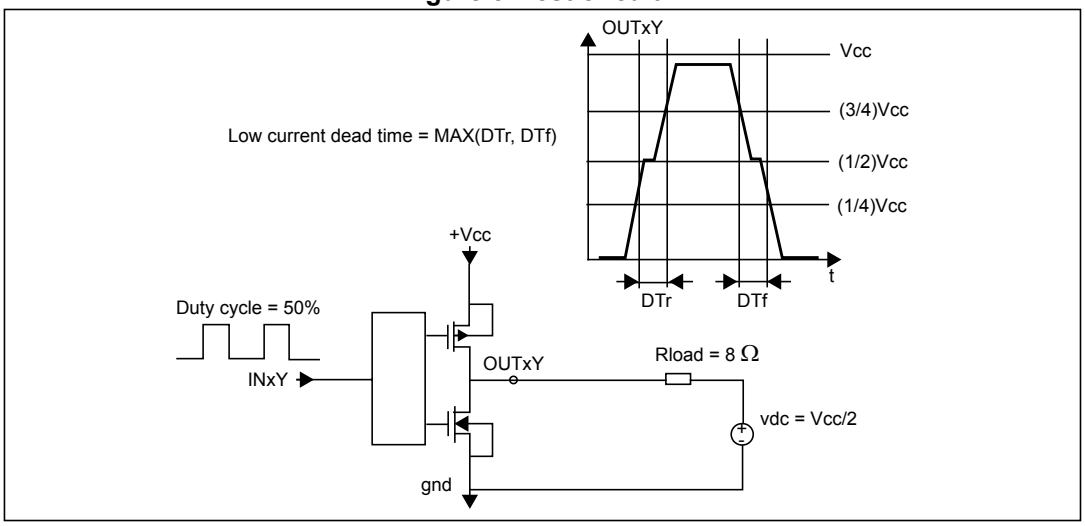
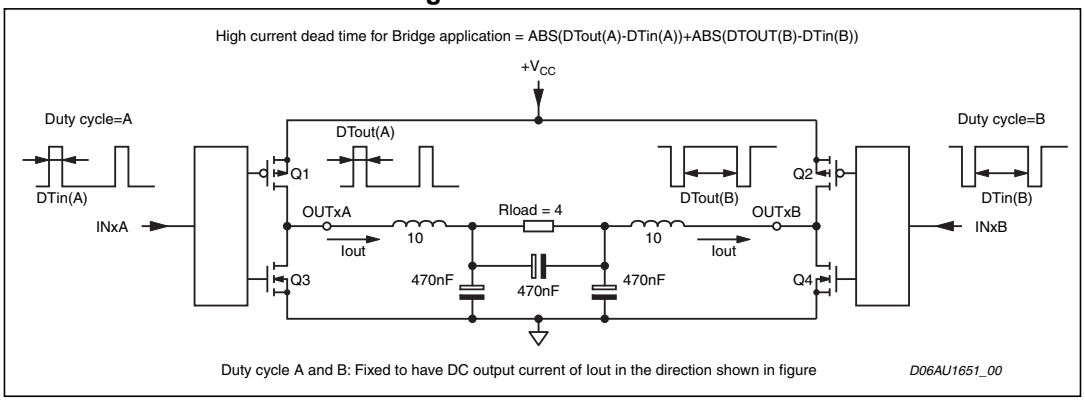


Figure 6. Test circuit 2



4 Serial audio interface

The STA339BW audio serial input interface was designed to interface with standard digital audio components and to accept a number of serial data formats. The STA339BW always acts as the slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using three inputs: left/right clock LRCKI, serial clock BICKI, and serial data SDI12.

The SAI bit and the SAIFB bit are used to specify the serial data format. The default serial data format is I^2S, MSB-first.

4.0.1 Timings

In the STA339BW the BICKI and LRCKI pins are configured as inputs and they must be supplied by the external peripheral.

Figure 7. Timing diagram for SAI interface

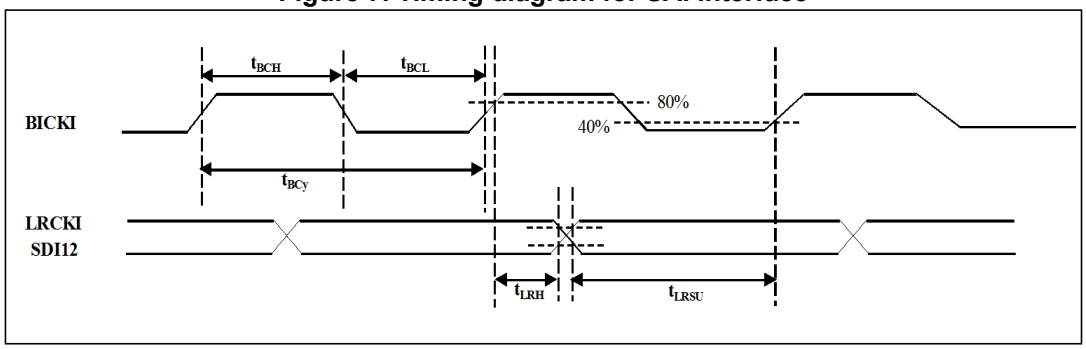


Table 9. Timing parameters for slave mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{BCy}	BICK cycle time	80	-	-	ns
t_{BCH}	BICK pulse width high	40	-	-	ns
t_{BCL}	BICK pulse width low	40	-	-	ns
t_{LRSU}	LRCKI setup time to BICKI strobing edge	40	-	-	ns
t_{LRH}	LRCKI hold time to BICKI strobing edge	40	-	-	ns
t_{LRJT}	LRCKI Jitter Tolerance			40	ns

4.0.2 Delay serial clock enable

To tolerate anomalies in some I^2S master devices, a PLL clock cycle delay can be added to the BICKI signal before the SAI interface.

4.0.3 Channel input mapping

Each channel received via I^2S can be mapped to any internal processing channel via the channel input mapping registers. This allows for flexibility in processing. The default settings of these registers map each I^2S input channel to its corresponding processing channel.

5 Processing data paths

The whole processing chain is composed of two consecutive sections. In the first one dual-channel processing is implemented, as described below. Then each channel is fed into the post-mixing block where there is a choice of processing, either the dual-band DRC is disabled or it is enabled. When B^2DRC is disabled a third channel, typically used in 2.1 output configuration and with cross-over filters enabled, is used. When B^2DRC is enabled the 2.0 output configuration with cross-over filters for defining the cutoff frequency of the two bands is used.

The first section, *Figure 8*, begins with a 2x oversampling FIR filter allowing a 2 * fs audio processing. Then a selectable high-pass filter removes the DC level (enabled if HFB = 0).

The channel 1 and 2 processing chain can include up to 8 filters, depending on the selected configuration (bits BQL, BQ5, BQ6, BQ7 and XO[3:0]).

By default, four independent filters per channel are enabled, plus the preconfigured de-emphasis, bass and treble controls (BQL = 0, BQ5 = 0, BQ6 = 0, BQ7 = 0).

If the coefficient sets are linked (BQL = 1) then it is possible to use the de-emphasis, bass and treble filter in a user defined configuration (provided the relevant BQx bits are set to 1). In other words both channels use the same processing coefficients and can have up to 7 filters each. Note that if BQL = 0 the BQx bits are ignored and the 5th, 6th and 7th filters are configured as de-emphasis, bass and treble controls, respectively.

Moreover the common 8th filter, from the subsequent processing section, can be available on both channels (provided the pre-defined cross-over frequencies are not used, XO[3:0] = 0, and the dual-band DRC is not used).

In the second section, mixing and crossover filters are available. If B^2DRC is not enabled (lower schematic in *Figure 9*) they are fully user-programmable and allow a third channel (2.1 outputs) to be generated. Alternatively, in B^2DRC mode (upper schematic in *Figure 9*), those blocks will be used to split the sub-band and define the cutoff frequencies of the two bands. A prescaler and a final post scaler allow full control over the signal dynamics before and after, respectively, the filtering stages. A mixer function is also available.

Figure 8. Left and right processing part 1

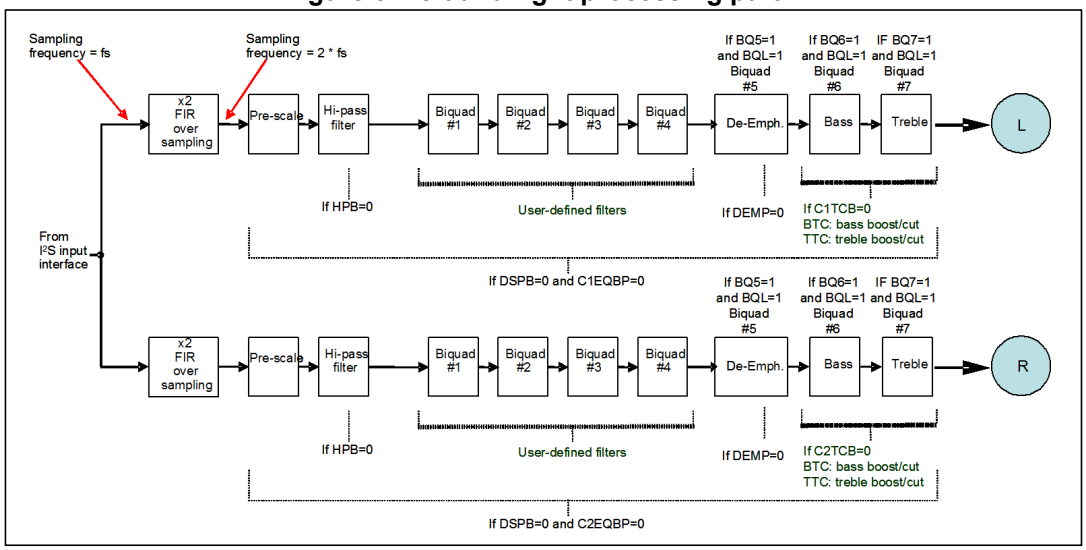
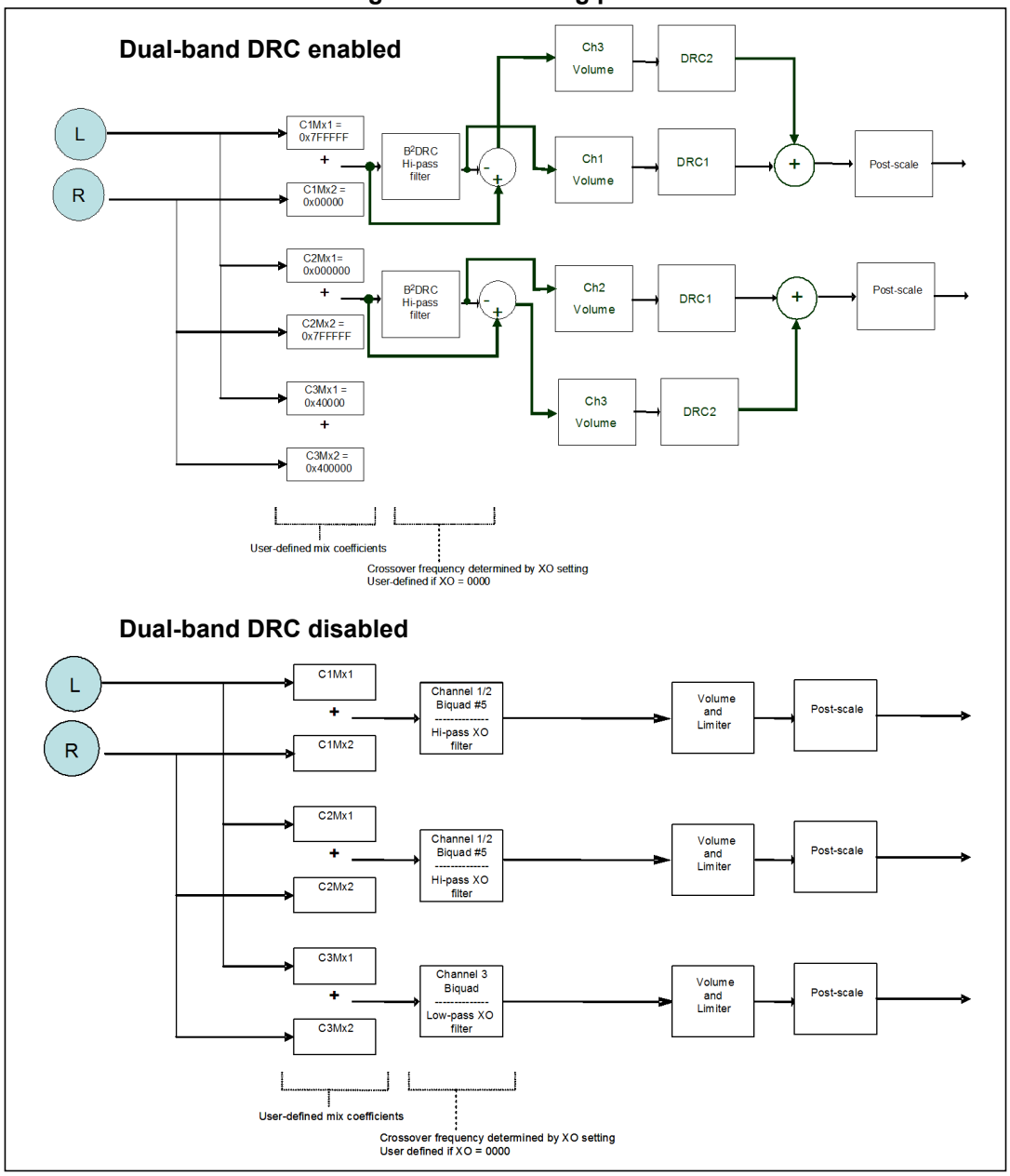


Figure 9. Processing part 2



6 I²C bus specification

The STA339BW supports the I²C protocol via the input ports SCL and SDA_IN (master to slave) and the output port SDA_OUT (slave to master). This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA339BW is always a slave device in all of its communications. It can operate at up to 400 kb/s (fast-mode bit rate). The STA339BW I²C interface is a slave only interface.

6.1 Communication protocol

6.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

6.1.2 Start condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

6.1.3 Stop condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between STA339BW and the bus master.

6.1.4 Data input

During the data input the STA339BW samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

6.2 Device addressing

To start communication between the master and the STA339BW, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode.

The seven most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA339BW the I²C interface has two device addresses depending on the SA port configuration, 0x38 when SA = 0, and 0x3A when SA = 1.

The eighth bit (LSB) identifies read or write operation RW, this bit is set to 1 in read mode and to 0 for write mode. After a START condition the STA339BW identifies on the bus the device address and if a match is found, acknowledges the identification on the SDA bus during the 9th bit time. The byte following the device identification byte is the internal space address.

6.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA339BW acknowledges this and the writes for the byte of internal address. After receiving the internal byte address the STA339BW again responds with an acknowledgement.

6.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by the STA339BW. The master then terminates the transfer by generating a STOP condition.

6.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

6.4 Read operation

6.4.1 Current address byte read

Following the START condition the master sends a device select code with the RW bit set to 1. The STA339BW acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

6.4.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA339BW. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

6.4.3 Random address byte read

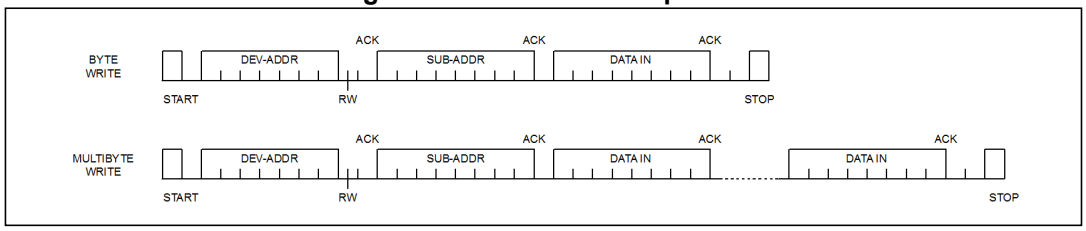
Following the START condition the master sends a device select code with the RW bit set to 0. The STA339BW acknowledges this and then the master writes the internal address byte. After receiving, the internal byte address the STA339BW again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA339BW acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

6.4.4 Random address multi-byte read

The multi-byte read modes could start from any internal address. Sequential data bytes are read from sequential addresses within the STA339BW. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

6.4.5 Write mode sequence

Figure 10. Write mode sequence



6.4.6 Read mode sequence

Figure 11. Read mode sequence