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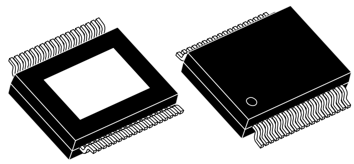
2.1-channel high-efficiency digital audio system Sound Terminal®

Datasheet - production data



PowerSSO-36
with exposed pad down (EPD)

Features

- Wide-range supply voltage
  – 5 V to 26 V (operating range)
  – 30 V (absolute maximum rating)
- Four power output configurations
  – 2 channels of ternary PWM (stereo mode) (2 x 30 W into 8 Ω at 22 V)
  – 3 channels - left, right using binary and LFE using ternary PWM (2.1 mode) (2 x 15 W + 1 x 30 W into 2 x 4Ω, 1 x 8 Ω at 22 V)
  – 2 channels of ternary PWM (2 x 30 W) + stereo lineout ternary)
- FFX® 100 dB SNR and dynamic range
- Selectable 32 to 192 kHz input sampling rates
- I^2C control with selectable device address
- Digital gain/attenuation +42 dB to -80 dB with 0.125 dB/step resolution
- Soft-volume update with programmable ratio
- Individual channel and master gain/attenuation
- Two independent DRCs configurable as a dual-band anti-clipper (B^2DRC) or independent limiters/compressors
- EQ-DRC for DRC based on filtered signals
- Dedicated LFE processing for bass boosting with 0.125 dB/step resolution
- Audio presets:
  – 15 preset crossover filters
  – 5 preset anti-clipping modes
  – Preset nighttime listening mode
- Individual channel and master soft/hard mute
- Independent channel volume and DSP bypass
- Automatic zero-detect mute
- Automatic invalid input-detect mute
- I^2S input data interface
- Input and output channel mapping
- Up to 8 user-programmable biquads per channel
- 3 coefficient banks for EQ presets storing with fast recall via I^2C interface
- Extended coefficient dynamic up to -4..4 for easy implementation of high shelf filters
- Bass/treble tones and de-emphasis control
- Selectable high-pass filter for DC blocking
- Advanced AM interference frequency switching and noise suppression modes
- Selectable high- or low-bandwidth noise-shaping topologies
- Selectable clock input ratio
- 96 kHz internal processing sampling rate with quantization error noise shaping for very low cutoff frequency filters
- Thermal overload and short-circuit protection embedded
- Video apps: 576 x Fs input mode supported
- Fully compatible with STA339BW, STA369BWS and STA350BW

Table 1. Device summary

Order code	Package	Packing
STA369BW	Power SSO-36	Tube
STA369BWTR	Power SSO-36	Tape and reel

Contents

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1 Description

The STA369BW is an integrated solution of digital audio processing, digital amplifier control, and FFX-power output stage, thereby creating a high-power single-chip FFX® solution comprising high-quality, high-efficiency, and all-digital amplification.

The STA369BW is based on an FFX (fully flexible amplification) processor, a proprietary technology from STMicroelectronics. FFX is the evolution and the enlargement of ST's ternary technology: the new processor can be configured to work in ternary, binary, binary differential and phase-shift PWM modulation schemes.

The STA369BW contains the ternary, binary and binary differential implementations, a subset of the full capability of the FFX processor.

The STA369BW is part of the Sound Terminal® family that provides full digital audio streaming to the speaker, offering cost effectiveness, low power dissipation and sound enrichment.

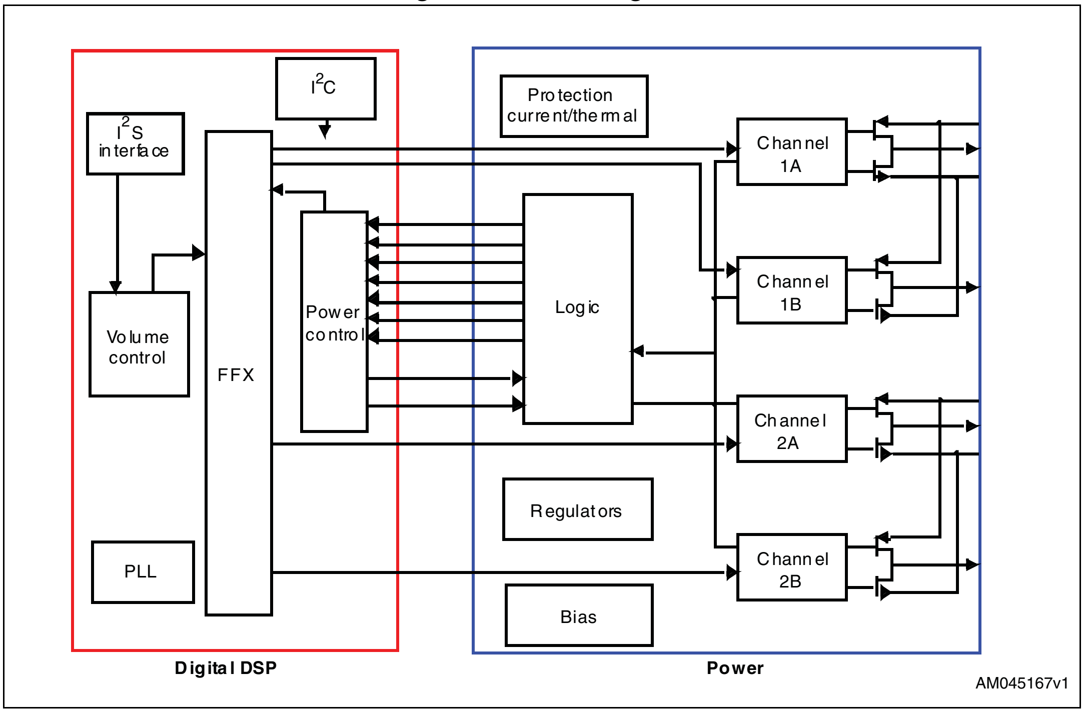
The STA369BW power section consists of four independent half-bridges. These can be configured via digital control to operate in different modes. 2.1 channels can be provided by two half-bridges and a single full-bridge, providing up to 2 x 15 W + 1 x 30 W of music output power, by using standard 4 and 8 Ω speakers. Two channels can be provided by two full-bridges, providing up to 2 x 30 W, by using standard 8 Ω speaker at 22 V. The IC can also be configured as 2.1 channels with 2 x 30 W provided by the device and external power for FFX power drive. Please refer to the package thermal characteristics and application suggestions for more details.

Also provided in the STA369BW are a full assortment of digital processing features. This includes up to 8 programmable biquads (EQ) per channel. Special digital signal processing techniques are available in order to manage low-frequency quantization noise in case of very low frequency cutoff filter thresholds. The coefficient range -4..4 allows the easy implementation of high shelf filters. Available presets allow the advantage of earlier time-to-market by substantially reducing the amount of software development needed for certain functions. This includes audio preset volume loudness, preset volume curves and preset EQ settings. There are also new advanced AM radio interference reduction modes. The dual-band DRC dynamically equalizes the system to provide speaker linear frequency response regardless of output power level. This feature independently processes the two bands, controlling dynamically the output power level in each band, thus providing better sound clarity.

The serial audio data input interface accepts all possible formats, including the popular I^2S format. Three channels of FFX processing are provided. This high-quality conversion from PCM audio to FFX PWM switching waveform provides over 100 dB SNR and dynamic range.

1.1 Block diagram

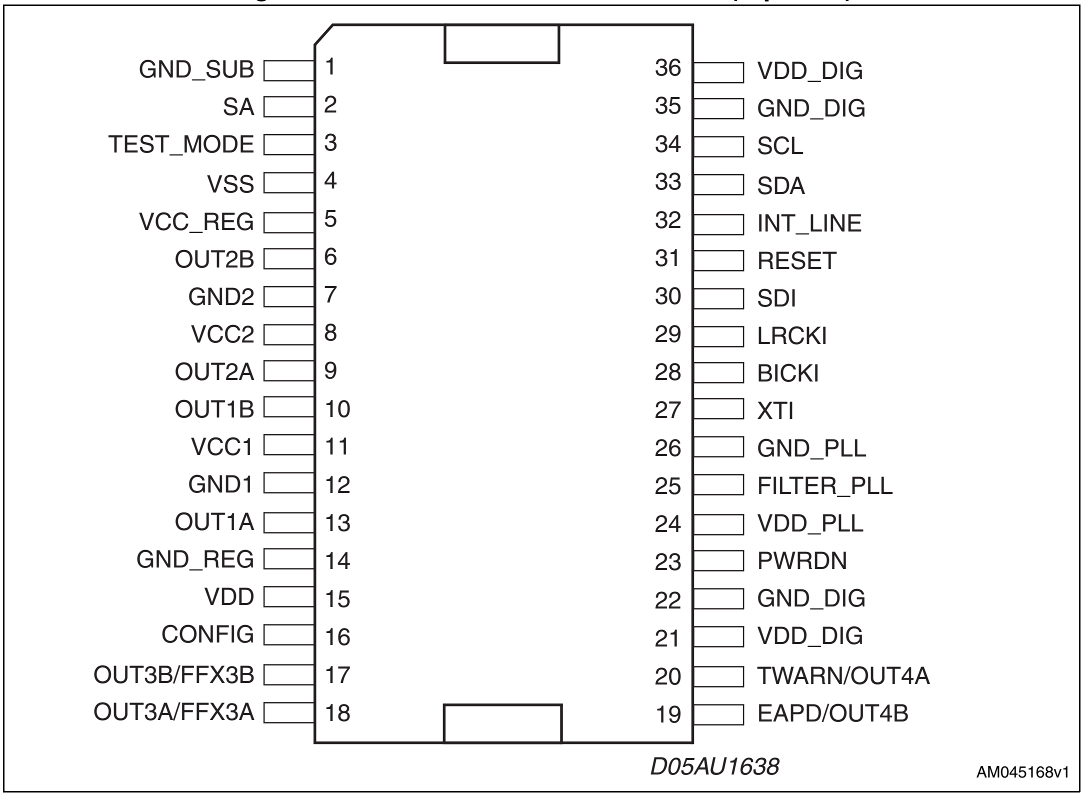
Figure 1. Block diagram



2 Pin connections

2.1 Connection diagram

Figure 2. Pin connection PowerSSO-36 (top view)



2.2 Pin description

Table 2. Pin description

Pin	Type	Name	Description
1	GND	GND_SUB	Substrate ground
2	I	SA	I^2C select address (pull-down)
3	I	TEST_MODE	This pin must be connected to ground (pull-down)
4	I/O	VSS	Internal reference at Vcc-3.3 V
5	I/O	VCC_REG	Internal Vcc reference
6	O	OUT2B	Output half-bridge 2B
7	GND	GND2	Power negative supply
8	Power	VCC2	Power positive supply
9	O	OUT2A	Output half-bridge 2A
10	O	OUT1B	Output half-bridge 1B

Table 2. Pin description (continued)

Pin	Type	Name	Description
11	Power	VCC1	Power positive supply
12	GND	GND1	Power negative supply
13	O	OUT1A	Output half-bridge 1A
14	GND	GND_REG	Internal ground reference
15	Power	VDD	Internal 3.3 V reference voltage
16	I	CONFIG	Parallel mode command
17	O	OUT3B/FFX3B	PWM out CH3B / external bridge driver
18	O	OUT3A/FFX3A	PWM out CH3A / external bridge driver
19	O	EAPD/OUT4B	Power-down for external bridge / PWM out CH4B
20	I/O	TWARN/OUT4A	Thermal warning from external bridge (pull-up when input) / PWM out CH4A
21	Power	VDD_DIG	Digital supply voltage
22	GND	GND_DIG	Digital ground
23	I	PWRDN	Power down (pull-up)
24	Power	VDD_PLL	Positive supply for PLL
25	I	FILTER_PLL	Connection to PLL filter
26	GND	GND_PLL	Negative supply for PLL
27	I	XTI	PLL input clock
28	I	BICKI	I^2S serial clock
29	I	LRCKI	I^2S left/right clock
30	I	SDI	I^2S serial data channels 1 and 2
31	I	RESET	Reset (pull-up)
32	O	INT_LINE	Fault interrupt
33	I/O	SDA	I^2C serial data
34	I	SCL	I^2C serial clock
35	GND	GND_DIG	Digital ground
36	Power	VDD_DIG	Digital supply voltage

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{cc}	Power supply voltage (VCCxA, VCCxB)	-0.3		30	V
VDD_DIG	Digital supply voltage	-0.3		4	V
VDD_PLL	PLL supply voltage	-0.3		4	
T_{op}	Operating junction temperature	-20		150	°C
T_{stg}	Storage temperature	-40		150	°C

Warning: Stresses beyond those listed in *Table 3* above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended operating conditions" are not implied. Exposure to AMR conditions for extended periods may affect device reliability. In the real application, power supplies with nominal values rated within the recommended operating conditions, may rise beyond the maximum operating conditions for a short time when no or very low current is sunk (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum ratings are not exceeded.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-case (thermal pad)			1.5	°C/W
$T_{th\text{-}sdj}$	Thermal shutdown junction temperature		150		°C
$T_{th\text{-}w}$	Thermal warning temperature		130		°C
$T_{th\text{-}sdh}$	Thermal shutdown hysteresis		20		°C
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient (1)				

1. See *Section 10: Package thermal characteristics on page 85* for details.

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{cc}	Power supply voltage (VCCxA, VCCxB)	5		26	V
VDD_DIG	Digital supply voltage	2.7	3.3	3.6	V
VDD_PLL	PLL supply voltage	2.7	3.3	3.6	V
T_{amb}	Ambient temperature	-20		+85	°C

3.4 Electrical specifications for the digital section

Table 6. Electrical specifications - digital section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Low-level input current without pull-up/down device	Vi = 0 V		1	5	µA
I_{ih}	High-level input current without pull-up/down device	Vi = VDD_DIG = 3.6 V		1	5	µA
V_{il}	Low-level input voltage				0.2 * VDD_DIG	V
V_{ih}	High-level input voltage		0.8 * VDD_DIG			V
V_{ol}	Low-level output voltage	Iol=2 mA			0.4 * VDD_DIG	V
V_{oh}	High-level output voltage	Ioh=2 mA	0.8 * VDD_DIG			V
I_{pu}	Pull-up/down current		25	66	125	µA
R_{pu}	Equivalent pull-up/down resistance			50		kΩ

3.5 Electrical specifications for the power section

The specifications given in this section are valid for the operating conditions: V_{CC} = 22 V, f = 1 kHz, f_{sw} = 384 kHz, T_{amb} = 25° C and R_L = 8 Ω, unless otherwise specified.

Table 7. Electrical specifications - power section

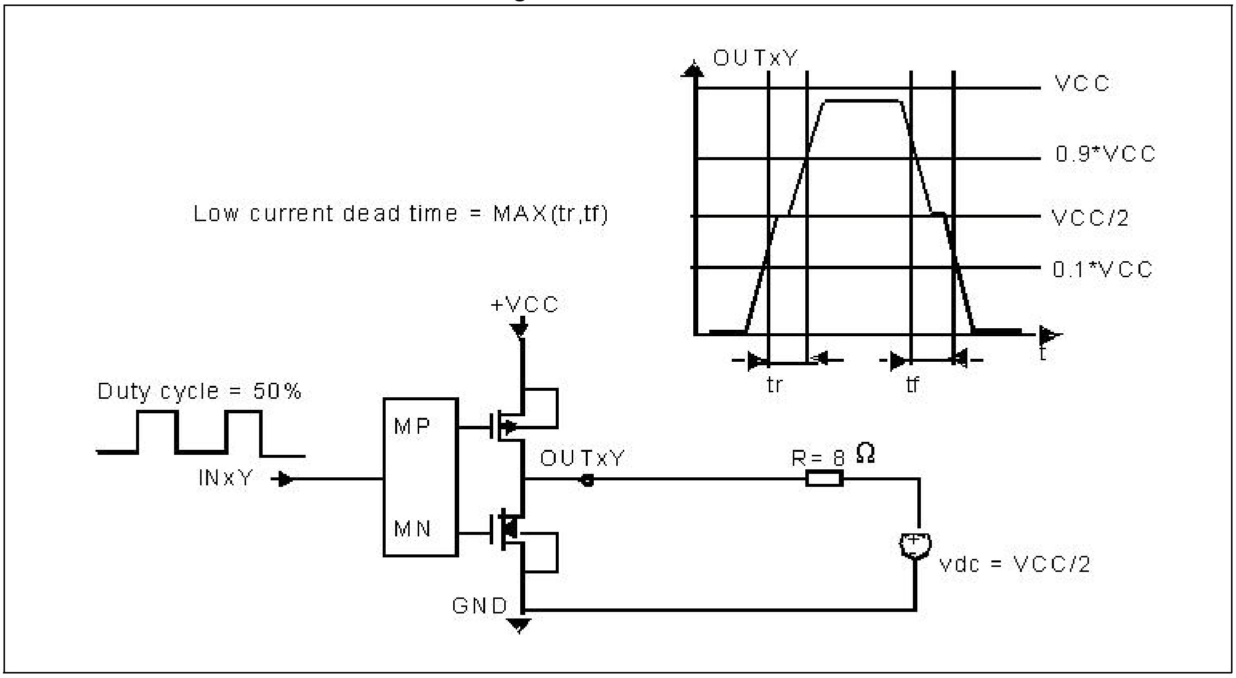
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Po	Continuous output power, BTL, ternary mode	THD = 1%		20		W
		THD = 10%		30		
	Continuous output power SE, binary mode, R_L = 4 Ω	THD = 1%		12		W
		THD = 10%		15		
R_{dsON}	Power Pchannel/Nchannel MOSFET (total bridge)	I_d = 1.5 A		180	250	mΩ
Idss	Power Pchannel/Nchannel leakage	VCC = 20 V			10	µA
I_{LDT}	Low current dead time (static)	Resistive load(1)		8	15	ns
I_{HDT}	High current dead time (dynamic)	I load(1) = 1.5 A		15	30	ns
t_r	Rise time	Resistive load(1)		10	18	ns
t_f	Fall time	Resistive load(1)		10	18	ns
V_{cc}	Supply voltage operating voltage		5		26	V
I_{vcc}	Supply current from Vcc in power-down	PWRDN = 0		1		µA
	Supply current from Vcc in operation	PCM input signal = -60 dBfs, Switching frequency = 384 kHz, No LC filters		52	60	mA
I_{vdd}	Supply current FFX processing (reference only)	Internal clock = 49.152 MHz		55	70	mA
Ilim	Overcurrent limit	(2)	2.6	2.8		A
Isc	Short-circuit protection	Hi-Z output	3.1	3.3		A
UVL	Undervoltage protection				4.3	V
OVP	Overvoltage protection			29		V
t_{min}	Output minimum pulse width	No load		100		ns
DR	Dynamic range			100		dB
SNR	Signal-to-noise ratio, ternary mode	A-Weighted		100		dB
	Signal-to-noise ratio binary mode			90		dB
THD+N	Total harmonic distortion + noise	FFX stereo mode, Po = 1 W f = 1 kHz		0.09		%

Table 7. Electrical specifications - power section (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
X_{TALK}	Crosstalk	FFX stereo mode, <5 kHz One channel driven at 1 W Other channel measured		80		dB
PSRR	Power Supply Rejection Ratio	FFX stereo mode, <5 kHz VRipple01V RMS Audio input = dither only		80		dB
η	Peak efficiency, FFX mode	Po = 2 x 25 W into 8 Ω		90		%
	Peak efficiency, binary modes	Po = 2 x 10W into 4Ω + 1 x 20W into 8 Ω		86		

1. Refer to *Figure 3: Test circuit*.
2. Limit current if the register (OCRB *Section 8.3.3*) overcurrent warning detect adjustment bypass is enabled. When disabled refer to the Isc.

Figure 3. Test circuit

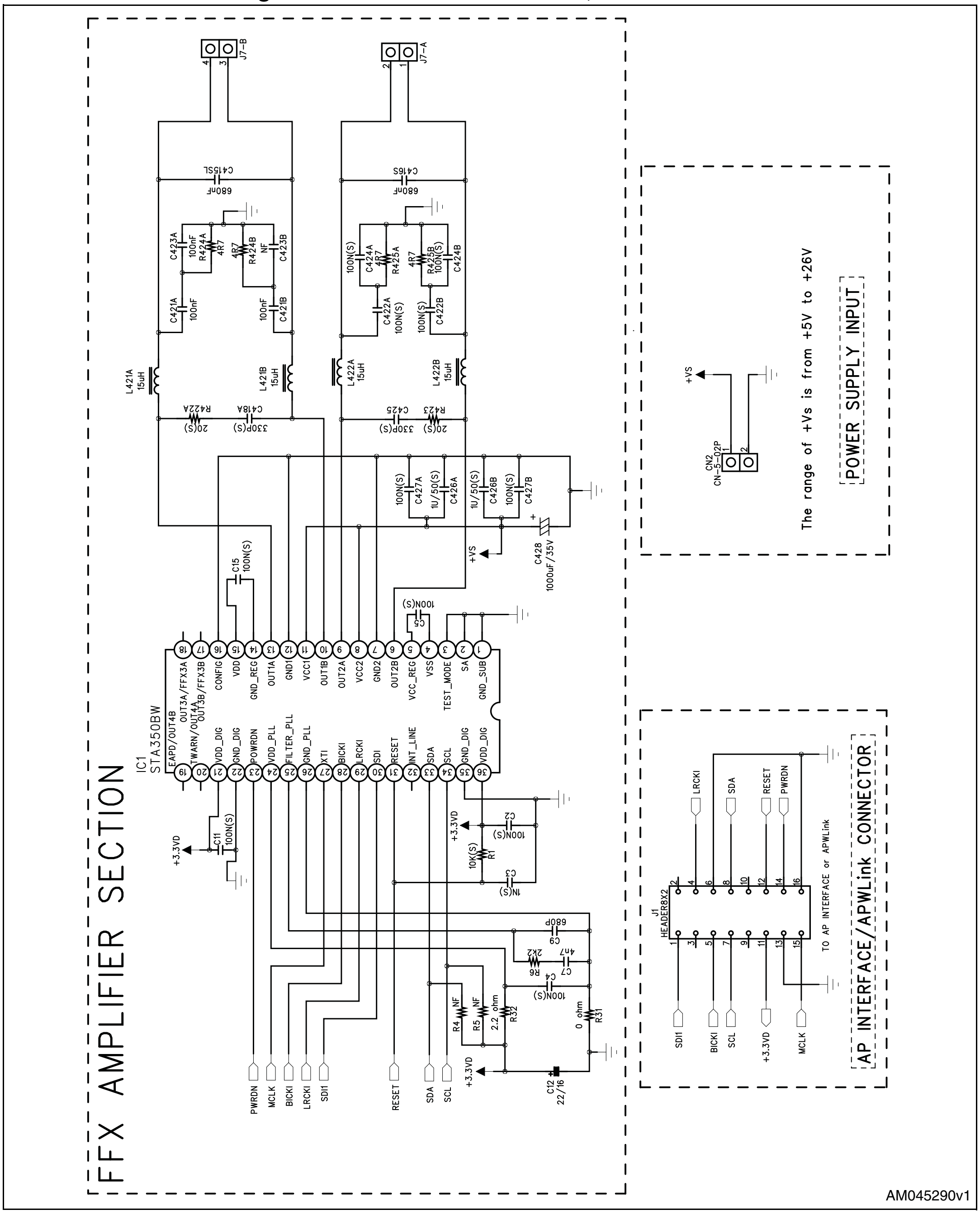


4 Characterization curves

The following characterization curves were made using the STA369BW demonstration board with 2.0 channels (refer to the schematic in *Figure 6*) under the following test conditions:

V_{CC} = 22 V, f = 1 kHz, f_{SW} = 384 kHz, Tamb = 25 °C and RL = 8 Ω, unless otherwise specified.

Figure 4. Demonstration board, 2.0 channels



AM045290v1

Figure 5. Mono parallel BTL schematic

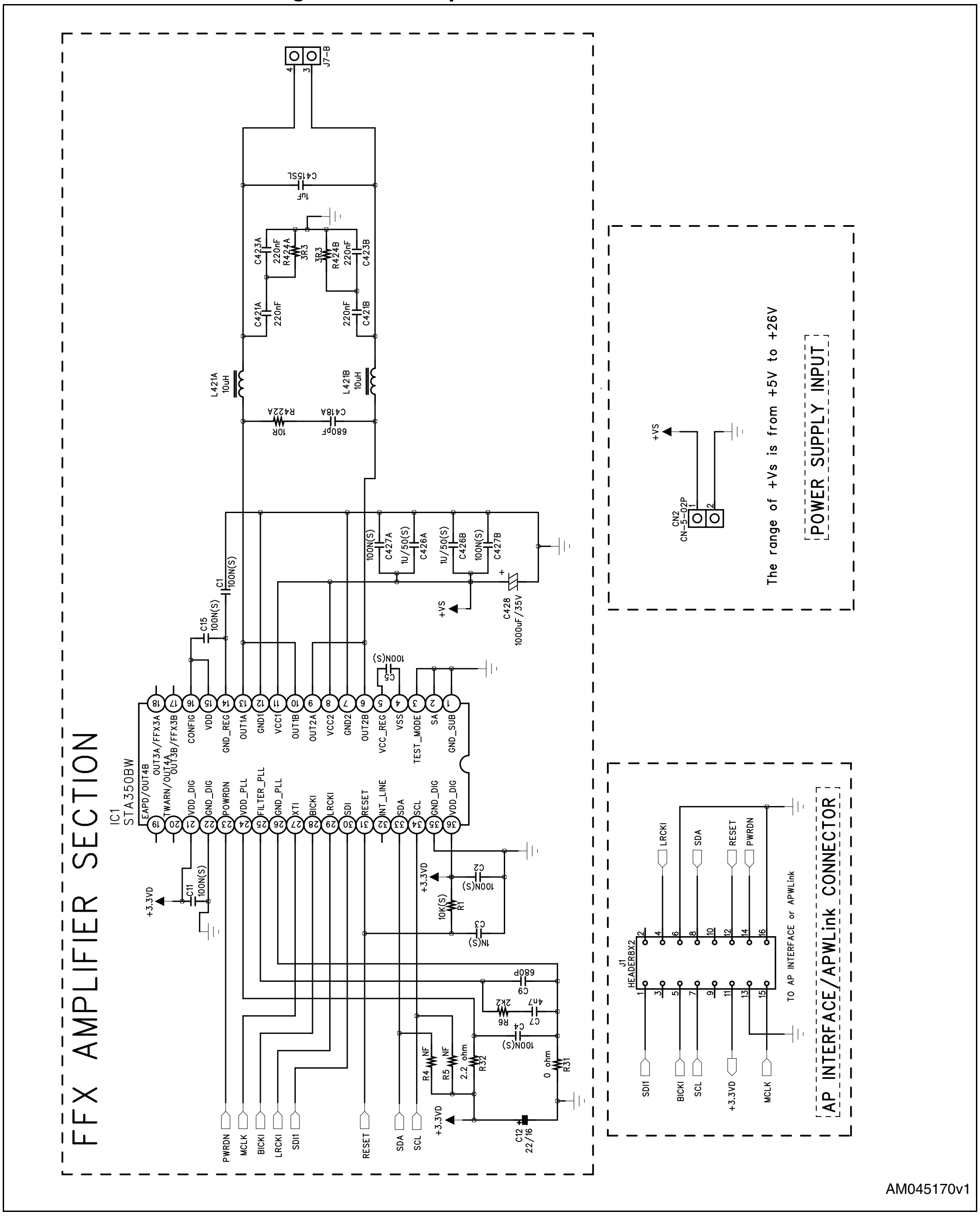


Figure 6. THD+N vs. output power (V_{CC} = 25 V, load = 6 Ω)

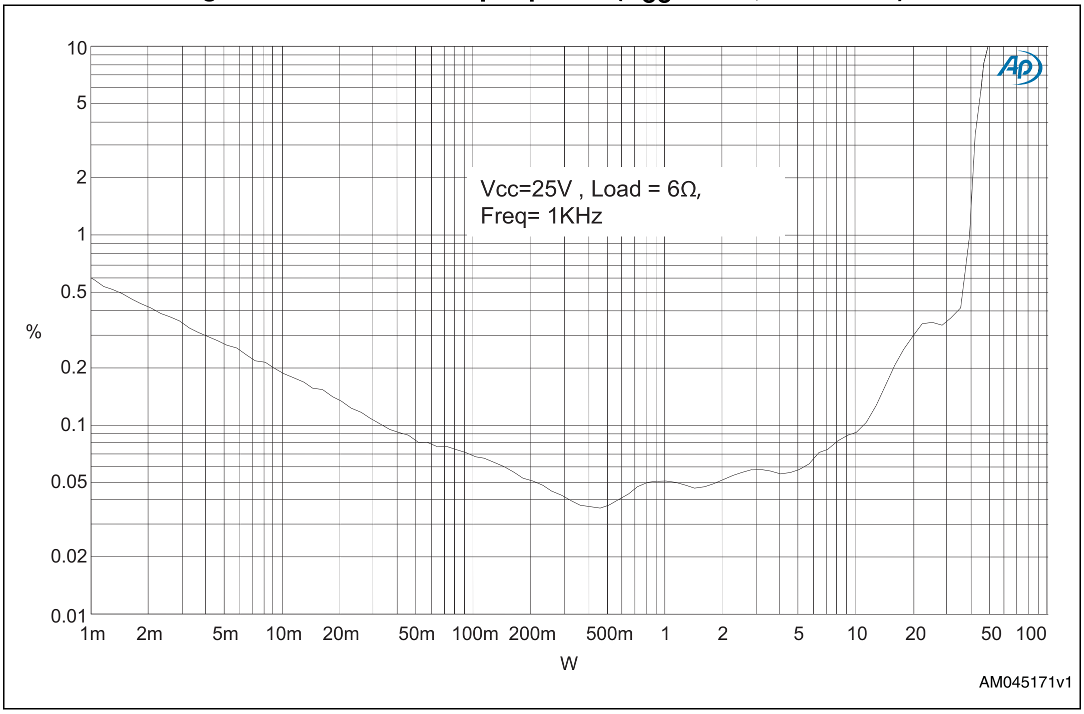


Figure 7. THD+N vs. output power (V_{CC} = 18 V, load = 8 Ω)

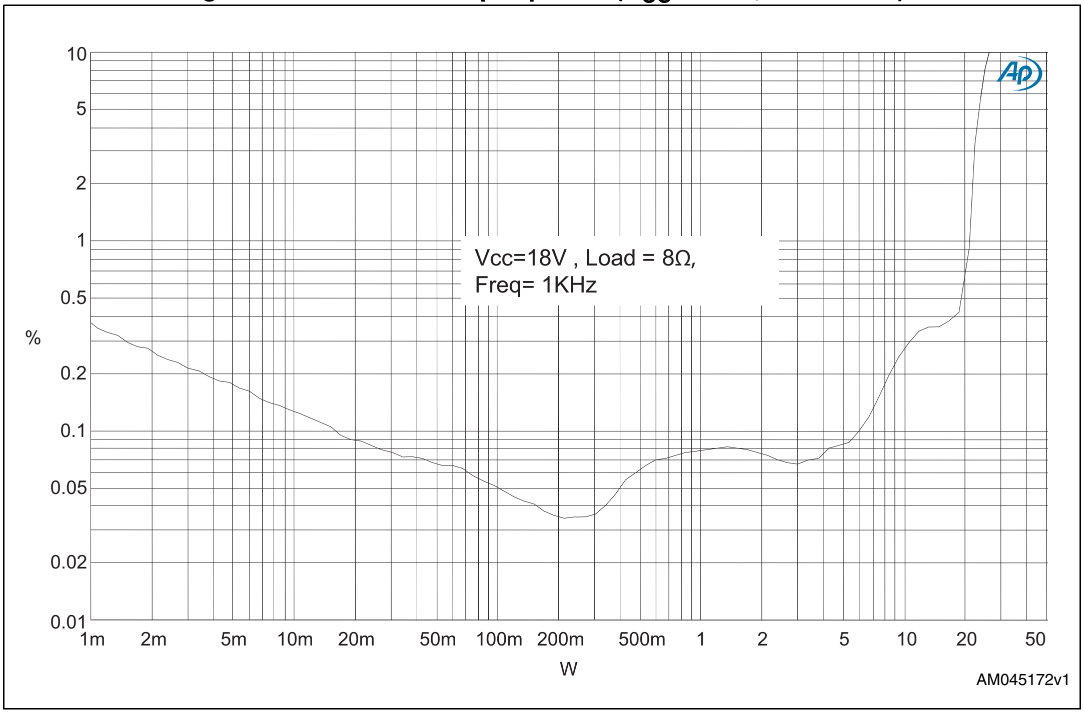


Figure 8. Output power vs. V_{CC} (load = 6 Ω)

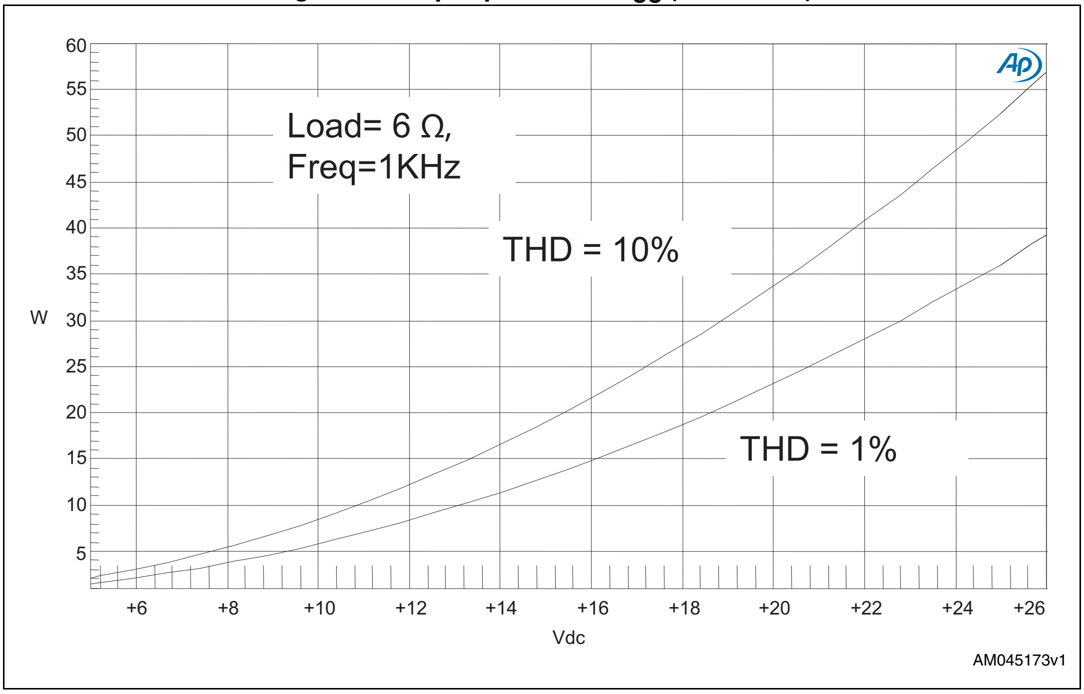


Figure 9. Output power vs. V_{CC} (load = 8 Ω)

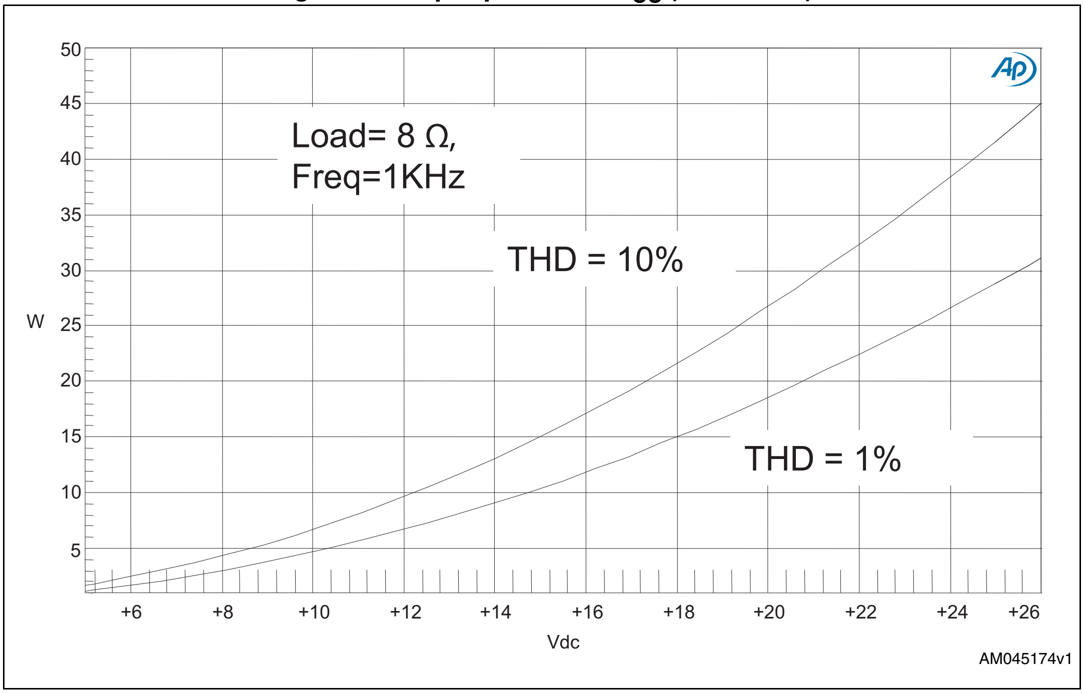


Figure 10. Efficiency vs. output power (V_{CC} = 25 V, load = 6 Ω)

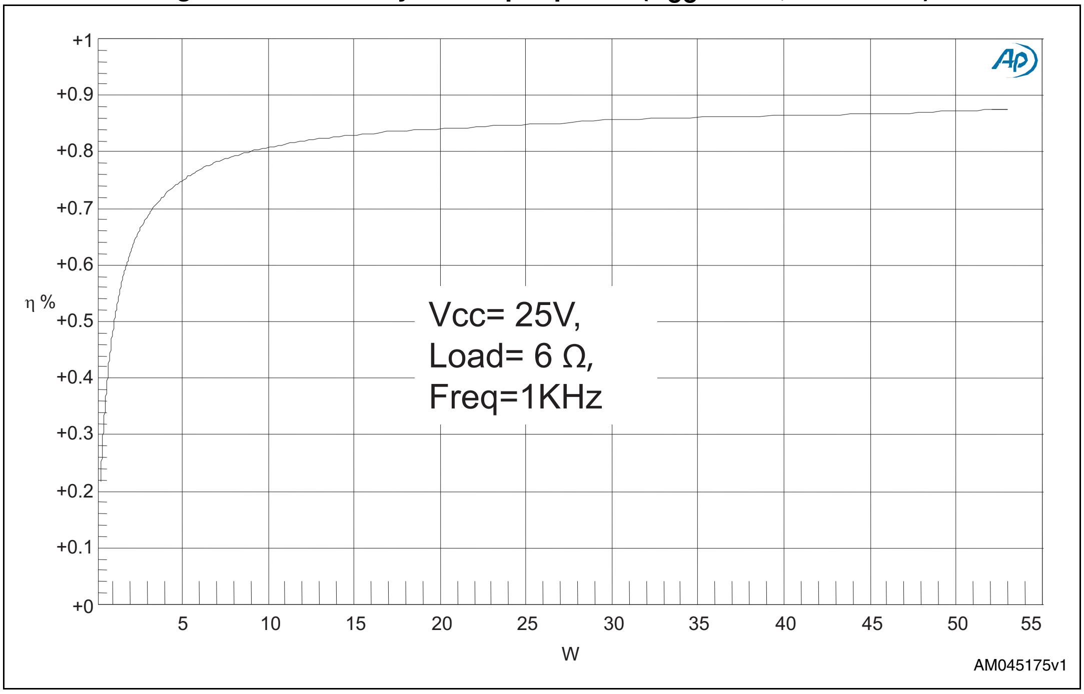
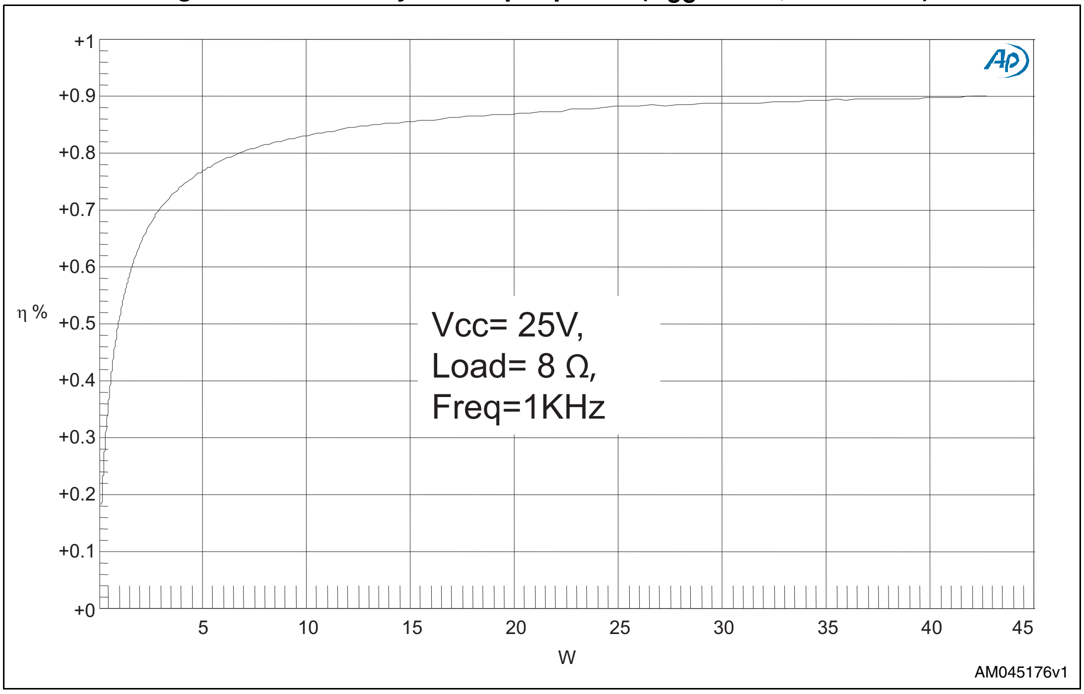


Figure 11. Efficiency vs. output power (V_{CC} = 25 V, load = 8 Ω)



4.1 Mono parallel BTL characteristics

Figure 12. THD+N vs. output power (V_{CC} = 25 V, load = 3 Ω)

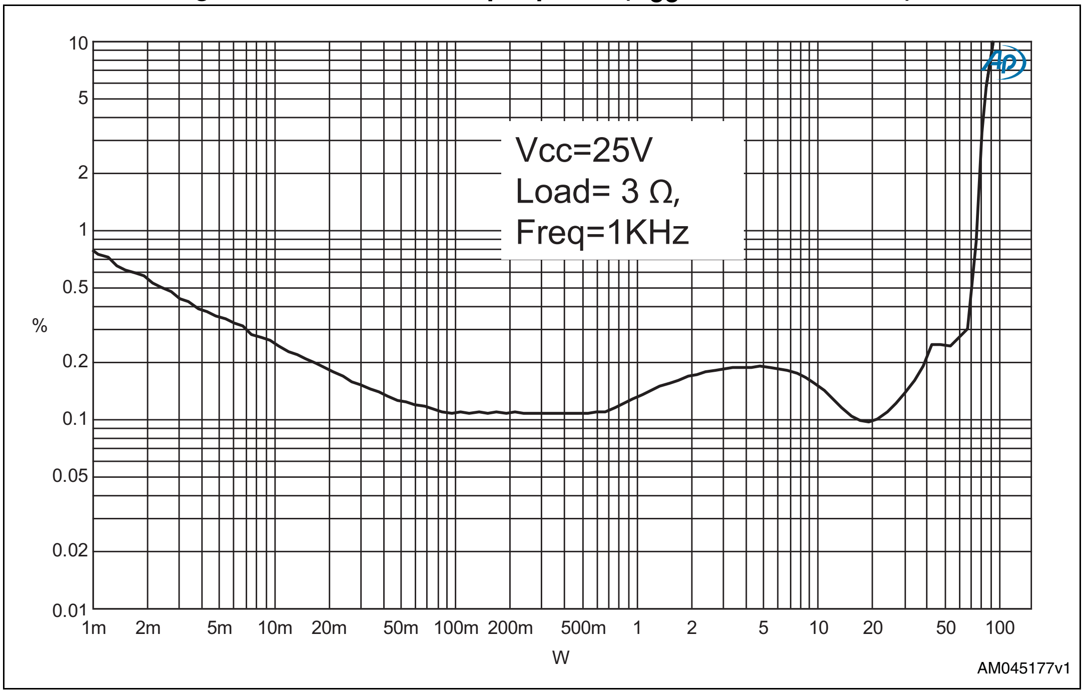


Figure 13. Output power vs. V_{CC} (load = 3 Ω)

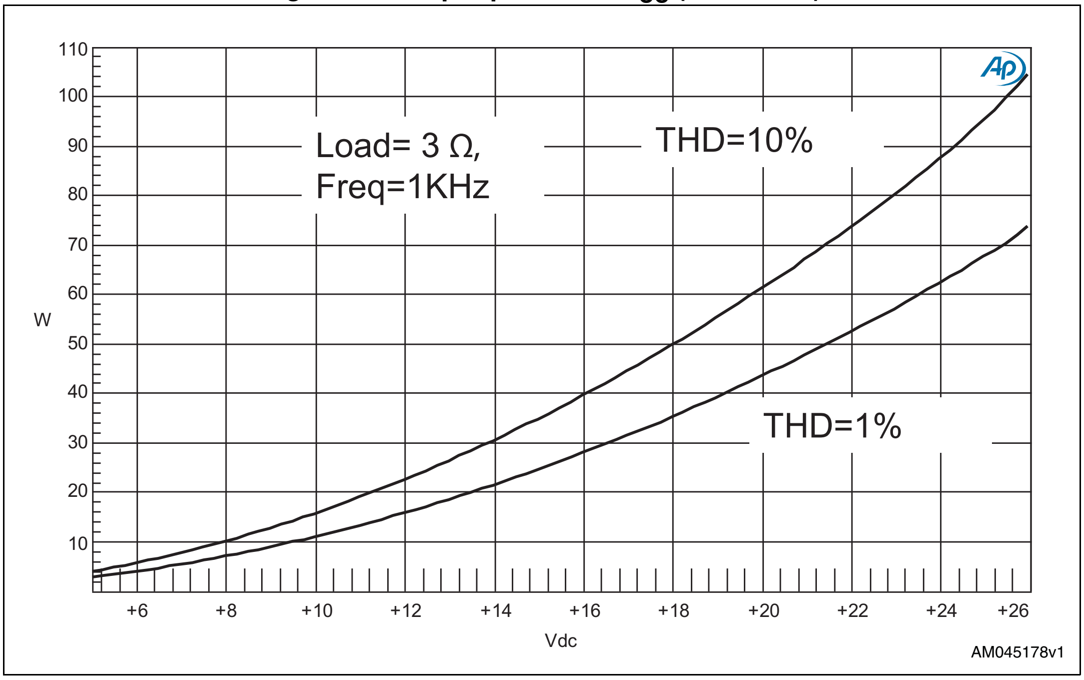


Figure 14. Efficiency vs. output power (V_{CC} = 26 V, load = 3 Ω)

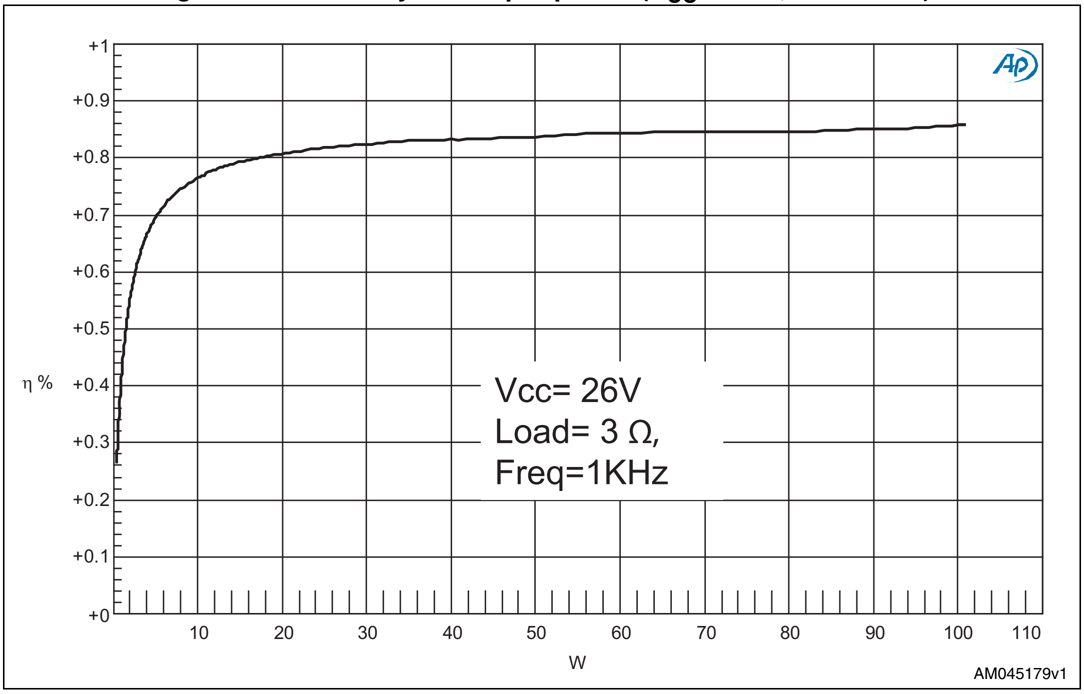
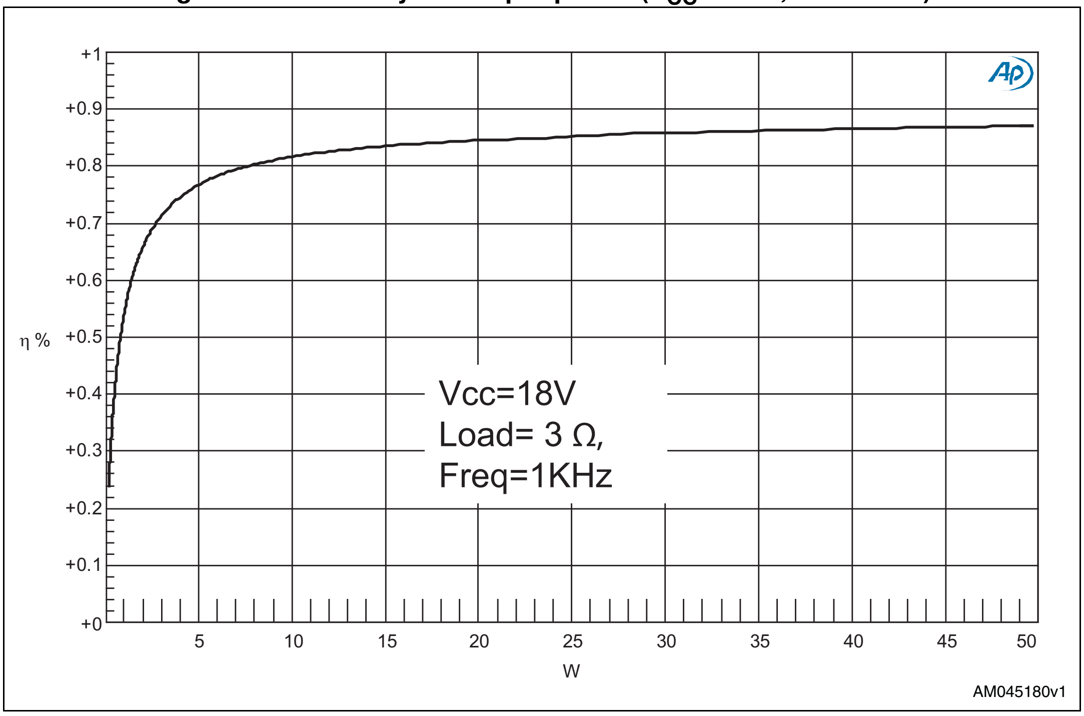


Figure 15. Efficiency vs. output power (V_{CC} = 18 V, load = 3 Ω)



5 Serial audio interface

The STA369BW audio serial input interface was designed to interface with standard digital audio components and to accept a number of serial data formats. The STA369BW always acts as the slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using three inputs: left/right clock LRCKI, serial clock BICKI, and serial data SDI12.

The SAI bit and the SAIFB bit are used to specify the serial data format. The default serial data format is I^2S, MSB-first.

5.0.1 Timings

In the STA369BW the BICKI and LRCKI pins are configured as inputs and they must be supplied by the external peripheral.

Figure 16. Timing diagram for SAI interface

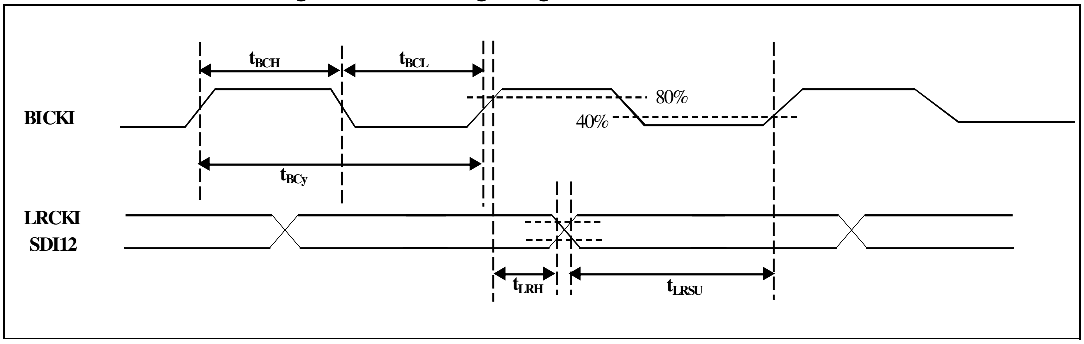


Table 8. Timing parameters for slave mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{BCy}	BICK cycle time	80	-	-	ns
t_{BCH}	BICK pulse width high	40	-	-	ns
t_{BCL}	BICK pulse width low	40	-	-	ns
t_{LRSU}	LRCKI setup time to BICKI strobing edge	40	-	-	ns
t_{LRH}	LRCKI hold time to BICKI strobing edge	40	-	-	ns
t_{LRJT}	LRCKI Jitter Tolerance			40	ns

5.0.2 Delay serial clock enable

To tolerate anomalies in some I^2S master devices, a PLL clock cycle delay can be added to the BICKI signal before the SAI interface.

5.0.3 Channel input mapping

Each channel received via I^2S can be mapped to any internal processing channel via the channel input mapping registers. This allows for flexibility in processing. The default settings of these registers map each I^2S input channel to its corresponding processing channel.