



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## Sound Terminal<sup>®</sup> 2.1-channel high-efficiency digital audio system

Datasheet - production data



### Features

- Wide-range supply voltage
  - 4.5 V to 26 V (operating range)
  - 30 V (absolute maximum rating)
- I<sup>2</sup>C control with selectable device address
- Embedded full IC protection
  - Manufacturing short-circuit protection (out vs. gnd, out vs. vcc, out vs. out)
  - Thermal protection
  - Overcurrent protection
  - Undervoltage protection
- 1 V<sub>rms</sub> stereo analog input
- I<sup>2</sup>S interface, sampling rate 32 kHz ~ 192 kHz, with internal sampling frequency converter for fixed processing frequency
- Three output power stage configurations
  - 2.0 mode, L/R full bridges
  - 2.1 mode, L/R two half-bridges, subwoofer full bridge
  - 2.1 mode, L/R full bridges, PWM output for external subwoofer amplifier
- Driving load capabilities
  - 2 x 20 W into 8 Ω ternary modulation
  - 2 x 9 W into 4 Ω + 1 x 20 W into 8 Ω
- FFX<sup>™</sup> 100 dB dynamic range
- Fixed output PWM frequency at any input sampling frequency
- Embedded RMS meter for measuring real-time loudness
- Two analog outputs
  - Selectable headphone / line out driver with adjustable gain via external resistors
  - New F3X<sup>™</sup> analog output
- New fully programmable noise-gating function
- Headphone
  - Embedded negative charge pump
  - Full capless output configuration
  - Driving load capabilities: 40 mW into 32 Ω
- Line out
  - 2 V<sub>rms</sub> line output capability
- Up to 12 user-programmable biquads with noise-shaping technology
- Direct access to coefficients through I<sup>2</sup>C shadowing mechanism
- Fixed (88.2 kHz / 96 kHz) internal processing sampling rate
- Two independent DRCs configurable as a dual-band anticlipper or independent limiters/compressors (B<sup>2</sup>DRC)
- Digital gain/att +48 dB to -80 dB with 0.125 dB/step resolution
- Independent (fade-in, fade-out) soft volume update with programmable rate 48 ~ 1.5 dB/ms
- Bass/treble tones control
- Audio presets: 15 crossover filters, 5 anticlipping modes, nighttime listening mode
- STSpeakerSafe<sup>™</sup> protection circuitry
  - Pre- and post-processing DC blocking filters
  - Checksum engine for filter coefficients
  - PWM fault self-diagnosis
- STCompressor<sup>™</sup> dual-band DRC

**Table 1. Device summary**

Order code	Package	Packing
STA381BW	VQFN48	Tray
STA381BWTR	VQFN48	Tape and Reel

# Contents

- 1 Description . . . . . 17**
  - 1.1 Block diagram . . . . . 18
- 2 Pin connections . . . . . 19**
  - 2.1 Connection diagram . . . . . 19
  - 2.2 Pin description . . . . . 20
- 3 Electrical specifications . . . . . 22**
  - 3.1 Absolute maximum ratings . . . . . 22
  - 3.2 Thermal data . . . . . 22
  - 3.3 Recommended operating conditions . . . . . 23
  - 3.4 Electrical specifications for the digital section . . . . . 23
  - 3.5 Electrical specifications for the power section . . . . . 24
  - 3.6 Power-on/off sequence . . . . . 26
  - 3.7 Electrical specifications for the analog section . . . . . 27
- 4 Device overview . . . . . 28**
  - 4.1 Processing data path . . . . . 28
  - 4.2 Input oversampling . . . . . 31
  - 4.3 STCompressorTM . . . . . 31
    - 4.3.1 STC block diagram . . . . . 32
    - 4.3.2 Band splitter . . . . . 32
    - 4.3.3 Level meter . . . . . 33
    - 4.3.4 Mapper . . . . . 33
    - 4.3.5 Attenuator . . . . . 36
    - 4.3.6 Dynamic attack . . . . . 36
    - 4.3.7 Offset . . . . . 37
    - 4.3.8 Stereo link . . . . . 37
    - 4.3.9 Programming of coefficients . . . . . 38
    - 4.3.10 Memory map . . . . . 40
- 5 I<sup>2</sup>C bus specification . . . . . 42**
  - 5.1 Communication protocol . . . . . 42



5.1.1	Data transition or change	42
5.1.2	Start condition	42
5.1.3	Stop condition	42
5.1.4	Data input	42
5.2	Device addressing	42
5.3	Write operation	43
5.3.1	Byte write	43
5.3.2	Multi-byte write	43
5.4	Read operation	43
5.4.1	Current address byte read	43
5.4.2	Current address multi-byte read	43
5.4.3	Random address byte read	43
5.4.4	Random address multi-byte read	43
5.4.5	Write mode sequence	44
5.4.6	Read mode sequence	44
<b>6</b>	<b>Register description: New Map</b>	<b>45</b>
6.1	CLK register (addr 0x00)	48
6.2	STATUS register (addr 0x01)	48
6.3	RESET register (addr 0x02)	49
6.4	Soft volume register (addr 0x03)	49
6.5	MVOL register (addr 0x04)	50
6.6	FINEVOL register (addr 0x05)	50
6.7	CH1VOL register (addr 0x06)	51
6.8	CH2VOL register (addr 0x07)	51
6.9	POST scaler register (addr 0x08)	52
6.10	OPER register (addr 0x09)	52
6.11	FUNCT register (addr 0x0A)	58
6.11.1	Dual-band DRC	58
6.12	HPCFG register (addr 0x10)	60
6.13	Configuration register A (addr 0x11)	60
6.13.1	Master clock select	60
6.13.2	Interpolation ratio selection	61
6.13.3	Fault-detect recovery bypass	61
6.14	Configuration register B (addr 0x12)	62

6.14.1	Serial data interface	62
6.14.2	Serial data first bit	63
6.14.3	Delay serial clock enable	65
6.14.4	Channel input mapping	65
6.15	Configuration register C (addr 0x13)	65
6.15.1	FFX compensating pulse size register	65
6.16	Configuration register D (addr 0x14)	66
6.16.1	DSP bypass	66
6.16.2	Post-scale link	66
6.16.3	Biquad coefficient link	66
6.16.4	Zero-detect mute enable	67
6.16.5	Submix mode enable	67
6.17	Configuration register E (addr 0x15)	67
6.17.1	Noise-shaper bandwidth selection	67
6.17.2	AM mode enable	67
6.17.3	PWM speed mode	68
6.17.4	Zero-crossing enable	68
6.18	Configuration register F (addr 0x16)	68
6.18.1	Invalid input detect mute enable	68
6.18.2	Binary output mode clock loss detection	68
6.18.3	LRCK double trigger protection	69
6.18.4	Power-down	69
6.18.5	External amplifier power-down	69
6.19	Volume control registers (addr 0x17 - 0x1B)	69
6.19.1	Mute/line output configuration register (addr 0x17)	69
6.19.2	Channel 3 / line output volume (addr 0x1B)	71
6.20	Audio preset registers (0x1D)	72
6.20.1	AM interference frequency switching	72
6.20.2	Bass management crossover	72
6.21	Channel configuration registers (addr 0x1F - 0x21)	73
6.21.1	Tone control bypass	73
6.21.2	EQ bypass	74
6.21.3	Volume bypass	74
6.21.4	Binary output enable registers	74
6.21.5	Limiter select	74
6.21.6	Output mapping	75

6.22	Tone control register (addr 0x22) . . . . .	75
6.22.1	Tone control . . . . .	75
6.23	Dynamic control registers (addr 0x23 - 0x26 / addr 0x43 - 0x46) . . . . .	76
6.23.1	Limiter 1 attack/release rate (L1AR addr 0x23) . . . . .	76
6.23.2	Limiter 1 attack/release threshold (L1ATRT addr 0x24) . . . . .	76
6.23.3	Limiter 2 attack/release rate ( L2AR addr 0x25) . . . . .	76
6.23.4	Limiter 2 attack/release threshold ( L2 ATRT addr 0x26) . . . . .	76
6.23.5	Limiter 1 extended attack threshold (addr 0x43) . . . . .	80
6.23.6	Limiter 1 extended release threshold (addr 0x44) . . . . .	80
6.23.7	Limiter 2 extended attack threshold (addr 0x45) . . . . .	81
6.23.8	Limiter 2 extended release threshold (addr 0x46) . . . . .	81
6.24	User-defined coefficient control registers (addr 0x27 - 0x37) . . . . .	81
6.24.1	Coefficient address register . . . . .	81
6.24.2	Coefficient b1 data register bits 23:16 . . . . .	81
6.24.3	Coefficient b1 data register bits 15:8 . . . . .	81
6.24.4	Coefficient b1 data register bits 7:0 . . . . .	81
6.24.5	Coefficient b2 data register bits 23:16 . . . . .	82
6.24.6	Coefficient b2 data register bits 15:8 . . . . .	82
6.24.7	Coefficient b2 data register bits 7:0 . . . . .	82
6.24.8	Coefficient a1 data register bits 23:16 . . . . .	82
6.24.9	Coefficient a1 data register bits 15:8 . . . . .	82
6.24.10	Coefficient a1 data register bits 7:0 . . . . .	82
6.24.11	Coefficient a2 data register bits 23:16 . . . . .	82
6.24.12	Coefficient a2 data register bits 15:8 . . . . .	83
6.24.13	Coefficient a2 data register bits 7:0 . . . . .	83
6.24.14	Coefficient b0 data register bits 23:16 . . . . .	83
6.24.15	Coefficient b0 data register bits 15:8 . . . . .	83
6.24.16	Coefficient b0 data register bits 7:0 . . . . .	83
6.24.17	Coefficient write/read control register . . . . .	83
6.24.18	User-defined EQ . . . . .	86
6.24.19	Pre-scale . . . . .	86
6.24.20	Post-scale . . . . .	86
6.25	Fault-detect recovery constant registers (addr 0x3C - 0x3D) . . . . .	88
6.26	Extended configuration register (addr 0x47) . . . . .	88
6.26.1	Extended post-scale range . . . . .	88
6.26.2	Extended attack rate . . . . .	88

6.26.3	Extended biquad selector	89
6.27	PLL configuration registers (address 0x52; 0x53; 0x54; 0x55; 0x56; 0x57)	90
6.28	Short-circuit protection mode registers SHOK (address 0x58)	92
6.29	Extended coefficient range up to -4...4 (address 0x5A)	93
6.30	Miscellaneous registers (address 0x5C, 0x5D)	94
6.30.1	Rate power-down enable (RPDNEN) bit	94
6.30.2	Bridge immediately off (BRIDGOFF) bit (address 0x4B, bit D5)	94
6.30.3	Channel PWM enable (CPWMEN) bit	95
6.30.4	External amplifier hardware pin enabler (LPDP, LPD LPDE) bits	95
6.30.5	Power-down delay selector (PNDLSL[2:0]) bits	95
6.30.6	Short-circuit check enable bit	96
6.31	Bad PWM detection registers (address 0x5E, 0x5F, 0x60)	96
6.32	Enhanced zero-detect mute and input level measurement (address 0x61-0x65, 0x3F, 0x40, 0x6F)	97
6.33	Headphone/Line out configuration register (address 0x66)	99
6.34	F3XCFG (address 0x69; 0x6A)	100
6.35	STCompressorTM configuration register (address 0x6B; 0x6C)	101
6.36	Charge pump synchronization (address 0x70)	101
6.37	Coefficient RAM CRC protection (address 0x71-0x7D)	102
6.38	MISC4 (address 0x7E)	104
<b>7</b>	<b>Register description: Sound Terminal compatibility</b>	<b>106</b>
7.1	Configuration register A (addr 0x00)	109
7.1.1	Master clock select	109
7.1.2	Interpolation ratio select	110
7.1.3	Fault-detect recovery bypass	110
7.2	Configuration register B (addr 0x01)	111
7.2.1	Serial data interface	111
7.2.2	Serial audio input interface format	111
7.2.3	Serial data first bit	111
7.2.4	Delay serial clock enable	114
7.2.5	Channel input mapping	114
7.3	Configuration register C (addr 0x02)	115
7.3.1	FFX compensating pulse size register	115
7.4	Configuration register D (addr 0x03)	115

7.4.1	DSP bypass	115
7.4.2	Post-scale link	116
7.4.3	Biquad coefficient link	116
7.4.4	Zero-detect mute enable	116
7.4.5	Submix mode enable	116
7.5	Configuration register E (addr 0x04)	116
7.5.1	Noise-shaper bandwidth selection	117
7.5.2	AM mode enable	117
7.5.3	PWM speed mode	117
7.5.4	Zero-crossing enable	117
7.5.5	Soft volume update enable	117
7.6	Configuration register F (addr 0x05)	118
7.6.1	Output configuration	118
7.6.2	Invalid input detect mute enable	124
7.6.3	Binary output mode clock loss detection	124
7.6.4	LRCK double trigger protection	124
7.6.5	IC power-down	124
7.6.6	External amplifier power-down	124
7.7	Volume control registers (addr 0x06 - 0x0A)	125
7.7.1	Mute/line output configuration register	125
7.7.2	Master volume register	126
7.7.3	Channel 1 volume	126
7.7.4	Channel 2 volume	126
7.7.5	Channel 3 / line output volume	126
7.8	Audio preset registers (addr 0x0C)	127
7.8.1	Audio preset register (addr 0x0C)	127
7.8.2	AM interference frequency switching	128
7.8.3	Bass management crossover	128
7.9	Channel configuration registers (addr 0x0E - 0x10)	129
7.9.1	Tone control bypass	129
7.9.2	EQ bypass	130
7.9.3	Volume bypass	130
7.9.4	Binary output enable registers	130
7.9.5	Limiter select	130
7.9.6	Output mapping	131
7.10	Tone control register (addr 0x11)	131



- 7.10.1 Tone control ..... 131
- 7.11 Dynamic control registers (addr 0x12 - 0x15) ..... 132
  - 7.11.1 Limiter 1 attack/release rate ..... 132
  - 7.11.2 Limiter 1 attack/release threshold ..... 132
  - 7.11.3 Limiter 2 attack/release rate ..... 132
  - 7.11.4 Limiter 2 attack/release threshold ..... 132
  - 7.11.5 Limiter 1 extended attack threshold (addr 0x32) ..... 136
  - 7.11.6 Limiter 1 extended release threshold (addr 0x33) ..... 136
  - 7.11.7 Limiter 2 extended attack threshold (addr 0x34 ..... ) 137
  - 7.11.8 Limiter 2 extended release threshold (addr 0x35) ..... 137
- 7.12 User-defined coefficient control registers (addr 0x16 - 0x26) ..... 137
  - 7.12.1 Coefficient address register ..... 137
  - 7.12.2 Coefficient b1 data register bits 23:16 ..... 137
  - 7.12.3 Coefficient b1 data register bits 15:8 ..... 137
  - 7.12.4 Coefficient b1 data register bits 7:0 ..... 137
  - 7.12.5 Coefficient b2 data register bits 23:16 ..... 138
  - 7.12.6 Coefficient b2 data register bits 15:8 ..... 138
  - 7.12.7 Coefficient b2 data register bits 7:0 ..... 138
  - 7.12.8 Coefficient a1 data register bits 23:16 ..... 138
  - 7.12.9 Coefficient a1 data register bits 15:8 ..... 138
  - 7.12.10 Coefficient a1 data register bits 7:0 ..... 138
  - 7.12.11 Coefficient a2 data register bits 23:16 ..... 138
  - 7.12.12 Coefficient a2 data register bits 15:8 ..... 139
  - 7.12.13 Coefficient a2 data register bits 7:0 ..... 139
  - 7.12.14 Coefficient b0 data register bits 23:16 ..... 139
  - 7.12.15 Coefficient b0 data register bits 15:8 ..... 139
  - 7.12.16 Coefficient b0 data register bits 7:0 ..... 139
  - 7.12.17 Coefficient write/read control register ..... 139
  - 7.12.18 User-defined EQ ..... 142
  - 7.12.19 Pre-scale ..... 142
  - 7.12.20 Post-scale ..... 142
- 7.13 Fault-detect recovery constant registers (addr 0x2B - 0x2C) ..... 144
- 7.14 Device status register (addr 0x2D) ..... 144
- 7.15 EQ coefficients configuration register (addr 0x31) ..... 144
- 7.16 Extended configuration register (addr 0x36) ..... 145
  - 7.16.1 Dual-band DRC ..... 145

7.16.2	Extended post-scale range	146
7.16.3	Extended attack rate	147
7.16.4	Extended BIQUAD selector	147
7.17	EQ soft volume configuration registers (addr 0x37 - 0x38)	148
7.18	Extra volume resolution configuration registers (address 0x3F; 0x40)	149
7.19	PLL configuration registers (address 0x41; 0x42; 0x43; 0x44; 0x45; 0x46)	150
7.20	Short-circuit protection mode registers SHOK (address 0x47)	152
7.21	Extended coefficient range up to -4...4 (address 0x49, 0x4A)	154
7.22	Miscellaneous registers (address 0x4B, 0x4C)	154
7.22.1	Rate power-down enable (RPDNEN) bit (address 0x4B, bit D7)	154
7.22.2	Bridge immediately off (BRIDGOFF) bit (address 0x4B, bit D5)	155
7.22.3	Channel PWM enable (CPWMEN) bit (address 0x4B, bit D2)	155
7.22.4	External amplifier hardware pin enabler (LPDP, LPD LPDE) bits (address 0x4C, bit D7, D6, D5)	155
7.22.5	Power-down delay selector (PNDLSL[2:0]) bits (address 0x4C, bit D4, D3, D2)	156
7.22.6	Short-circuit check enable bit (address 0x4C, bit D0)	156
7.23	Bad PWM detection registers (address 0x4D, 0x4E, 0x4F)	157
7.24	Enhanced zero-detect mute and input level measurement (address 0x50-0x54, 0x2E, 0x2F and 0x5E)	158
7.25	Headphone/Line out configuration register (address 0x55)	160
7.26	F3XCFG (address 0x58; 0x59)	161
7.27	STCompressor™ configuration register (address 0x5A; 0x5B)	162
7.28	Charge pump synchronization (address 0x5F)	163
7.29	Coefficient RAM CRC protection (address 0x60-0x6C)	164
7.30	MISC3 (address 0x6E)	166
7.31	MISC4 (address 0x7E)	166
<b>8</b>	<b>Applications</b>	<b>167</b>
8.1	Application schemes	167
8.2	Headphone and 2 Vrms line out	169
8.3	Typical output configuration	170
<b>9</b>	<b>Package information</b>	<b>171</b>

---

**10**      **Revision history** ..... **173**

# List of tables

Table 1.	Device summary . . . . .	1
Table 2.	Pin list . . . . .	20
Table 3.	Absolute maximum ratings . . . . .	22
Table 4.	Thermal data . . . . .	22
Table 5.	Recommended operating conditions . . . . .	23
Table 6.	Electrical specifications - digital section . . . . .	23
Table 7.	Electrical specifications - power section . . . . .	24
Table 8.	Electrical specifications for the analog section . . . . .	27
Table 9.	Coefficients extended-range configuration 0x74h. . . . .	33
Table 10.	Compressor ratio . . . . .	35
Table 11.	Conversion example . . . . .	39
Table 12.	STC coefficients memory map . . . . .	40
Table 13.	STC band splitter filters memory map . . . . .	41
Table 14.	Default register map table: NEW MAP . . . . .	45
Table 15.	CLK register . . . . .	48
Table 16.	STATUS register . . . . .	48
Table 17.	RESET register . . . . .	49
Table 18.	Soft volume register . . . . .	49
Table 19.	Master volume register . . . . .	50
Table 20.	Fine volume register . . . . .	50
Table 21.	Channel 1 volume register . . . . .	51
Table 22.	Channel 2 volume register . . . . .	51
Table 23.	OPER register . . . . .	52
Table 24.	OPER configuration selection . . . . .	52
Table 25.	FUNCT register . . . . .	58
Table 26.	HPCFG register . . . . .	60
Table 27.	Master clock select . . . . .	60
Table 28.	Input sampling rates . . . . .	61
Table 29.	Internal interpolation ratio . . . . .	61
Table 30.	IR bit settings as a function of the input sampling rate . . . . .	61
Table 31.	Fault-detect recovery bypass . . . . .	61
Table 32.	Serial data first bit . . . . .	63
Table 33.	Support serial audio input formats for MSB-first (SAIFB = 0) . . . . .	63
Table 34.	Supported serial audio input formats for LSB-first (SAIFB = 1) . . . . .	64
Table 35.	Delay serial clock enable . . . . .	65
Table 36.	Channel input mapping . . . . .	65
Table 37.	FFX compensating pulse size bits . . . . .	65
Table 38.	Compensating pulse size . . . . .	66
Table 39.	DSP bypass . . . . .	66
Table 40.	Post-scale link . . . . .	66
Table 41.	Biquad coefficient link . . . . .	66
Table 42.	Zero-detect mute enable . . . . .	67
Table 43.	Submix mode enable . . . . .	67
Table 44.	Noise-shaper bandwidth selection . . . . .	67
Table 45.	AM mode enable . . . . .	67
Table 46.	PWM speed mode . . . . .	68
Table 47.	Zero-crossing enable . . . . .	68
Table 48.	Invalid input detect mute enable . . . . .	68

Table 49.	Binary output mode clock loss detection . . . . .	68
Table 50.	LRCK double trigger protection . . . . .	69
Table 51.	IC power-down . . . . .	69
Table 52.	External amplifier power-down . . . . .	69
Table 53.	Line output configuration . . . . .	70
Table 54.	Mute configuration . . . . .	70
Table 55.	Channel 3 volume as a function of CH3VOL[7:0] . . . . .	71
Table 56.	AM interference frequency switching bits . . . . .	72
Table 57.	Audio preset AM switching frequency selection . . . . .	72
Table 58.	Bass management crossover . . . . .	72
Table 59.	Bass management crossover frequency . . . . .	73
Table 60.	Tone control bypass . . . . .	73
Table 61.	EQ bypass . . . . .	74
Table 62.	Volume bypass register . . . . .	74
Table 63.	Binary output enable registers . . . . .	74
Table 64.	Channel limiter mapping as a function of C3LS bits . . . . .	74
Table 65.	Channel output mapping as a function of C3OM bits . . . . .	75
Table 66.	Tone control boost/cut as a function of BTC and TTC bits . . . . .	75
Table 67.	Limiter attack rate as a function of LxA bits . . . . .	78
Table 68.	Limiter release rate as a function of LxR bits . . . . .	78
Table 69.	Limiter attack threshold as a function of LxAT bits (AC mode) . . . . .	79
Table 70.	Limiter release threshold as a function of LxRT bits (AC mode) . . . . .	79
Table 71.	Limiter attack threshold as a function of LxAT bits (DRC mode) . . . . .	80
Table 72.	Limiter release threshold as a function of LxRT bits (DRC mode) . . . . .	80
Table 73.	RAM block for biquads, mixing, scaling and bass management . . . . .	87
Table 74.	Extended post-scale range . . . . .	88
Table 75.	Extended attack rate, limiter 1 . . . . .	88
Table 76.	Extended attack rate, limiter 2 . . . . .	89
Table 77.	Extended biquad selector, biquad 5 . . . . .	89
Table 78.	Extended biquad selector, biquad 6 . . . . .	89
Table 79.	Extended biquad selector, biquad 7 . . . . .	89
Table 80.	PLL factors . . . . .	90
Table 81.	PLL register 0x54 bits . . . . .	91
Table 82.	PLL register 0x55 bits . . . . .	91
Table 83.	PLL register 0x56 bits . . . . .	91
Table 84.	PLL register 0x57 bits . . . . .	92
Table 85.	Coefficients extended range configuration . . . . .	94
Table 86.	External amplifier enabler configuration bits . . . . .	95
Table 87.	PNDLSL bits configuration . . . . .	96
Table 88.	Zero-detect threshold . . . . .	97
Table 90.	Manual threshold register 0x3F, 0x40 and 0x6F . . . . .	98
Table 89.	Zero-detect hysteresis . . . . .	98
Table 91.	Headphone/Line out configuration bits . . . . .	99
Table 92.	F3X configuration register 1 . . . . .	100
Table 93.	F3X configuration register 2 . . . . .	100
Table 94.	Register STCCFG0 . . . . .	101
Table 95.	STCCFG0 register . . . . .	101
Table 96.	Register STCCFG1 . . . . .	101
Table 97.	STCCFG1 register . . . . .	101
Table 98.	Charge pump sync configuration bits . . . . .	101
Table 99.	Misc register 4 . . . . .	104
Table 100.	I <sup>2</sup> C registers summary . . . . .	106



Table 101.	Master clock select . . . . .	109
Table 102.	Input sampling rates . . . . .	109
Table 103.	Internal interpolation ratio . . . . .	110
Table 104.	IR bit settings as a function of the input sampling rate . . . . .	110
Table 105.	Fault-detect recovery bypass . . . . .	110
Table 106.	Serial audio input interface . . . . .	111
Table 107.	Serial data first bit . . . . .	111
Table 108.	Support serial audio input formats for MSB-first (SAIFB = 0) . . . . .	112
Table 109.	Supported serial audio input formats for LSB-first (SAIFB = 1) . . . . .	113
Table 110.	Delay serial clock enable . . . . .	114
Table 111.	Channel input mapping . . . . .	114
Table 112.	FFX compensating pulse size bits . . . . .	115
Table 113.	Compensating pulse size . . . . .	115
Table 114.	DSP bypass . . . . .	115
Table 115.	Post-scale link . . . . .	116
Table 116.	Biquad coefficient link . . . . .	116
Table 117.	Zero-detect mute enable . . . . .	116
Table 118.	Submix mode enable . . . . .	116
Table 119.	Noise-shaper bandwidth selection . . . . .	117
Table 120.	AM mode enable . . . . .	117
Table 121.	PWM speed mode . . . . .	117
Table 122.	Zero-crossing enable . . . . .	117
Table 123.	Soft volume update enable . . . . .	117
Table 124.	Output configuration . . . . .	118
Table 125.	Output configuration engine selection . . . . .	118
Table 126.	Invalid input detect mute enable . . . . .	124
Table 127.	Binary output mode clock loss detection . . . . .	124
Table 128.	LRCK double trigger protection . . . . .	124
Table 129.	IC power-down . . . . .	124
Table 130.	External amplifier power-down . . . . .	124
Table 131.	Line output configuration . . . . .	125
Table 132.	Mute configuration . . . . .	125
Table 133.	Master volume offset as a function of MVOL[7:0] . . . . .	127
Table 134.	Channel volume as a function of CxVOL[7:0] . . . . .	127
Table 135.	AM interference frequency switching bits . . . . .	128
Table 136.	Audio preset AM switching frequency selection . . . . .	128
Table 137.	Bass management crossover . . . . .	128
Table 138.	Bass management crossover frequency . . . . .	129
Table 139.	Tone control bypass . . . . .	129
Table 140.	EQ bypass . . . . .	130
Table 141.	Volume bypass register . . . . .	130
Table 142.	Binary output enable registers . . . . .	130
Table 143.	Channel limiter mapping as a function of CxLS bits . . . . .	130
Table 144.	Channel output mapping as a function of CxOM bits . . . . .	131
Table 145.	Tone control boost/cut as a function of BTC and TTC bits . . . . .	131
Table 146.	Limiter attack rate as a function of LxA bits . . . . .	134
Table 147.	Limiter release rate as a function of LxR bits . . . . .	134
Table 148.	Limiter attack threshold as a function of LxAT bits (AC mode) . . . . .	135
Table 149.	Limiter release threshold as a function of LxRT bits (AC mode) . . . . .	135
Table 150.	Limiter attack threshold as a function of LxAT bits (DRC mode) . . . . .	136
Table 151.	Limiter release threshold as a function of LxRT bits (DRC mode) . . . . .	136
Table 152.	RAM block for biquads, mixing, scaling and bass management . . . . .	143

Table 153.	Status register bits . . . . .	144
Table 154.	Extended post-scale range . . . . .	146
Table 155.	Extended attack rate, limiter 1 . . . . .	147
Table 156.	Extended attack rate, limiter 2 . . . . .	147
Table 157.	Extended biquad selector, biquad 5 . . . . .	147
Table 158.	Extended biquad selector, biquad 6 . . . . .	147
Table 159.	Extended biquad selector, biquad 7 . . . . .	147
Table 160.	Soft volume update enable, increase . . . . .	148
Table 161.	Soft volume update enable, decrease . . . . .	148
Table 162.	Volume fine-tuning steps . . . . .	149
Table 163.	Extra volume resolution enable. . . . .	150
Table 164.	PLL factors . . . . .	151
Table 165.	PLL register 0x43 bits . . . . .	151
Table 166.	PLL register 0x44 bits . . . . .	151
Table 167.	PLL register 0x45 bits . . . . .	152
Table 168.	PLL register 0x46 bits . . . . .	152
Table 169.	Coefficients extended range configuration . . . . .	154
Table 170.	External amplifier enabler configuration bits . . . . .	155
Table 171.	PNDLSL bits configuration . . . . .	156
Table 172.	Zero-detect threshold . . . . .	159
Table 173.	Zero-detect hysteresis . . . . .	159
Table 174.	Manual threshold register 0x2E, 0x2F and 0x5E . . . . .	160
Table 175.	Headphone/Line out configuration bits . . . . .	160
Table 176.	F3X configuration register 1 . . . . .	161
Table 177.	F3X configuration register 2 . . . . .	161
Table 178.	STCompressorTM configuration bits1 . . . . .	162
Table 179.	STCompressorTM configuration bits 2 . . . . .	162
Table 180.	Charge pump sync configuration bits . . . . .	163
Table 181.	Misc register 3. . . . .	166
Table 182.	MISC4. . . . .	166
Table 183.	VQFN48 (7 x 7 x 0.9 mm) package dimensions . . . . .	172
Table 184.	Document revision history. . . . .	173

## List of figures

Figure 1.	Block diagram	18
Figure 2.	Pin connections VQFN48 (top view)	19
Figure 3.	Test circuit.	25
Figure 4.	Power-on sequence	26
Figure 5.	Power-off sequence for pop-free turn-off	26
Figure 6.	Processing path, first part	28
Figure 7.	Processing path, second part: 2.1 output with individually configurable anticlipper/DRCs	29
Figure 8.	Processing path, second part: 2.0 output with B <sup>2</sup> DRC	30
Figure 9.	Processing path, second part: 2.1 output configuration with STCompressor™	30
Figure 10.	STCompressor™ block diagram	32
Figure 11.	Band splitter with 4th order filtering	33
Figure 12.	STCompressor™ behavior	34
Figure 13.	STCompressor™ behavior as a limiter	35
Figure 14.	Offset effect	37
Figure 15.	Stereo link block diagram	38
Figure 16.	Write mode sequence	44
Figure 17.	Read mode sequence	44
Figure 18.	OPER = 00 (default value)	53
Figure 19.	OPER = 11	53
Figure 20.	OPER = 10	53
Figure 21.	OPER = 01	54
Figure 22.	Output mapping scheme	54
Figure 23.	2.0 channels (OPER = 00) PWM slots	55
Figure 24.	2.1 channels (OPER = 11) PWM slots	56
Figure 25.	2.1 channels (OPER = 10) PWM slots	57
Figure 26.	B <sup>2</sup> DRC scheme	58
Figure 27.	Basic limiter and volume flow diagram	78
Figure 28.	Short-circuit detection timing diagram (no short detected)	93
Figure 29.	Alternate function for INTLINE pin	95
Figure 30.	Coefficients direct access single-write operation	105
Figure 31.	Coefficients direct access multiple-write operation	105
Figure 32.	Coefficients direct access single-read operation	105
Figure 33.	OCFG = 00 (default value)	119
Figure 34.	OCFG = 01	119
Figure 35.	OCFG = 10	119
Figure 36.	OCFG = 11	120
Figure 37.	Output mapping scheme	120
Figure 38.	2.0 channels (OCFG = 00) PWM slots	121
Figure 39.	2.1 channels (OCFG = 01) PWM slots	122
Figure 40.	2.1 channels (OCFG = 10) PWM slots	123
Figure 41.	Basic limiter and volume flow diagram	134
Figure 42.	B <sup>2</sup> DRC scheme	145
Figure 43.	Extra resolution volume scheme	149
Figure 44.	Short-circuit detection timing diagram (no short detected)	153
Figure 45.	Alternate function for INTLINE pin	156
Figure 46.	External audio source to line/headphone out application scheme	167
Figure 47.	F3X (from SAI) source to line/headphone out application scheme	168
Figure 48.	F3X auxiliary analog output	169

Figure 49. Headphone and line out block diagram .....	169
Figure 50. Output configuration for stereo BTL mode in filterlight configuration .....	170
Figure 51. VQFN48 (7 x 7 x 0.9 mm) package outline.....	171

# 1 Description

The STA381BW is an integrated solution embedding digital audio processing, digital amplification, FFX<sup>TM</sup> power output stage, headphone and 2 V<sub>rms</sub> line outputs. It is part of the Sound Terminal<sup>®</sup> family and provides full digital audio streaming from the source to the speaker, offering cost effectiveness, low power dissipation and sound enrichment.

The STA381BW input section consists of a flexible digital input serial audio interface, feeding the digital processing unit, and an analog 1 V<sub>rms</sub> input for a seamless connection with pure analog sources. The serial audio data input interface supports many formats, including the popular IIS format.

The STA381BW is based on an FFX<sup>TM</sup> (Fully Flexible Amplification) processor, proprietary technology from STMicroelectronics. FFX<sup>TM</sup> is the evolution of the ST ternary technology: the advanced processor is available for ternary, binary, binary differential and phase shift PWM modulation. The STA381BW embeds the ternary, binary and binary differential implementations, a subset of the full capability of the FFX<sup>TM</sup> processor.

The STA381BW power section consists of four independent half-bridges. These can be configured via digital control to operate in different modes. A 2.1-channel setup can be implemented with two half-bridges (L/R) together with a single full-bridge (subwoofer). Alternatively, the 2.0-channel setup can be done with two full-bridges. When using this configuration, an external amplifier for the SW channel can also be driven through the PWM output. The STA381BW is able to deliver 2 x 20 W (ternary) into an 8 Ω load at 18 V or 2 x 9 W (binary) into a 4 Ω load, plus 1 x 20 W (ternary) into an 8 Ω load at 18 V.

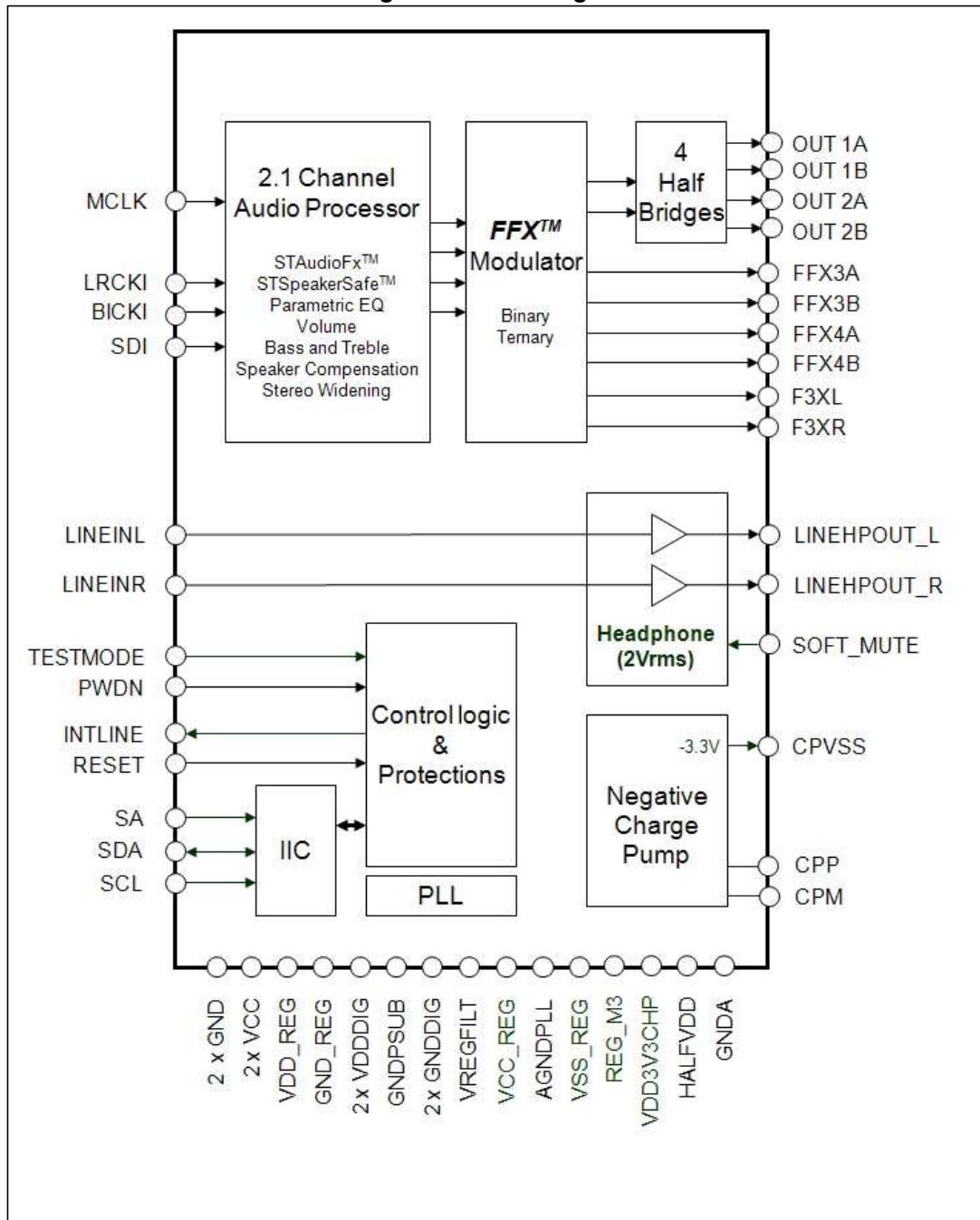
The STA381BW also provides a capless headphone out (with embedded negative charge pump), able to deliver up to 40 mW into a 32 Ω load or, alternatively, can be configured as a 2 V<sub>rms</sub> line output.

The STA381BW digital processing unit includes up to 12 programmable biquads (EQs), allowing perfect sound equalization and offering advanced noise-shaping techniques. Moreover, the coefficient range ensures a great variety of filter shapes (low/high-pass, low/high shelf, peak, notch, band-pass). The equalization engine is fully compatible with the ST speaker compensation technology embedded into the APWorkbench suite. A state-of-the-art multi-band DRC, STCompressor<sup>TM</sup> equalizes the system to provide active speaker protection with full audio quality preservation against sudden sound peaks. Moreover, STSpeakerSafe<sup>TM</sup> technology offers reliable speaker protection under any condition. The master clock can be from stable BICKI (64xfs, 50% duty cycle) or external XTI.



# 1.1 Block diagram

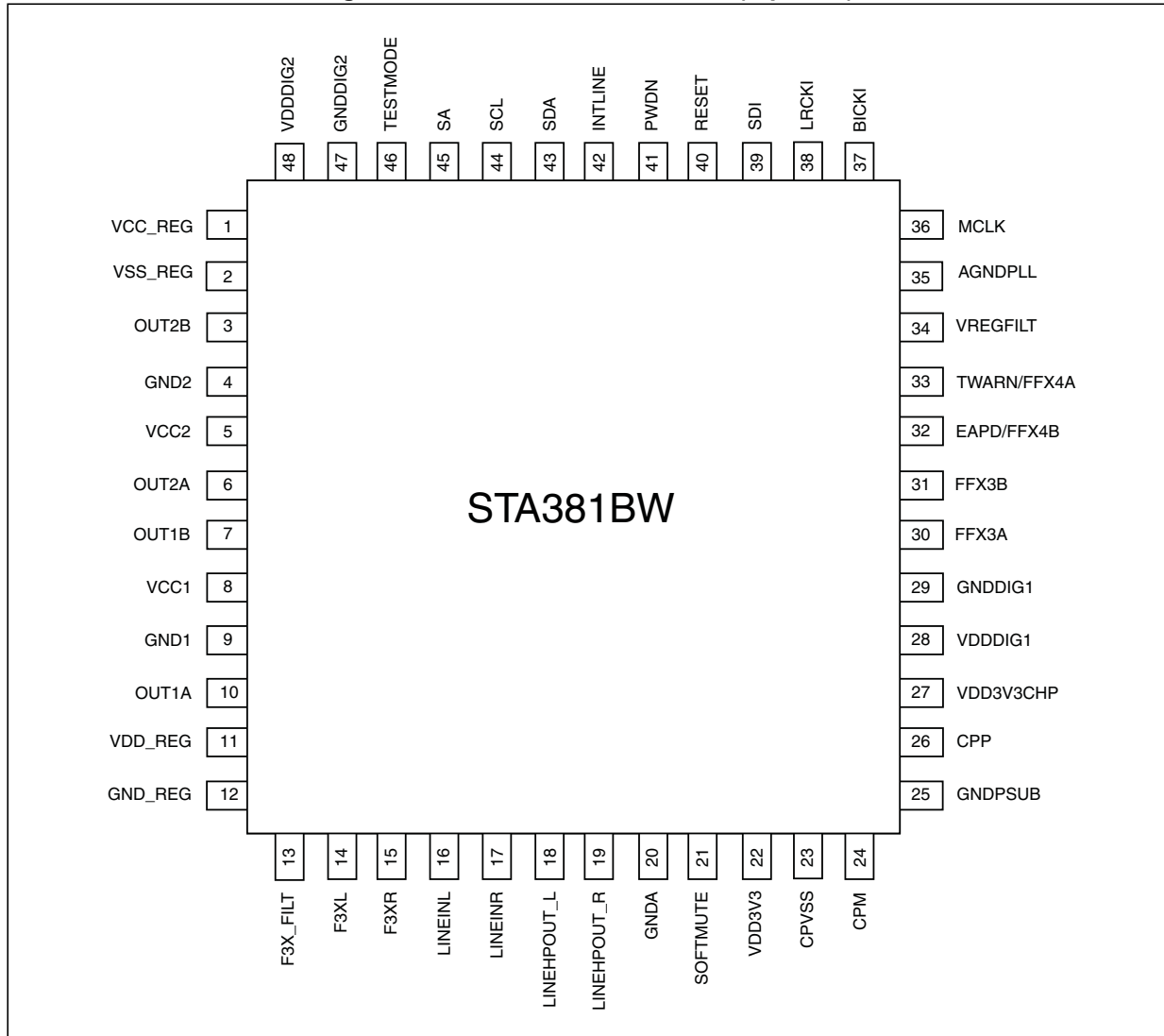
Figure 1. Block diagram



## 2 Pin connections

### 2.1 Connection diagram

Figure 2. Pin connections VQFN48 (top view)



## 2.2 Pin description

Table 2. Pin list

VQFN 48-pin	Name	Type	Description
1	VCC_REG	Power	VCC reg
2	VSS_REG	Power	Vss reg, VCC_REG-3.3 V
3	OUT2B	Output	Half-bridge 2B output
4	GND2	Power	Half-bridge 2A and 2B ground
5	VCC2	Power	Half-bridge 2A and 2B supply
6	OUT2A	Output	Half-bridge 2A output
7	OUT1B	Output	Half-bridge 1B output
8	VCC1	Power	Half-bridge 1A and 1B supply
9	GND1	Power	Half-bridge 1A and 1B ground
10	OUT1A	Output	Half-bridge 1A output
11	VDD_REG	Power	VDD reg 3.3 V
12	GND_REG	Power	DC reg ground
13	F3X_FILT	Power	F3X reference voltage
14	F3XL	Output	F3X analog out left channel
15	F3XR	Output	F3X analog out right channel
16	LINEINL	Input	Line in left channel
17	LINEINR	Input	Line in right channel
18	LINEHPOUT_L	Output	Headphone/line driver left channel
19	LINEHPOUT_R	Output	Headphone/line driver right channel
20	GND_A	Power	Headphone/line driver power ground
21	SOFTMUTE	Input	Soft mute
22	VDD3V3	Power	+3 V LDO power supply
23	CPVSS	Power	-3.3 V charge pump pin
24	CPM	Filter	CHP Cfly negative
25	GNDPSUB	Power	Charge pump ground
26	CPP	Filter	CHP Cfly positive
27	VDD3V3CHP	Power	Charge pump power supply
28	VDDDIG1	Power	I/O ring power supply
29	GNDDIG1	Power	Digital core ground
30	FFX3A	Output	Digital PWM line out
31	FFX3B	Output	Digital PWM line out

Table 2. Pin list (continued)

VQFN 48-pin	Name	Type	Description
32	EAPD/FFX4B	Output	Digital PWM line out
33	TWARN/FFX4A	Output	Digital PWM line out
34	VREGFILT	Power	Digital VDD from core
35	AGNDPLL	Power	PLL analog ground
36	MCLK	Input	PLL input clock
37	BICKI	Input	IIS serial clock
38	LRCKI	Input	IIS left/right clock
39	SDI	Input	IIS serial data input
40	RESET	Input	Reset
41	PWDN	Input	Device power-down 0 = power-down 1 = normal operation
42	INTLINE	Output	Fault interrupt
43	SDA	I/O	IIC serial data
44	SCL	Input	IIC serial clock
45	SA	Input	IIC select address (pull-down)
46	TEST_MODE	Input	This pin must be connected to ground (pull-down)
47	GNDDIG2	Power	Digital I/O ground
48	VDDDIG2	Power	Digital core LDO supply

## 3 Electrical specifications

### 3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
Vcc	Power supply voltage (VCCxA, VCCxB)	-0.3		30	V
VDD_DIG	Digital supply voltage	-0.3		4	V
VDD3V3 VDD3V3CHP	Charge pump and analog path LDO supply	-0.3		4	V
Top	Operating junction temperature	0		150	°C
Tstg	Storage temperature	-40		150	°C
R <sub>Line</sub>	Load impedance - line driver mode	1			kΩ
R <sub>Hp</sub>	Load impedance - headphone driver mode	16			Ω
R <sub>Btl</sub>	Load impedance - power output-BTL mode	5			Ω

**Warning:** Stresses beyond those listed in [Table 3](#) above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended operating conditions” are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, power supplies with nominal values rated within the recommended operating conditions may rise beyond the maximum operating conditions for a short time when no or very low current is sunk (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum ratings are not exceeded.

### 3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
Rth j-case	Thermal resistance junction-case (thermal pad)			1.5	°C/W
Tth-sdj	Thermal shutdown junction temperature		150		°C
Tth-w	Thermal warning temperature		130		°C
Tth-sdh	Thermal shutdown hysteresis		20		°C



### 3.3 Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Min	Typ	Max	Unit
Vcc	Power supply voltage (VCCxA, VCCxB)	4.5		26	V
VDD_DIG	Digital supply voltage	2.7	3.3	3.6	V
VDD3V3 VDD3V3CHP	Charge pump and analog path LDO supply	2.7	3.3	3.6	V
Tamb	Ambient temperature	0		70	°C
R <sub>Line</sub>	Load impedance - line driver mode	5	10		kΩ
R <sub>Hp</sub>	Load impedance - headphone driver mode	16	32		Ω
R <sub>Btl</sub>	Load impedance - power output-BTL mode	5	8		Ω

### 3.4 Electrical specifications for the digital section

The specifications given in this section are valid for the operating conditions:  
VDD\_DIG = 3.3 V, T<sub>amb</sub> = 25 °C.

**Table 6. Electrical specifications - digital section**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>il</sub>	Low level input current without pull-up/down device	V <sub>i</sub> = 0 V			0.5	μA
I <sub>ih</sub>	High level input current without pull-up/down device	V <sub>i</sub> = VDD_DIG = 3.3 V			0.1	μA
V <sub>il</sub>	Low level input voltage				0.8	V
V <sub>ih</sub>	High level input voltage		2.0			V
V <sub>ol</sub>	Low level output voltage	I <sub>ol</sub> = 2 mA			0.15	V
V <sub>oh</sub>	High level output voltage	I <sub>oh</sub> = 2 mA	VDD_DIG - 0.15			V
R <sub>pu</sub>	Pull-up/down resistance			50		kΩ

### 3.5 Electrical specifications for the power section

The specifications given in this section are valid for the operating conditions:  $V_{CC} = 24\text{ V}$ ,  $f = 1\text{ kHz}$ ,  $f_{sw} = 384\text{ kHz}$ ,  $T_{amb} = 25^\circ\text{ C}$  and  $R_L = 8\ \Omega$ , unless otherwise specified.

**Table 7. Electrical specifications - power section**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Po	Output power BTL	Digital limited <sup>(1)</sup>		20		W
	Output power SE	Digital limited <sup>(1)</sup>		5		
	Output power SE $R_L = 4\ \Omega$	Digital limited <sup>(1)</sup>		9		
$R_{dsON}$	Power Pchannel/Nchannel MOSFET	$I_d = 1.5\text{ A}$		120		m $\Omega$
gP	Power Pchannel $R_{dsON}$ matching	$I_d = 1.5\text{ A}$	95			%
gN	Power Nchannel $R_{dsON}$ matching	$I_d = 1.5\text{ A}$	95			%
$I_{dss}$	Power Pchannel/Nchannel leakage				10	$\mu\text{A}$
$I_{LDT}$	Low current dead time (static)	Resistive load <sup>(2)</sup>		8	15	ns
$t_r$	Rise time	Resistive load <sup>(2)</sup>		10	18	ns
$t_f$	Fall time	Resistive load <sup>(2)</sup>		10	18	ns
$I_{VCC}$	Supply current from Vcc in power-down	PWRDN = 0		0.1	1	$\mu\text{A}$
	Supply current from Vcc in operation	PCM Input signal = -60 dBfs, Switching frequency = 384 kHz, No LC filters		52	60	mA
$I_{lim}$	Overcurrent limit		4	5	6.5	A
UVL	Undervoltage protection			3.5	4.3	V
$V_{OV}$	Overvoltage protection			28.25		V
$t_{min}$	Output minimum pulse width	No load	20	30	60	ns
DR	Dynamic range			100		dB
SNR	Signal-to-noise ratio, ternary mode	A-weighted		100		dB
	Signal-to-noise ratio, binary mode	A-weighted		90		dB
THD+N	Total harmonic distortion + noise	FFX stereo mode, $P_o = 1\text{ W}$ , $f = 1\text{ kHz}$		0.2		%
$X_{TALK}$	Crosstalk	FFX stereo mode, <5 kHz, one channel driven at 1 W and other channel measured		80		dB
$\eta$	Peak efficiency, FFX mode	$P_o = 2 \times 20\text{ W}$ into $8\ \Omega$		90		%

1. The related THD can be defined through appropriate DRC settings (see section: [4.3: STCompressorTM](#))

2. Refer to [Figure 3: Test circuit](#).

Figure 3. Test circuit

