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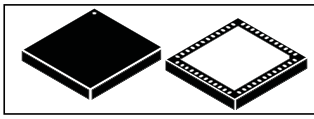
STA381BW

Sound Terminal®
2.1-channel high-efficiency digital audio system

Datasheet - production data



VQFN48 (7 x 7 mm)

Features

- Wide-range supply voltage
  - 4.5 V to 26 V (operating range)
  - 30 V (absolute maximum rating)
- I^2C control with selectable device address
- Embedded full IC protection
  - Manufacturing short-circuit protection (out vs. gnd, out vs. vcc, out vs. out)
  - Thermal protection
  - Overcurrent protection
  - Undervoltage protection
- 1 Vrms stereo analog input
- I^2S interface, sampling rate 32 kHz ~ 192 kHz, with internal sampling frequency converter for fixed processing frequency
- Three output power stage configurations
  - 2.0 mode, L/R full bridges
  - 2.1 mode, L/R two half-bridges, subwoofer full bridge
  - 2.1 mode, L/R full bridges, PWM output for external subwoofer amplifier
- Driving load capabilities
  - 2 x 20 W into 8 Ω ternary modulation
  - 2 x 9 W into 4 Ω + 1 x 20 W into 8 Ω
- FFX™ 100 dB dynamic range
- Fixed output PWM frequency at any input sampling frequency
- Embedded RMS meter for measuring real-time loudness
- Two analog outputs
  - Selectable headphone / line out driver with adjustable gain via external resistors
  - New F3X™ analog output
- New fully programmable noise-gating function
- Headphone
  - Embedded negative charge pump
  - Full capless output configuration
  - Driving load capabilities: 40 mW into 32 Ω
- Line out
  - 2 Vrms line output capability
- Up to 12 user-programmable biquads with noise-shaping technology
- Direct access to coefficients through I^2C shadowing mechanism
- Fixed (88.2 kHz / 96 kHz) internal processing sampling rate
- Two independent DRCs configurable as a dual-band anticlipper or independent limiters/compressors (B^2DRC)
- Digital gain/att +48 dB to -80 dB with 0.125 dB/step resolution
- Independent (fade-in, fade-out) soft volume update with programmable rate 48 ~ 1.5 dB/ms
- Bass/treble tones control
- Audio presets: 15 crossover filters, 5 anticlipping modes, nighttime listening mode
- STSpeakerSafe™ protection circuitry
  - Pre- and post-processing DC blocking filters
  - Checksum engine for filter coefficients
  - PWM fault self-diagnosis
- STCompressor™ dual-band DRC

Table 1. Device summary

Order code	Package	Packing
STA381BW	VQFN48	Tray
STA381BWTR	VQFN48	Tape and Reel

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1 Description

The STA381BW is an integrated solution embedding digital audio processing, digital amplification, FFX™ power output stage, headphone and 2 Vrms line outputs. It is part of the Sound Terminal® family and provides full digital audio streaming from the source to the speaker, offering cost effectiveness, low power dissipation and sound enrichment.

The STA381BW input section consists of a flexible digital input serial audio interface, feeding the digital processing unit, and an analog 1 Vrms input for a seamless connection with pure analog sources. The serial audio data input interface supports many formats, including the popular IIS format.

The STA381BW is based on an FFX™ (Fully Flexible Amplification) processor, proprietary technology from STMicroelectronics. FFX™ is the evolution of the ST ternary technology: the advanced processor is available for ternary, binary, binary differential and phase shift PWM modulation. The STA381BW embeds the ternary, binary and binary differential implementations, a subset of the full capability of the FFX™ processor.

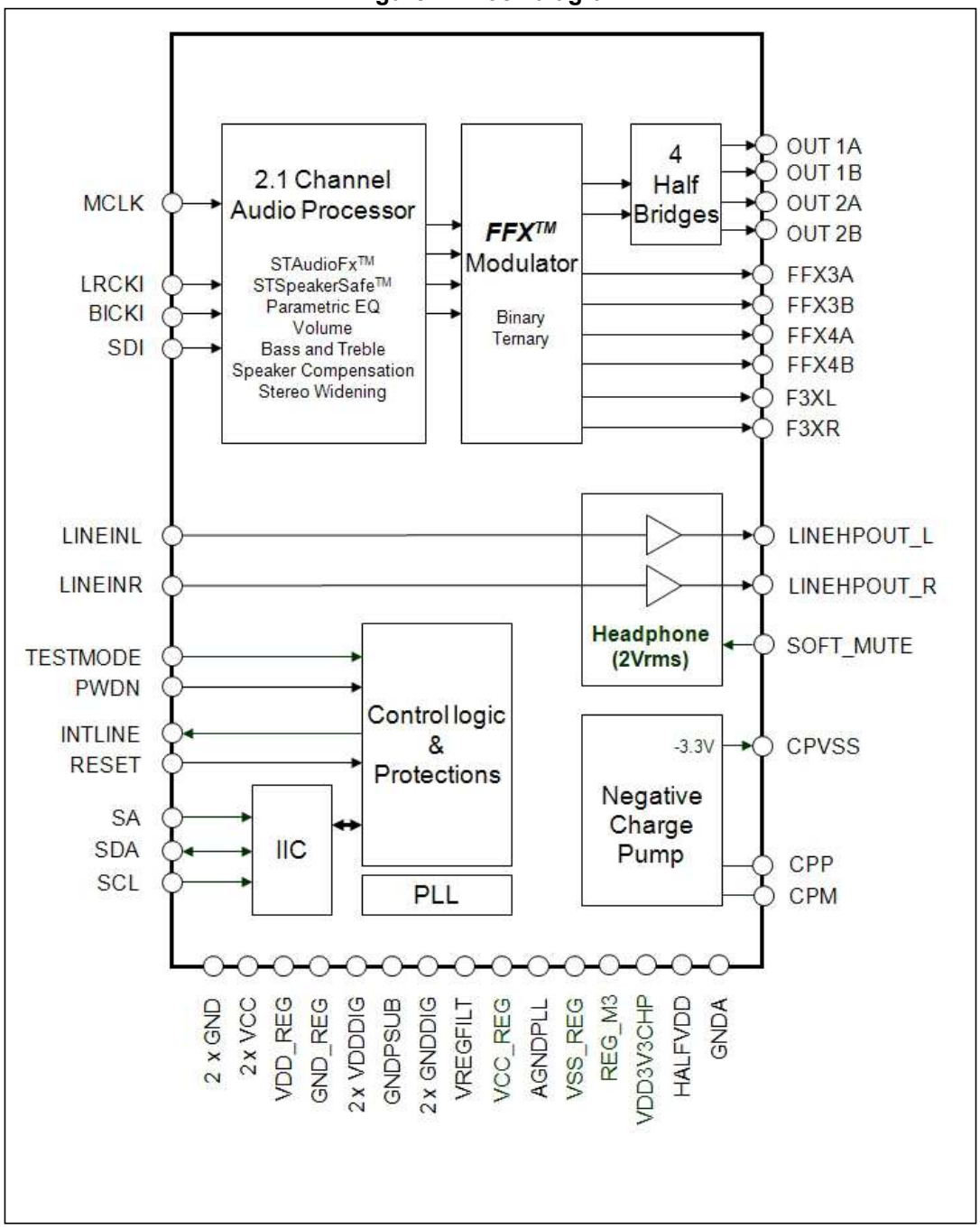
The STA381BW power section consists of four independent half-bridges. These can be configured via digital control to operate in different modes. A 2.1-channel setup can be implemented with two half-bridges (L/R) together with a single full-bridge (subwoofer). Alternatively, the 2.0-channel setup can be done with two full-bridges. When using this configuration, an external amplifier for the SW channel can also be driven through the PWM output. The STA381BW is able to deliver 2 x 20 W (ternary) into an 8 Ω load at 18 V or 2 x 9 W (binary) into a 4 Ω load, plus 1 x 20 W (ternary) into an 8 Ω load at 18 V.

The STA381BW also provides a capless headphone out (with embedded negative charge pump), able to deliver up to 40 mW into a 32 Ω load or, alternatively, can be configured as a 2 Vrms line output.

The STA381BW digital processing unit includes up to 12 programmable biquads (EQs), allowing perfect sound equalization and offering advanced noise-shaping techniques. Moreover, the coefficient range ensures a great variety of filter shapes (low/high-pass, low/high shelf, peak, notch, band-pass). The equalization engine is fully compatible with the ST speaker compensation technology embedded into the APWorkbench suite. A state-of-the-art multi-band DRC, STCompressor™ equalizes the system to provide active speaker protection with full audio quality preservation against sudden sound peaks. Moreover, STSpeakerSafe™ technology offers reliable speaker protection under any condition. The master clock can be from stable BICKI (64xfs, 50% duty cycle) or external XTI.

1.1 Block diagram

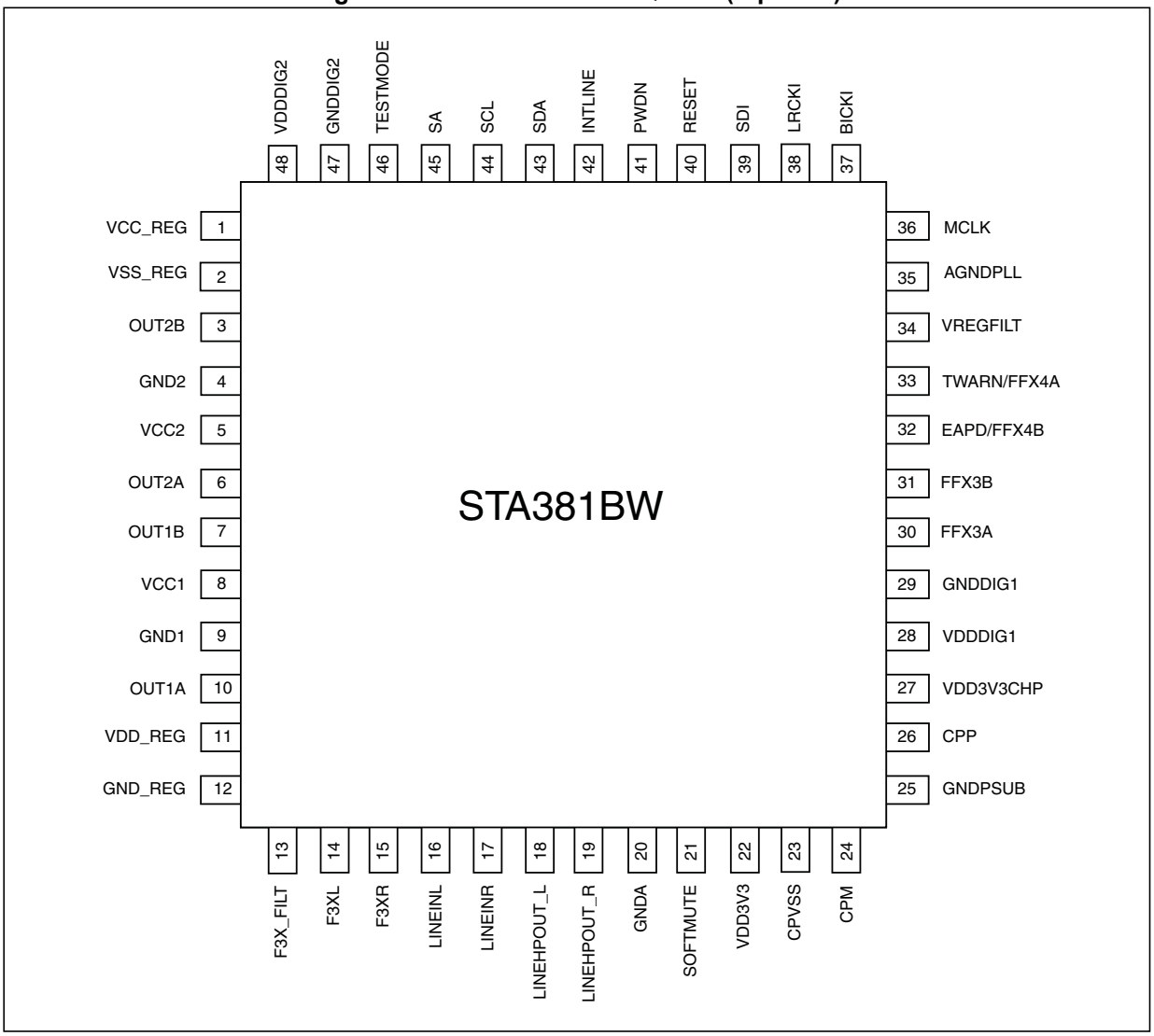
Figure 1. Block diagram



2 Pin connections

2.1 Connection diagram

Figure 2. Pin connections VQFN48 (top view)



2.2 Pin description

Table 2. Pin list

VQFN 48-pin	Name	Type	Description
1	VCC_REG	Power	VCC reg
2	VSS_REG	Power	Vss reg, VCC_REG-3.3 V
3	OUT2B	Output	Half-bridge 2B output
4	GND2	Power	Half-bridge 2A and 2B ground
5	VCC2	Power	Half-bridge 2A and 2B supply
6	OUT2A	Output	Half-bridge 2A output
7	OUT1B	Output	Half-bridge 1B output
8	VCC1	Power	Half-bridge 1A and 1B supply
9	GND1	Power	Half-bridge 1A and 1B ground
10	OUT1A	Output	Half-bridge 1A output
11	VDD_REG	Power	VDD reg 3.3 V
12	GND_REG	Power	DC reg ground
13	F3X_FILT	Power	F3X reference voltage
14	F3XL	Output	F3X analog out left channel
15	F3XR	Output	F3X analog out right channel
16	LINEINL	Input	Line in left channel
17	LINEINR	Input	Line in right channel
18	LINEHPOUT_L	Output	Headphone/line driver left channel
19	LINEHPOUT_R	Output	Headphone/line driver right channel
20	GNDA	Power	Headphone/line driver power ground
21	SOFTMUTE	Input	Soft mute
22	VDD3V3	Power	+3 V LDO power supply
23	CPVSS	Power	-3.3 V charge pump pin
24	CPM	Filter	CHP Cfly negative
25	GNDPSUB	Power	Charge pump ground
26	CPP	Filter	CHP Cfly positive
27	VDD3V3CHP	Power	Charge pump power supply
28	VDDDIG1	Power	I/O ring power supply
29	GNDDIG1	Power	Digital core ground
30	FFX3A	Output	Digital PWM line out
31	FFX3B	Output	Digital PWM line out

Table 2. Pin list (continued)

VQFN 48-pin	Name	Type	Description
32	EAPD/FFX4B	Output	Digital PWM line out
33	TWARN/FFX4A	Output	Digital PWM line out
34	VREGFILT	Power	Digital VDD from core
35	AGNDPLL	Power	PLL analog ground
36	MCLK	Input	PLL input clock
37	BICKI	Input	IIS serial clock
38	LRCKI	Input	IIS left/right clock
39	SDI	Input	IIS serial data input
40	RESET	Input	Reset
41	PWDN	Input	Device power-down 0 = power-down 1 = normal operation
42	INTLINE	Output	Fault interrupt
43	SDA	I/O	IIC serial data
44	SCL	Input	IIC serial clock
45	SA	Input	IIC select address (pull-down)
46	TEST_MODE	Input	This pin must be connected to ground (pull-down)
47	GNDDIG2	Power	Digital I/O ground
48	VDDDIG2	Power	Digital core LDO supply

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
Vcc	Power supply voltage (VCCxA, VCCxB)	-0.3		30	V
VDD_DIG	Digital supply voltage	-0.3		4	V
VDD3V3 VDD3V3CHP	Charge pump and analog path LDO supply	-0.3		4	V
Top	Operating junction temperature	0		150	°C
Tstg	Storage temperature	-40		150	°C
R_{Line}	Load impedance - line driver mode	1			kΩ
R_{Hp}	Load impedance - headphone driver mode	16			Ω
R_{Btl}	Load impedance - power output-BTL mode	5			Ω

Warning: **Stresses beyond those listed in *Table 3* above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended operating conditions" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, power supplies with nominal values rated within the recommended operating conditions may rise beyond the maximum operating conditions for a short time when no or very low current is sunk (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum ratings are not exceeded.**

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
Rth j-case	Thermal resistance junction-case (thermal pad)			1.5	°C/W
Tth-sdj	Thermal shutdown junction temperature		150		°C
Tth-w	Thermal warning temperature		130		°C
Tth-sdh	Thermal shutdown hysteresis		20		°C

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
Vcc	Power supply voltage (VCCxA, VCCxB)	4.5		26	V
VDD_DIG	Digital supply voltage	2.7	3.3	3.6	V
VDD3V3 VDD3V3CHP	Charge pump and analog path LDO supply	2.7	3.3	3.6	V
Tamb	Ambient temperature	0		70	°C
R_{Line}	Load impedance - line driver mode	5	10		kΩ
R_{Hp}	Load impedance - headphone driver mode	16	32		Ω
R_{Btl}	Load impedance - power output-BTL mode	5	8		Ω

3.4 Electrical specifications for the digital section

The specifications given in this section are valid for the operating conditions: VDD_DIG = 3.3 V, T_{amb} = 25 °C.

Table 6. Electrical specifications - digital section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Low level input current without pull-up/down device	V_i = 0 V			0.5	µA
I_{ih}	High level input current without pull-up/down device	V_i = VDD_DIG = 3.3 V			0.1	µA
V_{il}	Low level input voltage				0.8	V
V_{ih}	High level input voltage		2.0			V
V_{ol}	Low level output voltage	I_{ol} = 2 mA			0.15	V
V_{oh}	High level output voltage	I_{oh} = 2 mA	VDD_DIG -0.15			V
R_{pu}	Pull-up/down resistance			50		kΩ

3.5 Electrical specifications for the power section

The specifications given in this section are valid for the operating conditions: V_{CC} = 24 V, f = 1 kHz, f_{sw} = 384 kHz, T_{amb} = 25° C and R_L = 8 Ω, unless otherwise specified.

Table 7. Electrical specifications - power section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Po	Output power BTL	Digital limited(1)		20		W
	Output power SE	Digital limited(1)		5		
	Output power SE R_L = 4 Ω	Digital limited(1)		9		
R_{dsON}	Power Pchannel/Nchannel MOSFET	I_d = 1.5 A		120		mΩ
gP	Power Pchannel R_{dsON} matching	I_d = 1.5 A	95			%
gN	Power Nchannel R_{dsON} matching	I_d = 1.5 A	95			%
Idss	Power Pchannel/Nchannel leakage				10	µA
I_{LDT}	Low current dead time (static)	Resistive load(2)		8	15	ns
t_r	Rise time	Resistive load(2)		10	18	ns
t_f	Fall time	Resistive load(2)		10	18	ns
I_{vcc}	Supply current from Vcc in power-down	PWRDN = 0		0.1	1	µA
	Supply current from Vcc in operation	PCM Input signal = -60 dBfs, Switching frequency = 384 kHz, No LC filters		52	60	mA
Ilim	Overcurrent limit		4	5	6.5	A
UVL	Undervoltage protection			3.5	4.3	V
V_{OV}	Overvoltage protection			28.25		V
t_{min}	Output minimum pulse width	No load	20	30	60	ns
DR	Dynamic range			100		dB
SNR	Signal-to-noise ratio, ternary mode	A-weighted		100		dB
	Signal-to-noise ratio, binary mode	A-weighted		90		dB
THD+N	Total harmonic distortion + noise	FFX stereo mode, Po = 1 W, f = 1 kHz		0.2		%
X_{TALK}	Crosstalk	FFX stereo mode, <5 kHz, one channel driven at 1 W and other channel measured		80		dB
η	Peak efficiency, FFX mode	Po = 2 x 20 W into 8 Ω		90		%

1. The related THD can be defined through appropriate DRC settings (see section: *4.3: STCompressorTM*)
2. Refer to *Figure 3: Test circuit*.

Figure 3. Test circuit