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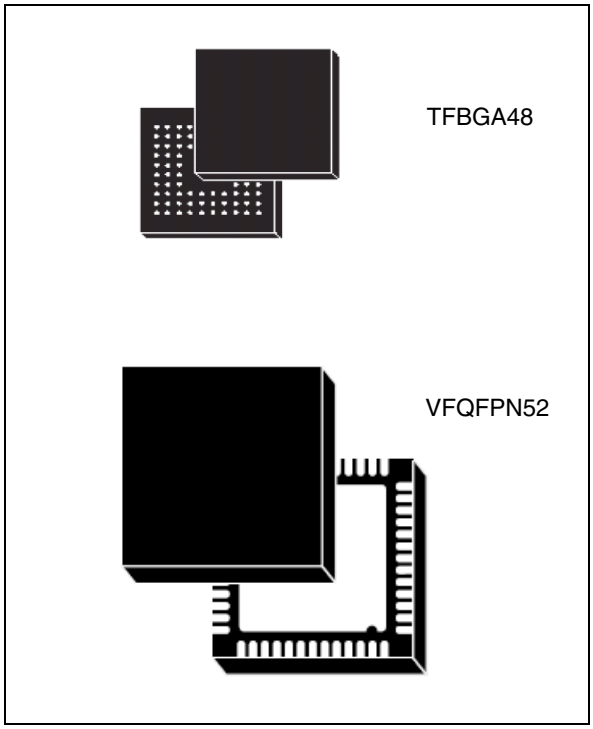
STA529

FFX™ audio codec with analog and digital inputs and 2 x 1.2 W (or 2 x 100 mW HP) class-D amplifier

Datasheet – production data

Features

- Up to 96 dB dynamic range
- Sample rates from 8 kHz to 192 kHz
- FFX™ class-D driver
- 1.55 V to 1.95 V digital power supply
- 1.80 V to 3.60 V analog and I/O power supply
- 18-bit audio processing and class-D FFX™ modulator
- >90-dB SNR analog-to-digital converter
- Digital volume control:
  - +36 dB to -105 dB in 0.5-dB steps
  - Software volume update
- 16-bit ADC
- Individual channel and master gain/attenuation
- Automatic invalid input detect mute
- 2-channel I^2S input/output data interface
- Digitally controlled pop-free operation
- 90% efficiency
- Output power for stereo headphones or stereo speakers applications (at THD = 10% and V_{CC} = 3.3 V):
  - 45 mW with 32-Ω headphones
  - 85 mW with 16-Ω headphones
  - 720 mW with 8-Ω speakers
  - 1.1 W with 4-Ω speakers



Applications

- Portable devices
  - Laptops
  - Digital cameras
  - Microless applications

Table 1. Device summary

Order code	Operating temp. range	Package	Packaging
STA529Q	-40 to 85 °C	VFQFPN52	Tray
STA529	-40 to 85 °C	TFBGA48	Tray

Contents

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List of tables

1 Description

The STA529 is a digital stereo class-D audio amplifier. It includes an audio DSP, an ST proprietary high-efficiency class-D driver and CMOS power output stage. It is intended for high-efficiency digital-to-power-audio conversion for portable applications. The STA529 also provides output capabilities for FFX™. In conjunction with a power device, the STA529 provides high-quality digital amplification.

The STA529 contains an on-chip volume/gain control.

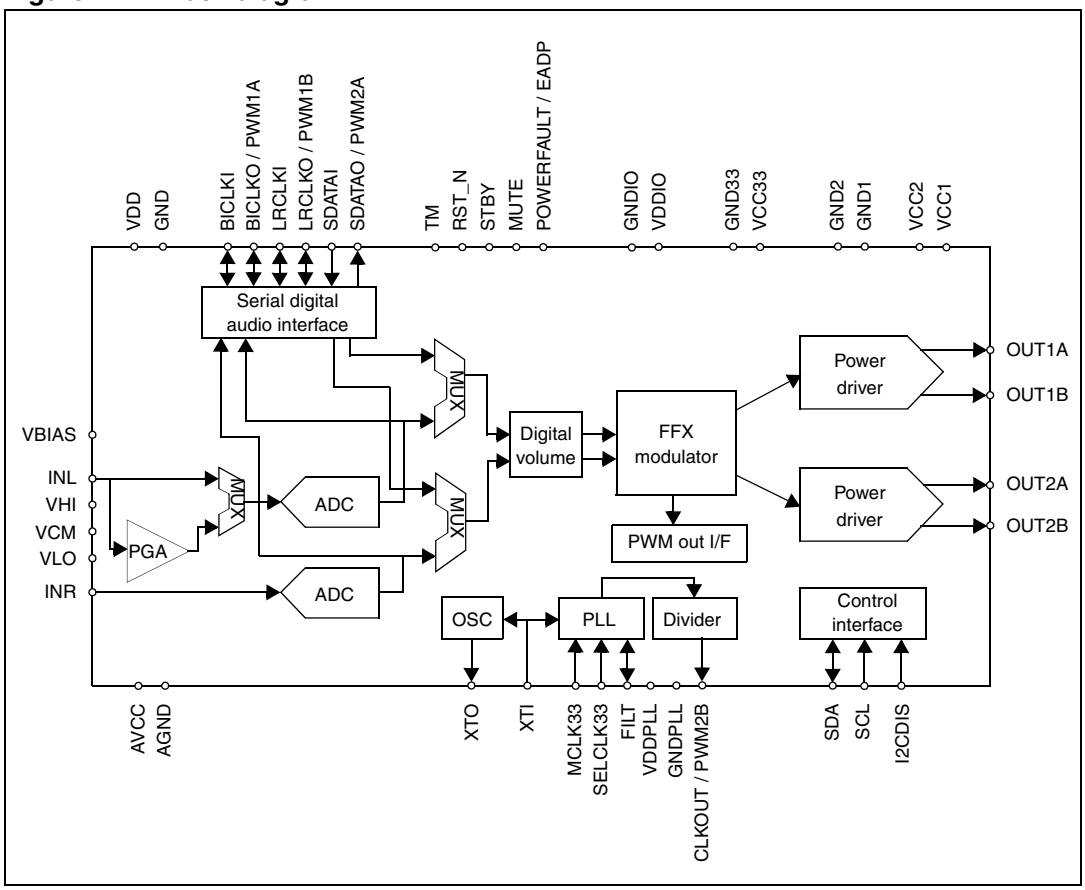
The PWM amplifier achieves greater than 90% efficiency for longer battery life for portable systems.

The innovative class-D modulation, allows the STA529 to work without external LC filters and without a heatsink.

The STA529 I2CDIS pin disables the audio DSP functions and the I^2C interface provides a direct conversion of the input signal into output power. This conversion is done without the microcontroller.

The STA529 is designed for low-power operation with extremely low-current consumption in standby mode. It is available in packages TFBGA48 and VFQFPN52. These are very thin packages (1.2 mm thick) ideal for small portable applications.

Figure 1. Block diagram



2 Connection diagrams and pin descriptions

This section includes connection diagrams and pin descriptions for the following packages:

- TFBGA48
- VFQFPN52

2.1 TFBGA48 package

Figure 2. Connection diagram for TFBGA48 (bottom view)

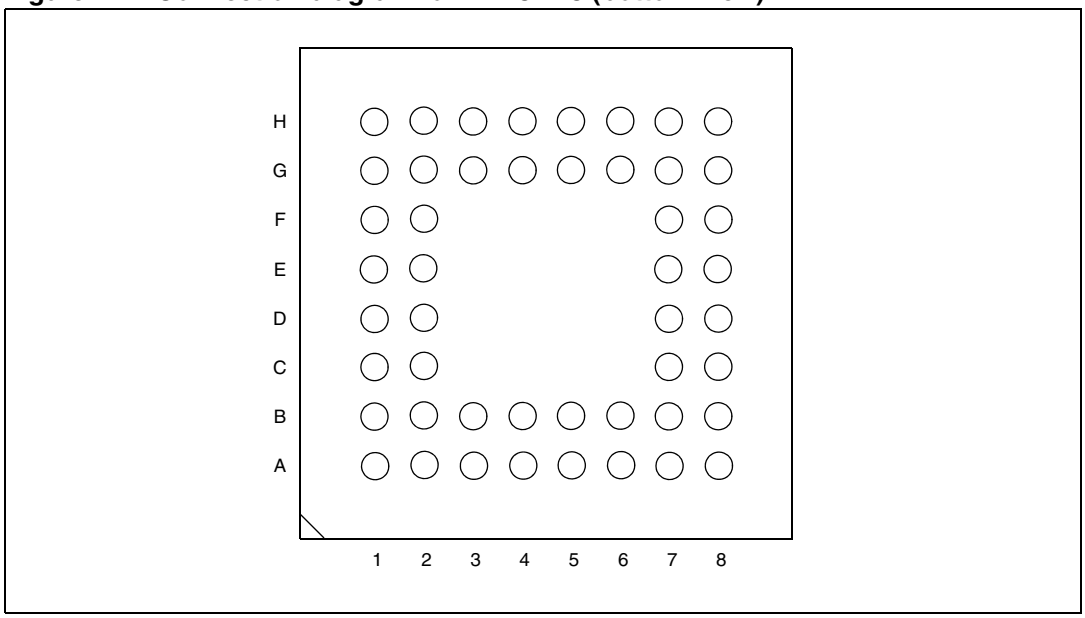


Table 2. Pin description for TFBGA48

Pin	Name	Type	Description
A1	VCC2	Supply	Channel 2 power supply
A2	GND2	Ground	Channel 2 power ground
A3	OUT2A	Analog output	Channel 2 half-bridge A output
A4	OUT2B	Analog output	Channel 2 half-bridge B output
A5	OUT1B	Analog output	Channel 1 half-bridge B output
A6	OUT1A	Analog output	Channel 1 half-bridge A output
A7	GND1	Ground	Channel 1 power ground
A8	VCC1	Supply	Channel 1 power supply
B1	GNDIO	Ground	I/O ring ground
B2	GND33	Ground	Pre-driver ground
B3	OUT2A	Analog output	Channel 2 half-bridge A output
B4	OUT2B	Analog output	Channel 2 half-bridge B output

Table 2. Pin description for TFBGA48 (continued)

Pin	Name	Type	Description
B5	OUT1B	Analog output	Channel 1 half-bridge B output
B6	OUT1A	Analog output	Channel 1 half-bridge A output
B7	MUTE	Digital input	Mute (active high)
B8	GND	Ground	Digital ground
C1	VDDIO	Supply	I/O ring supply
C2	VCC33	Supply	Pre-driver supply
C7	CLKOUT / PWM2B	Digital output	Buffered clock output / PWM2B FFX
C8	VDD	Supply	Digital supply
D1	XTI	Digital input 1.8V	Crystal input or master clock input
D2	XTO	Digital output 1.8V	Crystal output
D7	RST_N	Digital input	Reset (active low)
D8	VCM	Analog I/O	ADC common mode voltage
E1	MCLK33	Digital input	Master clock input 3.3-V capable
E2	SDATAI	Digital input	Input serial audio interface data
E7	VLO	Analog input	ADC low reference voltage
E8	AGND	Ground	ADC analog ground
F1	SCL	Digital input	I^2C serial clock
F2	POWERFAULT / EAPD	Digital output	Power fault signal (active high) / external audio power-down signal
F7	VHI	Analog input	ADC high reference voltage
F8	AVDD	Supply	ADC analog supply
G1	SDA	Digital I/O	I^2C serial data
G2	I2CDIS	Digital input	I^2C disable pin (active high)
G3	SELCLK33	Digital input	Master clock input selector: 0: XTI selected 1: MCLK33 selected
G4	SDATAO / PWM2A	Digital output	Output serial audio interface data / PWM2A FFX
G5	LRCLKO / PWM1B	Digital I/O	Output serial audio interface L/R-clock (volume increases when I2CDIS = 1) / PWM1B FFX
G6	BICLKO / PWM1A	Digital I/O	Output serial audio interface bit-clock (volume decreases when I2CDIS = 1) / PWM1A FFX
G7	VBIAS	Analog I/O	ADC microphone bias voltage
G8	STBY	Digital input	Standby (active high)
H1	FILT	Analog I/O	PLL loop filter terminal

Table 2. Pin description for TFBGA48 (continued)

Pin	Name	Type	Description
H2	TM	Digital input	Test mode (active high)
H3	GNDPLL	Ground	PLL analog ground
H4	VDDPLL	Supply	PLL analog supply
H5	LRCLKI	Digital I/O	Input serial audio interface L/R-clock
H6	BICLKI	Digital I/O	Input serial audio interface bit-clock
H7	INL	Analog input	ADC left channel line input or microphone input
H8	INR	Analog I/O	ADC right channel line input

2.2 VFQFPN52 package

Figure 3. Connection diagram for VFQFPN52 (bottom view)

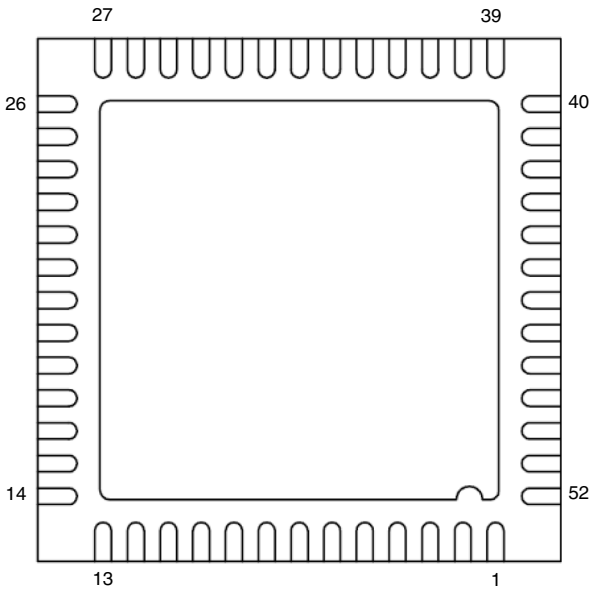


Table 3. Pin description for VFQFPN52

Pin	Name	Type	Description
1	STBY	Digital input	Standby (active high)
2	INL	Analog input	ADC left channel line input or microphone input
3	INR	Analog I/O	ADC right channel line input
4	VBIAS	Analog I/O	ADC microphone bias voltage
5	AVDD	Supply	ADC analog supply
6	VHI	Analog input	ADC high reference voltage
7	VLO	Analog input	ADC low reference voltage

Table 3. Pin description for VFQFPN52 (continued)

Pin	Name	Type	Description
8	AGND	Ground	ADC analog ground
9	VCM	Analog I/O	ADC Common mode voltage
10	RST_N	Digital input	Reset (active low)
11	CLKOUT / PWM2B	Digital output	Buffered clock output / PWM2B FFX
12	GND1	Ground	Digital ground
13	VDD1	Supply	Digital supply
14	MUTE	Digital input	Mute (active high)
15	VCC1A	Supply	Channel 1 half-bridge A power supply
16	OUT1A	Analog output	Channel 1 half-bridge A output
17	GND1A	Ground	Channel 1 half-bridge A power ground
18	GND1B	Ground	Channel 1 half-bridge B power ground
19	OUT1B	Analog output	Channel 1 half-bridge B output
20	VCC1B	Supply	Channel 1 half-bridge B power supply
21	VCC2B	Supply	Channel 2 half-bridge B power supply
22	OUT2B	Analog output	Channel 2 half-bridge B output
23	GND2B	Ground	Channel 2 half-bridge B power ground
24	GND2A	Ground	Channel 2 half-bridge A power ground
25	OUT2A	Analog output	Channel 2 half-bridge A output
26	VCC2A	Supply	Channel 2 half-bridge A power supply
27	GND33	Ground	Pre-driver ground
28	GNDIO1	Ground	I/O ring ground
29	VDDIO1	Supply	I/O ring supply
30	VCC33	Supply	Pre-driver supply
31	POWERFAULT / EAPD	Digital output	Power fault signal (active high) / external audio power down signal
32	TM	Digital input	Test mode (active high)
33	I2CDIS	Digital input	I^2C disable pin (active high)
34	SCL	Digital input	I^2C serial clock
35	SDA	Digital I/O	I^2C serial data
36	SELCLK33	Digital input	Master clock input selector: 0: XTI selected 1: MCLK33 selected
37	MCLK33	Digital input	Master clock input 3.3-V capable
38	XTI	Digital input 1.8V	Crystal input or master clock input

Table 3. Pin description for VFQFPN52 (continued)

Pin	Name	Type	Description
39	XTO	Digital output 1.8V	Crystal output
40	FILT	Analog I/O	PLL loop filter terminal
41	GNDPLL	Ground	PLL analog ground
42	VDDPLL	Supply	PLL analog supply
43	GND2	Ground	Digital ground
44	VDD2	Supply	Digital supply
45	SDATAI	Digital input	Input serial audio interface data
46	SDATAO / PWM2A	Digital output	Output serial audio interface data / PWM2A FFX
47	LRCLKI	Digital I/O	Input serial audio interface L/R-clock
48	LRCLKO / PWM1B	Digital I/O	Output serial audio interface L/R-clock (volume increases when I2CDIS = 1) / PWM1B FFX
49	GNDIO2	Ground	I/O ring ground
50	VDDIO2	Supply	I/O ring supply
51	BICLKI	Digital I/O	Input serial audio interface bit-clock
52	BICLKO / PWM1A	Digital I/O	Output serial audio interface bit-clock (volume decreases when I2CDIS = 1) / PWM1A FFX

3 Electrical and thermal specifications

3.1 Thermal data

Table 4. Thermal data

Device	Parameter	Min	Typ	Max	Unit
TFBGA48	Thermal resistance junction to ambient	-	40	-	°C/W
VFQFPN52	Thermal resistance junction to ambient	-	22	-	°C/W

3.2 Absolute maximum ratings

Table 5. Absolute maximum ratings

Pin/symbol	Description	Min	Max	Unit
VDD VDD1 VDD2	Digital supply voltage	-0.5	+2.5	V
AVDD	ADC supply voltage	-0.5	+4	V
VDDPLL	PLL analog supply voltage	-0.5	+2.5	V
VCC1A VCC1B VCC2A VCC2B	Power stage supply voltage	-0.5	+4	V
VCC33	Pre-driver supply	-0.5	+4	V
VDDIO	Digital I/O supply	-0.5	+4	V
T_{STG}	Storage temperature	-40	150	°C
T_J	Junction temperature	-40	150	°C

Note: All grounds must be within 0.3 V of each other.

3.3 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD VDD1 VDD2	Digital supply voltage	1.55	1.80	1.95	V
AVDD	ADC supply voltage	1.8	3.3	3.6	V
VDDPLL	PLL analog supply voltage	1.55	1.80	1.95	V
VCC1A VCC1B VCC2A VCC2B	Power stage supply voltage	1.8	3.0	3.3	V
VCC33	Pre-driver supply (must be at same level as VCC1A/1B/2A/2B)	1.8	3.0	3.3	V
VDDIO	Power supply for I/Os	1.8	3.0	3.6	V
GND1, GND2, GND33	Channel 1 and 2 power ground, pre-driver ground	-	0	-	V
GNDIO	Ground for I/Os	-	0	-	V
V_{IH}	3.3-V supply	2.0	-	-	V
V_{IL}	3.3-V supply	-	-	0.8	V
V_{HYST}	Schmitt trigger hysteresis (VDDIO)	0.4	-	-	V
T_{AMB}	Ambient operating temperature	-40	-	85	^{o}C

3.4 Electrical characteristics

The electrical specifications in *Table 7* below are given for operation under the recommended conditions listed in *Table 6*. Unless otherwise specified, LRCLKI frequency (fs) = 48 kHz, input frequency = 1 kHz, and R_{LOAD} = 32 Ω.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Eff	Output power efficiency	-	-	90	-	%
R_{dson}	Output stage N/PMOS on-resistance	-	-	250	380	mΩ
IstbyL	Logic power supply current at standby	-	-	1.3	-	µA
IstbyP	Bridges power supply current in standby	-	-	0.7	-	µA
IddL	Logic power supply current at operating	-	-	15	-	mA
IddP	Bridges power supply current at operating	-	-	0.5	-	mA
Tds	Low current dead time (static)	-	-	1	-	ns
Tdd	High current dead time (dynamic)	-	-	2.5	-	ns
Tr	Rise time	-	-	3	-	ns
Tf	Fall time	-	-	3	-	ns
DNR	Dynamic range A-weighted	Speaker mode	-	96	-	dB
SNR	Signal-to-noise ratio (A-weighted)	Speaker mode	-	92	-	dB
THDN	Total harmonic distortion	0 dBFS input, 8 Ω speakers	-	0.1	-	%
		-6 dBFS input, 8 Ω speakers	-	0.05	-	%
		0 dBFS input, 32 Ω headphones	-	0.1	-	%
		-6 dBFS input, 32 Ω headphones	-	0.05	-	%

The following tables give the output power for 1% and 10% THD levels for headphones and speakers.

Table 8. Load power at 1% distortion in headphone mode

Load (Ω)	P (mW) at 1.8 V	P (mW) at 3.3 V
16	20	65
32	10	32

Table 9. Load power at 10% distortion in headphone mode

Load (Ω)	P (mW) at 1.8 V	P (mW) at 3.3 V
16	25	85
32	13	42

Table 10. Load power at 1% distortion in speaker mode

Load (Ω)	P (mW) at 1.8 V	P (mW) at 3.3 V
4	310	860
8	166	560
16	86	290
32	43	147

Table 11. Load power at 10% distortion in speaker mode

Load (Ω)	P (mW) at 1.8 V	P (mW) at 3.3 V
4	400	1100
8	216	720
16	112	380
32	57	200

3.5 Lock time

Table 12 gives the typical lock time of the PLL using the suggested loop filter with 1.8 V supply and 30 ^{o}C junction temperature.

Table 12. PLL lock time

Parameter	Value
Lock time	200 µs

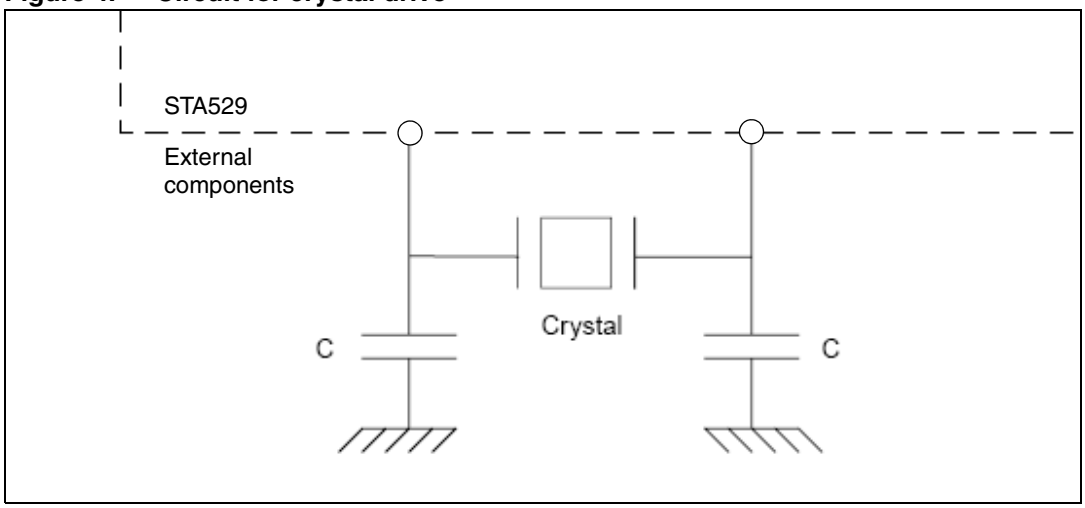
4 Input clock

4.1 SELCLK33

In STA529 the oversampling clock comes from MCLK33 or from pin XTI. The selection is done by applying the appropriate voltage to pin SELCLK33. If SELCLK33 is logical 1 then MCLK33 is selected, otherwise XTI is selected.

If an external crystal is used, SELCLK33 pin must be connected to GND and the suggested circuit shown below should be used.

Figure 4. Circuit for crystal drive



5 Digital processing

The STA529 processor block is a digital block providing two channels of audio processing and channel-mapping capability.

5.1 Signal processing flow

I^2S or stereo ADC data can be selected. The I^2S frequency range is 8 kHz to 192 kHz. The ADC sampling frequency can be selected between 8 kHz and 48 kHz.

5.2 I^2C interface disable

When pin I2CDIS = 1, the SDA, SCL, LRCLKO and BICLKO pins can be pulled high or low to change certain parameters of operation.

- SDA = 0: FFX input comes from ADC
  SDA = 1: FFX input comes from digital audio interface
- SCL = 0: binary output mode (binary soft start/stop enabled)
  SCL = 1: phase shift output mode
- LRCLKO = 0: no volume change
  LRCLKO = 1: channel volume up on both channel
- BICLKO = 0: no volume change
  BICLKO = 1: channel volume down on both xchannel.

At power up, the channel volume is set to -60 dB. When holding pin LRCLKO = 1 and pin BICLKO = 1 simultaneously, the channel volume is set to 0 dB. A high pulse on pin LRCLKO causes a channel volume change of +0.5 dB and a high pulse on pin BICLKO causes a channel volume change of -0.5 dB.

5.3 Volume control and gain

The volume control structure of the STA529 consists of individual volume registers for each channel and a master volume register that provides an offset to each channel's volume setting. The individual channel volumes are adjustable in 0.5-dB steps from +36 dB to -91.5 dB. As an example, if register LVOL = 0x00 or +36 dB and register MVOL = 0x18 or -12 dB, then the total gain for the left channel is +24 dB.

When the mute bit is set to 1, all channels are muted. The volume control provides a soft mute with the volume ramping down to mute in 4096 samples from the maximum volume setting at the internal processing rate (around 48 kHz).

Table 13. Master volume offset as a function of register MVOL

MVOL[7:0]	Volume offset from channel value
0x00	0 dB
0x01	-0.5 dB
0x02	-1dB
…	…
0x78	-60 dB
…	…
0xFE	-105 dB
0xFF	Hard master mute

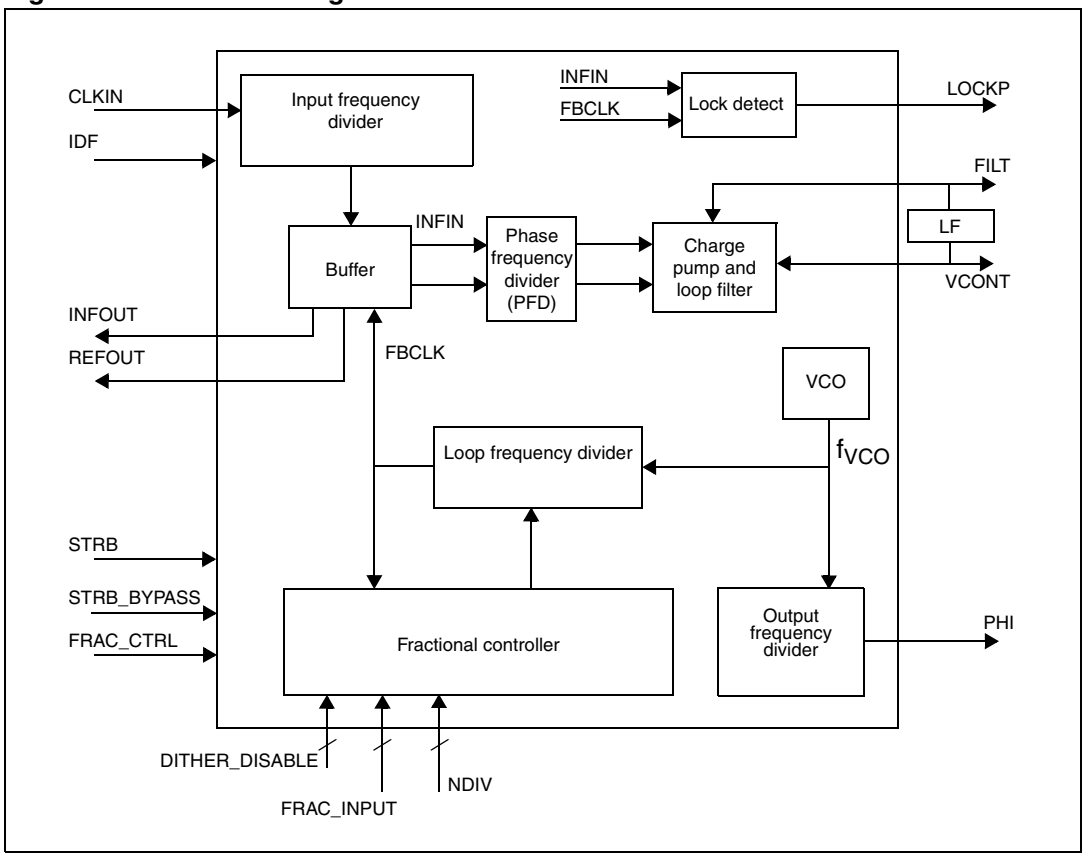
Table 14. Channel volume as a function of registers LVOL and RVOL

LVOL/RVOL[7:0]	Volume
0x00	+36 dB
0x01	+35.5 dB
0x02	+35 dB
…	…
0x47	+0.5 dB
0x48	0 dB
0x49	-0.5 dB
…	…
…	…
0xFF	-91.5 dB

6 PLL

Figure 5 shows the main components of the PLL.

Figure 5. PLL block diagram



6.1 Functional description

Phase/frequency detector

The phase/frequency detector (PFD) compares the phase difference between the corresponding rising edges of INFIN and FBCLK, (clock output from the loop frequency divider) by generating voltage pulses with widths proportional to the input phase error.

Charge pump and loop filter

This block converts the voltage pulses from the phase/frequency detector to current pulses which charge the loop filter and generate the control voltage for the voltage-controlled oscillator. The loop filter is placed external to the PLL on pin FILT.

Voltage controlled oscillator

The voltage controlled oscillator (VCO) is the oscillator inside the PLL. It produces a frequency (f_{VCO}) proportional to the input control voltage.

Input frequency divider

This frequency divider divides the PLL input clock CLKIN by a factor called the input division factor (IDF) to generate the PFD input frequency INFIN.

Loop frequency divider

This frequency divider is present within the PLL for dividing f_{VCO} by a factor called the loop division factor (LDF). The output of this block is clock FBCLK.

Output frequency divider

The output frequency divider divides f_{VCO} by the output division factor (ODF) to produce the output clock PHI and the clock to the core. In the STA529, ODF = 2 and cannot be reconfigured.

Lock-detect circuit

The output of this block (signal LOCKP) is asserted high when the PLL enters the state of Coarse Lock in which the output frequency is within ±10%, approximately, of the desired frequency. LOCKP is refreshed every 32 cycles of clock INFIN. The generated value is based on the result of comparing the number of FBCLK cycles in a window of 14 INFIN cycles. The different cases generated after comparison are as follows.

- If LOCKP is already at 0, then in the next refresh cycle LOCKP goes to 1 if the number of FBCLK cycles in the 14-cycle INFIN window is 13, 14, or 15. Otherwise LOCKP stays at 0.
- If LOCKP is already at 1, then in the next refresh cycle LOCKP goes to 0 if the number of FBCLK cycles in the 25-cycle INFIN window is less than 11 or higher than 17, otherwise LOCKP stays at 1.
- If LOCKP is already at 1 and CLKIN is lost (no longer present on the input pin), LOCKP stays at 1. In this case, the PLL is unlocked.

PLL filter

Figure 6 below shows the PLL filter circuit. Recommended values are R1 = 12.5 kΩ, C1 = 250 pF and C2 = 82 pF.

Figure 6. PLL filter circuit

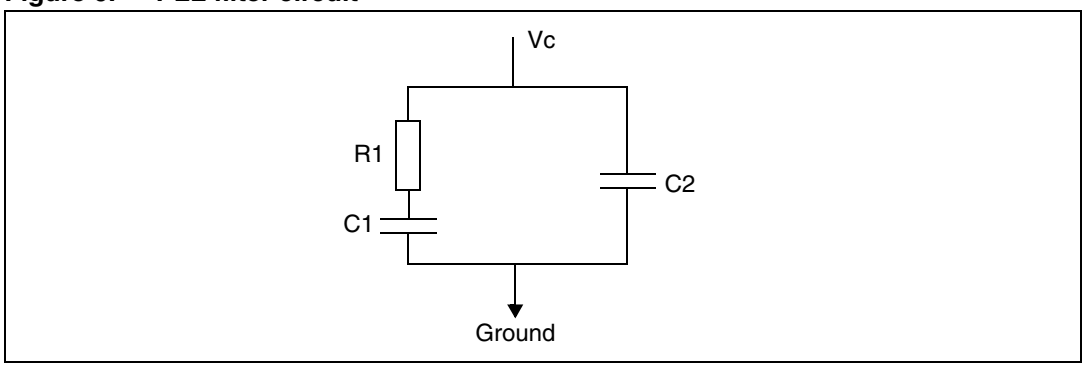


Table 12 on page 16 gives a typical lock time value for the PLL.

6.2 Configuration examples

The STA529 PLL can be configured in two ways:

- default startup configuration
- direct PLL programming

The default startup configuration reads the device defaults. With this configuration, it is not necessary to program the PLL dividers directly as preset values are used. In this mode, the oversampling ratio between pins XTI (or MCLK33) and LRCLKI is fixed to 256.

The direct PLL programming bypasses the automatic presets allowing direct programming of the PLL dividers.

The output PLL frequency can be determined by the following equations.

Output division factor:

ODF = 2.

Relation between input and output clock frequency:

$f_{INFIN} = f_{XTI} / IDF$.

If register bit PLLCFG0.FRAC_CTRL = 1

$f_{VCO} = f_{INFIN} * (LDF + FRACT / 2^{16} + 1 / 2^{17})$

$f_{PHI} = f_{VCO} / ODF$.

When register bit PLLCFG0.DITHER_DISABLE[1] = 1, the $1/2^{17}$ factor is not in the multiplication. This is recommended in order to keep register bit PLLCFG0.DITHER_DISABLE[1] = 0, otherwise there can be spurious signals in the output clock spectrum.

If register bit PLLCFG0.FRAC_CTRL = 0, then:

$f_{VCO} = f_{INFIN} * LDF$

$f_{PHI} = f_{VCO} / ODF$.

In the above equations:

FRACT = decimal equivalent of register bit PLLCFG1.FRAC_INPUT[15:0]

IDF = input division factor

LDF = loop division factor

ODF = output division factor = 2

f_{INFIN} = INFIN frequency

f_{XTI} = XTI frequency

f_{VCO} = VCO frequency

f_{PHI} = frequency of the PLL output clock.

When selecting the values for IDF, LDF and FRACT, ensure that the following limits are maintained:

2.048 MHz < f_{XTI} < 49.152 MHz

2.048 MHz < f_{INFIN} < 16.384 MHz

65.536 MHz < f_{VCO} < 98.304 MHz

There are also some additional constraints on IDF and LDF. IDF should be greater than 0, LDF should be greater than 5 if FRAC_CTRL = 0 and greater than 8 if FRAC_CTRL = 1.

When automatic settings are not used, the PLL must be configured to generate an internal frequency, f_{PHI}, of N * fs, where fs is the frequency of pin LRCLKI. Values for N are given in *Table 15*.

Table 15. Oversampling table

fs (kHz)	N	f_{PHI} (MHz)
8	4096	32.768
11.025	4096	45.1584
12	4096	49.152
16	2048	32.768
22.05	2048	45.1584
24	2048	49.152
32	1024	32.768
44.1	1024	45.1584
48	1024	49.152
64	512	32.768
88.2	512	45.1584
96	512	49.152
128	256	32.768
176.4	256	45.1584
192	256	49.152

Example 1

f_{XTI} = 13 MHz and fs = 44.1 kHz

IDF should be equal to 3 otherwise LDF becomes less than 8 (FRAC_CTRL must be 1):

LDF = floor(45.1584 / (13 / IDF)) = 10

FRACT = round([(45.1584 / (13 / IDF)) - floor(45.1584 / (13 / IDF))] * 2^{16}) = 27602.

where:

floor means rounded down and
round means rounded to nearest integer.

Using the above configuration, the system clock is 45.15841675 MHz, the approximate static error is 16 Hz (that is, 0.5 ppm).

Example 2

f_{XTI} = 19.2 MHz and fs = 48 kHz

IDF should be equal to 4 otherwise LDF become less than 8 (FRAC_CTRL must be 1):

LDF = floor(49.152 / (19.2 / IDF)) = 10

FRACT = round([(49.152 / (19.2 / IDF)) - floor(49.152 / (19.2 / IDF))] * 2^{16}) = 15728.

Using the above configuration, the system clock is 49.151953125 MHz, the approximate static error is 47 Hz (that is, 1 ppm).

6.3 Set fractional PLL

The following procedure is mandatory to configure the fractional PLL:

1. Set bit D7 reg 0x18 (PLL_BYP_UNL) to "1"
2. Write reg 0x17 (PLLCFG3)
3. Write reg 0x14 (PLLCFG0)
4. Write reg 0x15 (PLLCFG1)
5. Write reg 0x16 (PLLCFG2)
6. Set bit D7 reg 0x18 (PLL_BYP_UNL) to "0"

7 ADC

7.1 ADC performance values

Table 16. Programmable gain performance

Parameter	Min	Typ	Max	Unit
Dynamic range 1 kHz, A-weighted (3.3 V supply)		92		dB
Dynamic range 1 kHz, A-weighted (1.8 V supply)		84		dB
SNDR 1 kHz, A-weighted (3.3 V supply)		92		dB
SNDR 1 kHz, A-weighted (1.8 V supply)		84		dB
THD 1 kHz (-1 dB input) (3.3 V supply)		-85		dB
THD 1 kHz (-1 dB input) (1.8 V supply)		-75		dB
Cross talk (3.3 V supply)		-80		dB
Cross talk (1.8 V supply)		-60		dB

7.2 Functional description

The STA529 analog input is provided through a low-power, low-voltage, 16-bit stereo audio analog-to-digital converter front end designed for audio applications. It includes a programmable gain amplifier, anti-aliasing filter, low-noise microphone biasing circuit, third-order MASH2-1 delta-sigma modulator, digital decimating filter and a first-order DC-removal filter.

The ADC works in the microphone input (mic-in) mode and in the line-input mode. If the line input mode is selected, the ADC is configured in stereo and all conversion channels are active.

If the microphone input mode is selected, the ADC is configured in mono. The mono channel is routed through the left conversion path, and the right conversion path is kept in power-down mode to minimize power consumption. A programmable gain amplifier (PGA) is available in mic-in mode, making it possible to amplify the signal from 0 to +42 dB in steps of 6 dB.