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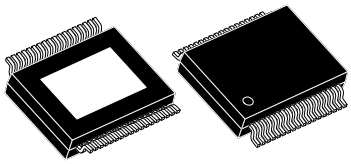
STA559BW

5 V, 2 A, 2.1 channel high-efficiency digital audio system Sound Terminal®

Datasheet - production data



PowerSSO-36

with exposed pad down (EPD)

Features

- Wide-range supply voltage, 4.5 V to 16 V
- Three power output configurations:
  - 2 channels of ternary PWM (2 x 3 W into 4 Ω at 5 V) + PWM output
  - 2 channels of ternary PWM (2 x 3 W into 4 Ω at 5 V) + ternary stereo line-out
  - 2.1 channels of binary PWM (left, right, LFE) (2 x 0.7 W + 1 x 3 W into 4 Ω at 5 V) (2 x 1.4 W + 1 x 6 W into 2 Ω at 5 V)
- FFX with 100-dB SNR and dynamic range
- Selectable 32- to 192-kHz input sample rates
- I²C control with selectable device address
- Digital gain/attenuation +48 dB to -80 dB with 0.5-dB/step resolution
- Soft volume update
- Individual channel and master gain/attenuation
- Two independent limiters/compressors
- Dynamic range compression or anti-clipping modes
- Audio presets:
  - 15 preset crossover filters
  - 5 preset anti-clipping modes
  - Preset night-time listening mode
- Individual channel soft/hard mute
- Independent channel volume and DSP bypass
- 2-channel I²S input data interface
- Input and output channel mapping
- Automatic invalid-input detect Mute
- Automatic zero-detect mute
- Up to 4 user-programmable biquads/channel
- Three coefficients banks for EQ presets storing with fast recall via I²C interface
- Bass/treble tones and de-emphasis control
- Selectable high-pass filter for DC blocking
- Advanced AM interference frequency switching and noise suppression modes
- Selectable high- or low-bandwidth noise-shaping topologies
- Selectable clock input ratio
- Thermal overload and short-circuit protection embedded
- Video apps: 576 x f_S input mode supported

Table 1. Device summary

Order code	Package	Packaging
STA559BWTR	PowerSSO-36 EPD	Tape and reel

Contents

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1 Description

The STA559BW is an integrated solution of digital audio processing, digital amplifier controls and power output stage to create a high-power single-chip FFX digital amplifier with high-quality and high-efficiency. Three channels of FFX processing are provided. The FFX processor implements the ternary, binary and binary differential processing capabilities of the full FFX processor.

The STA559BW is part of the Sound Terminal® family that provides full digital audio streaming to the speakers and offers cost effectiveness, low power dissipation and sound enrichment.

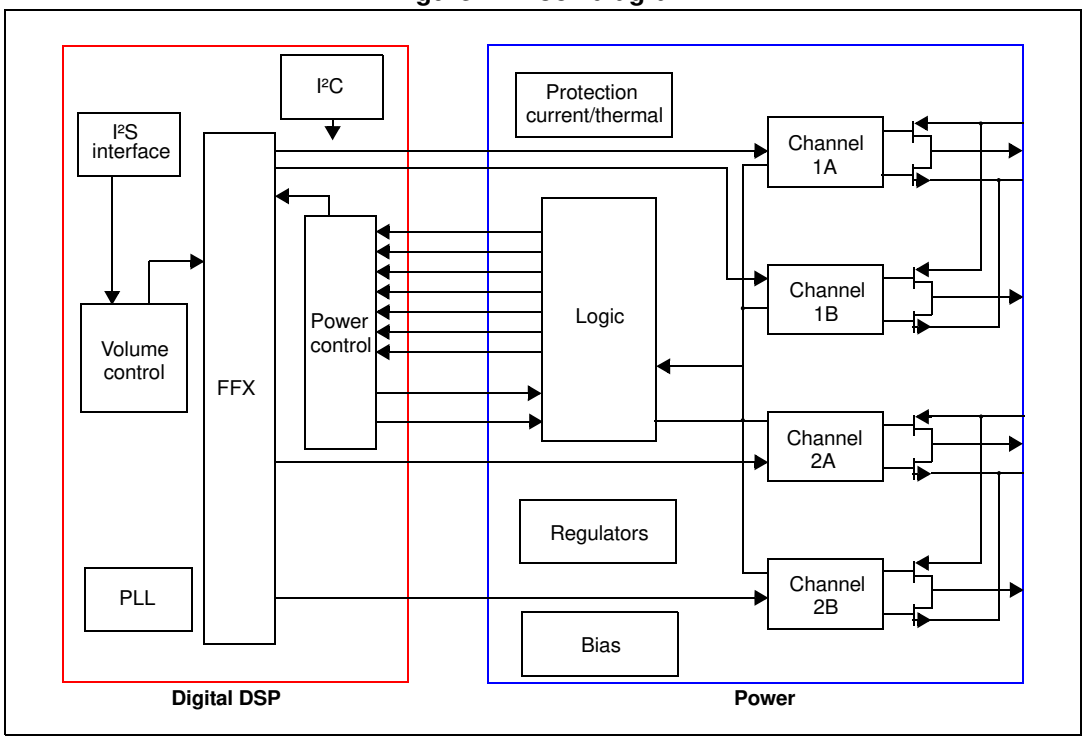
The power section consists of four independent half-bridges. These can be configured via digital control to operate in different modes.

For example, 2.1 channels can be provided by two half bridges and a single full bridge, supplying up to 2 x 1.4 W + 1 x 6 W of output power or two channels can be provided by two full-bridges, supplying up to 2 x 3 W of output power.

The IC can also be configured as 2.1 channels with 2 x 20 W supplied by the device plus a drive for an external FFX power amplifier, such as STA533WF or STA515W.

Also provided in the STA559BW are a full assortment of digital processing features. This includes up to four programmable biquads (EQ) per channel. Available presets enable a time-to-market advantage by substantially reducing the amount of software development needed for functions such as audio preset volume loudness, preset volume curves and preset EQ settings. There are also new advanced AM radio interference reduction modes.

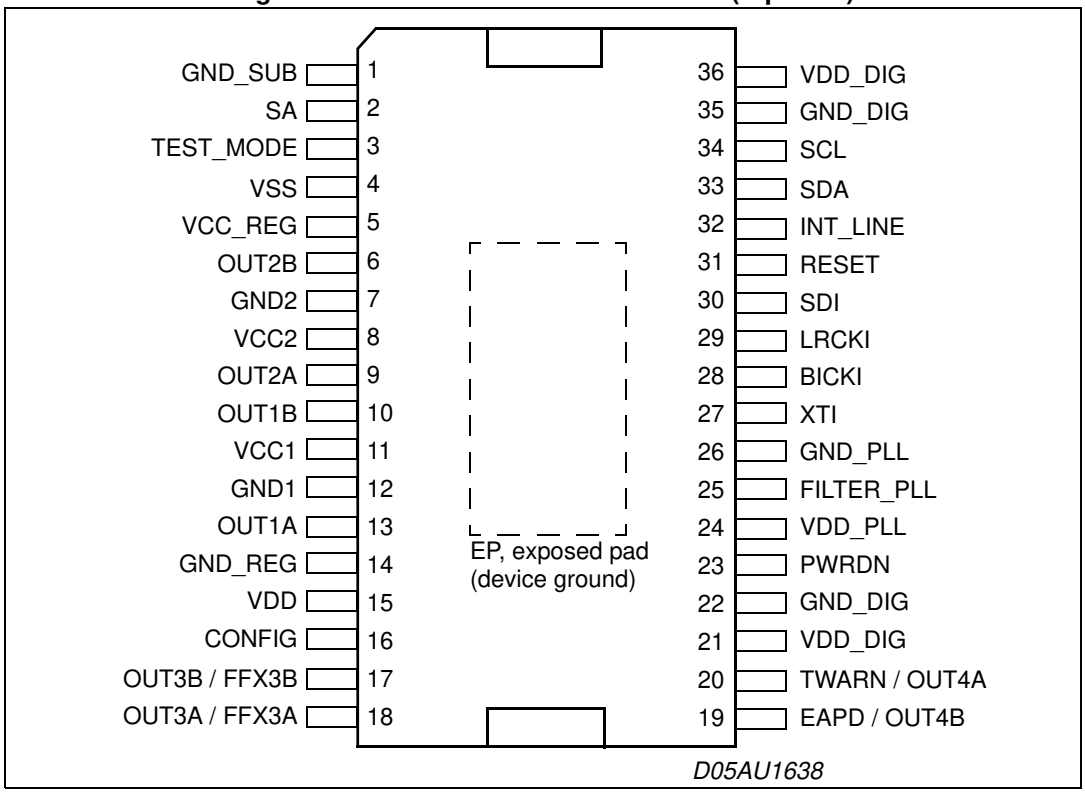
Figure 1. Block diagram



2 Pin connections

2.1 Connection diagram

Figure 2. Pin connection PowerSSO-36 (top view)



2.2 Pin description

Table 2. Pin description

Pin	Type	Name	Description
1	GND	GND_SUB	Substrate ground
2	I	SA	I²C select address (pull-down)
3	I	TEST_MODE	This pin must be connected to ground (pull-down)
4	I/O	VSS	Internal reference at V_{CC} - 3.3 V
5	I/O	VCC_REG	Internal V_{CC} reference
6	O	OUT2B	Output half-bridge channel 2B
7	GND	GND2	Power negative supply
8	Power	VCC2	Power positive supply
9	O	OUT2A	Output half-bridge channel 2A
10	O	OUT1B	Output half-bridge channel 1B

Table 2. Pin description (continued)

Pin	Type	Name	Description
11	Power	VCC1	Power positive supply
12	GND	GND1	Power negative supply
13	O	OUT1A	Output half-bridge channel 1A
14	GND	GND_REG	Internal ground reference
15	Power	VDD	Internal 3.3 V reference voltage
16	I	CONFIG	Parallel mode command
17	O	OUT3B / FFX3B	PWM out channel 3B / external bridge driver
18	O	OUT3A / FFX3A	PWM out channel 3A / external bridge driver
19	O	EAPD / OUT4B	Power down for external bridge / PWM out channel 4B
20	I/O	TWARN / OUT4A	Thermal warning from external bridge (pull-up when input) / PWM out channel 4A
21	Power	VDD_DIG	Digital supply voltage
22	GND	GND_DIG	Digital ground
23	I	PWRDN	Power down (pull-up)
24	Power	VDD_PLL	Positive supply for PLL
25	I	FILTER_PLL	Connection to PLL filter
26	GND	GND_PLL	Negative supply for PLL
27	I	XTI	PLL input clock
28	I	BICKI	I²S serial clock
29	I	LRCKI	I²S left/right clock
30	I	SDI	I²S serial data channels 1 and 2
31	I	RESET	Reset (pull-up)
32	O	INT_LINE	Fault interrupt
33	I/O	SDA	I²C serial data
34	I	SCL	I²CI²C serial clock
35	GND	GND_DIG	Digital ground
36	Power	VDD_DIG	Digital supply voltage
-	-	EP	Exposed pad for PCB heatsink, to be connected to GND

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power supply voltage (pins VCCx)	-0.3	-	24	V
V_{DD}	Digital supply voltage (pins VDD_DIG)	-0.3	-	4.0	V
V_{DD}	PLL supply voltage (pin VDD_PLL)	-0.3	-	4.0	V
T_{op}	Operating junction temperature	-20	-	150	°C
T_{stg}	Storage temperature	-40	-	150	°C

Warning: **Stresses beyond those listed in *Table 3* above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended operating conditions" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, power supplies with nominal values rated within the recommended operating conditions, may experience some rising beyond the maximum operating conditions for a short time when no or very low current is sinked (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum ratings are not exceeded.**

3.2 Thermal data

Table 4. Thermal data

	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-case (thermal pad)	-	-	1.5	°C/W
$T_{th\text{-}sdj}$	Thermal shut-down junction temperature	-	150	-	°C
$T_{th\text{-}w}$	Thermal warning temperature	-	130	-	°C
$T_{th\text{-}sdh}$	Thermal shut-down hysteresis	-	20	-	°C
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient (1)	-	24	-	°C/W

1. See *Chapter 8: Package thermal characteristics on page 63* for details.

3.3 Recommended operating conditions

Table 5. Recommended operating condition

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power supply voltage (VCCxA, VCCxB)	4.5	-	16.0	V
V_{DD_DIG}	Digital supply voltage	2.7	3.3	3.6	V
V_{DD_PLL}	PLL supply voltage	2.7	3.3	3.6	V
T_{amb}	Ambient temperature	-20	-	70	°C

3.4 Electrical specifications for the digital section

The specifications given in this section are valid for T_{amb} = 25 °C unless otherwise specified.

Table 6. Electrical specifications - digital section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Low level input current without pull-up/down device	Vi = 0 V	-	-	1	µA
I_{ih}	High level input current without pull-up/down device	Vi = VDD_DIG = 3.6 V	-	-	1	µA
V_{il}	Low level input voltage	-	-	-	0.2 * VDD_DIG	V
V_{ih}	High level input voltage	-	0.8 * VDD_DIG	-	-	V
V_{ol}	Low level output voltage	Iol = 2 mA		-	0.4 * VDD_DIG	V
V_{oh}	High level output voltage	Ioh = 2 mA	0.8 * VDD_DIG	-	-	V
R_{pu}	Equivalent pull-up/down resistance	-	-	50	-	kΩ

3.5 Electrical specifications for the power section

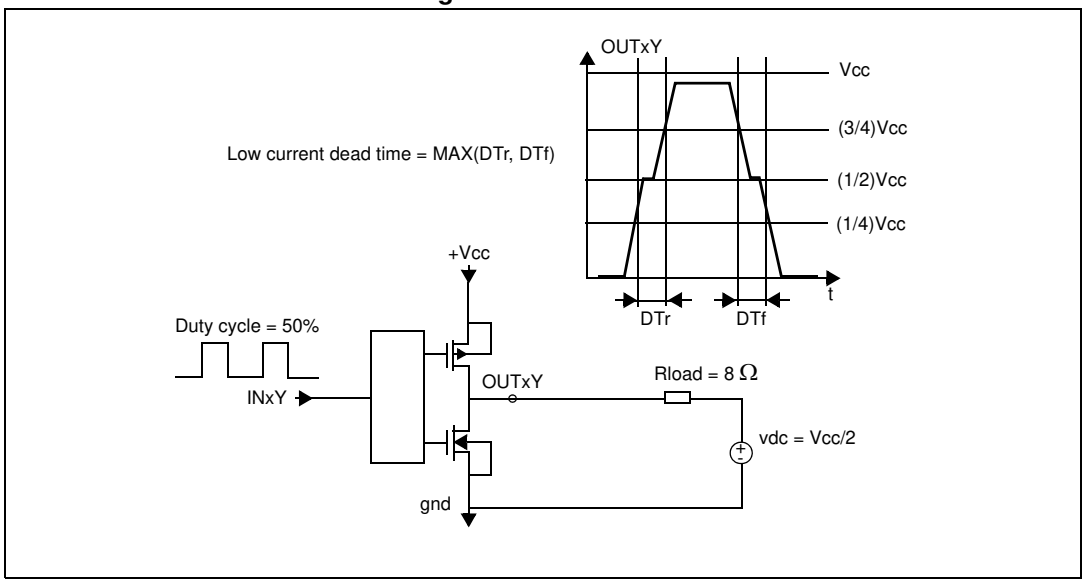
The specifications given in this section are valid for the operating conditions: V_{CC} = 5 V, f = 1 kHz, f_{sw} = 384 kHz, T_{amb} = 25 °C and R_L = 4 Ω, unless otherwise specified.

Table 7. Electrical specifications - power section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Po	Output power BTL	THD = 1%R_L= 2 Ω	-	4.2	-	W
		THD = 10%R_L= 2 Ω	-	5.3	-	
	Output power SE	THD = 1%,R_L= 2 Ω	-	1	-	W
		THD = 10%,R_L= 2 Ω	-	1.3	-	
R_{dsON}	Power P-channel or N-channel MOSFET	I_d = 0.75 A	-	-	250	mΩ
gP	Power P-channel RdsON matching	I_d = 0.75 A	-	100	-	%
gN	Power N-channel RdsON matching	I_d = 0.75 A	-	100	-	%
Idss	Power P-channel/N-channel leakage	Vcc=9V	-	-	1	µA
t_r	Rise time	Resistive load, see *Figure 3* below	-	-	10	ns
t_f	Fall time		-	-	10	ns
I_{VCC}	Supply current from V_{CC} in power down	PWRDN = 0	-	0.3	-	µA
	Supply current from V_{CC} in operation	PWRDN = 1	-	15	-	mA
I_{VDD}	Supply current FFX processing	Internal clock = 49.152 MHz	-	55	-	mA
I_{LIM}	Overcurrent limit	(1)	2.2	3.0	-	A
I_{SCP}	Short -circuit protection	R_L = 0 Ω	2.7	3.6	-	A
V_{UVP}	Undervoltage protection	-	-	-	4.3	V
t_{min}	Output minimum pulse width	No load	20	40	60	ns
DR	Dynamic range	-	-	100	-	dB
SNR	Signal to noise ratio, ternary mode	A-Weighted	-	100	-	dB
	Signal to noise ratio binary mode	-	-	90	-	dB
THD+N	Total harmonic distortion + noise	FFX stereo mode, Po = 1 W f = 1 kHz	-	0.2	-	%
X_{TALK}	Crosstalk	FFX stereo mode, <5 kHz One channel driven at 1 W, other channel measured	-	80	-	dB
η	Peak efficiency, FFX mode	Po = 2 x 20 W into 8 Ω	-	90	-	%
	Peak efficiency, binary modes	Po = 2 x 9 W into 4 Ω + 1 x 20 W into 8 Ω	-	87	-	

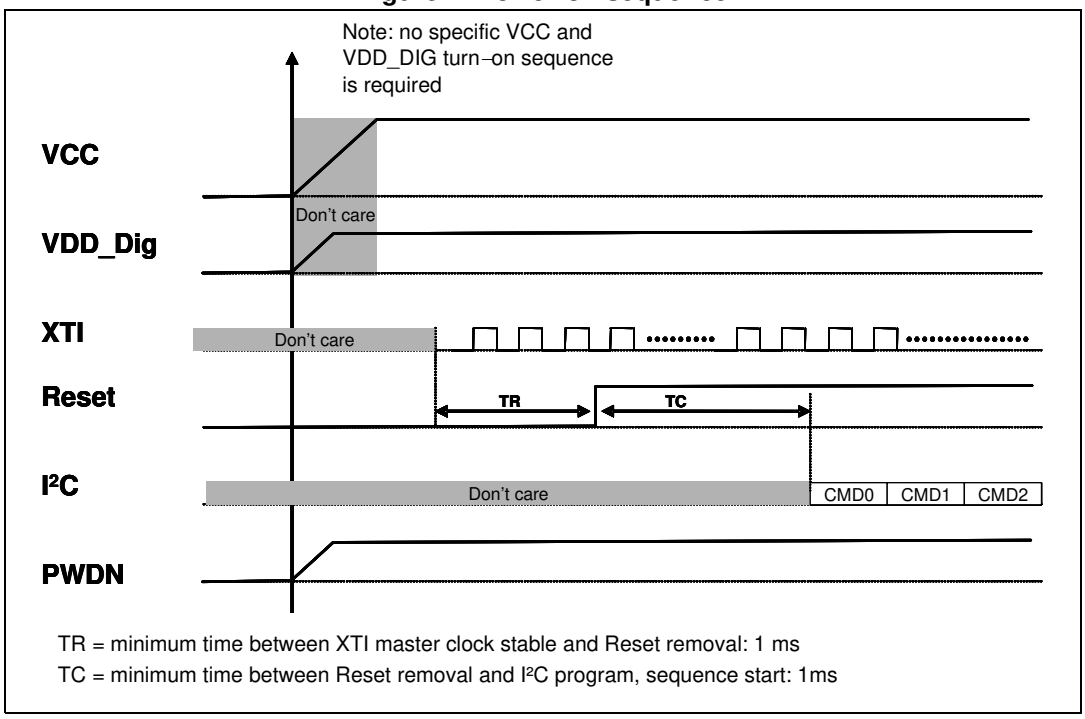
1. Limit the current if overcurrent warning detect adjustment bypass is enabled (register bit CONFC.OCRB *on page 28*). When disabled refer to I_{SCP}.

Figure 3. Test circuit



3.6 Power on/off sequence

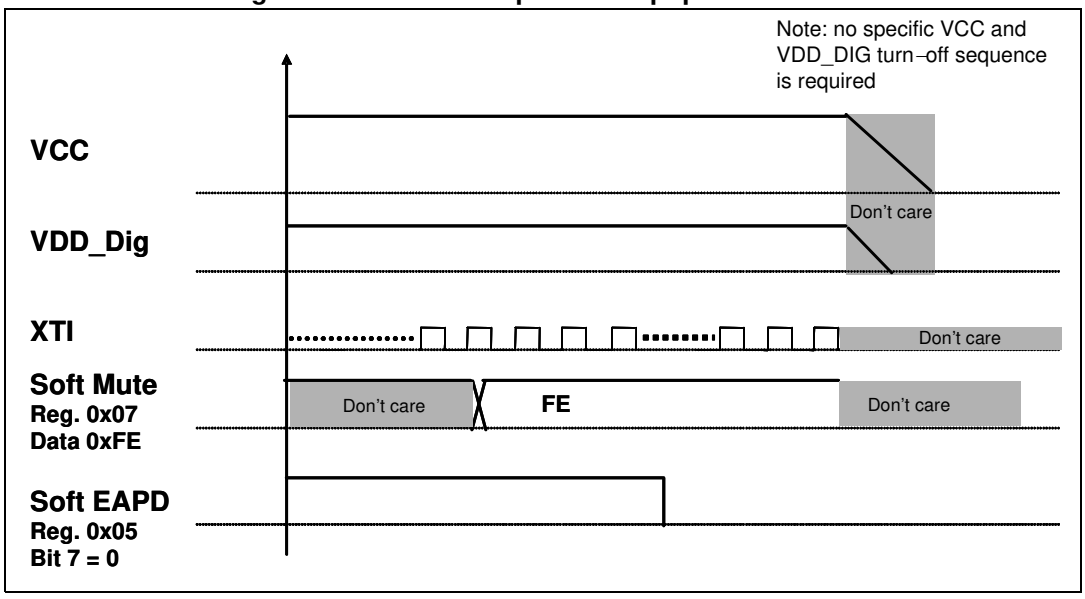
Figure 4. Power-on sequence



Note: The definition of a stable clock is when f_{max} - f_{min} < 1 MHz.

Section : Serial data interface on page 25 gives information on setting up the I²SI²S interface.

Figure 5. Power-off sequence for pop-free turn-off



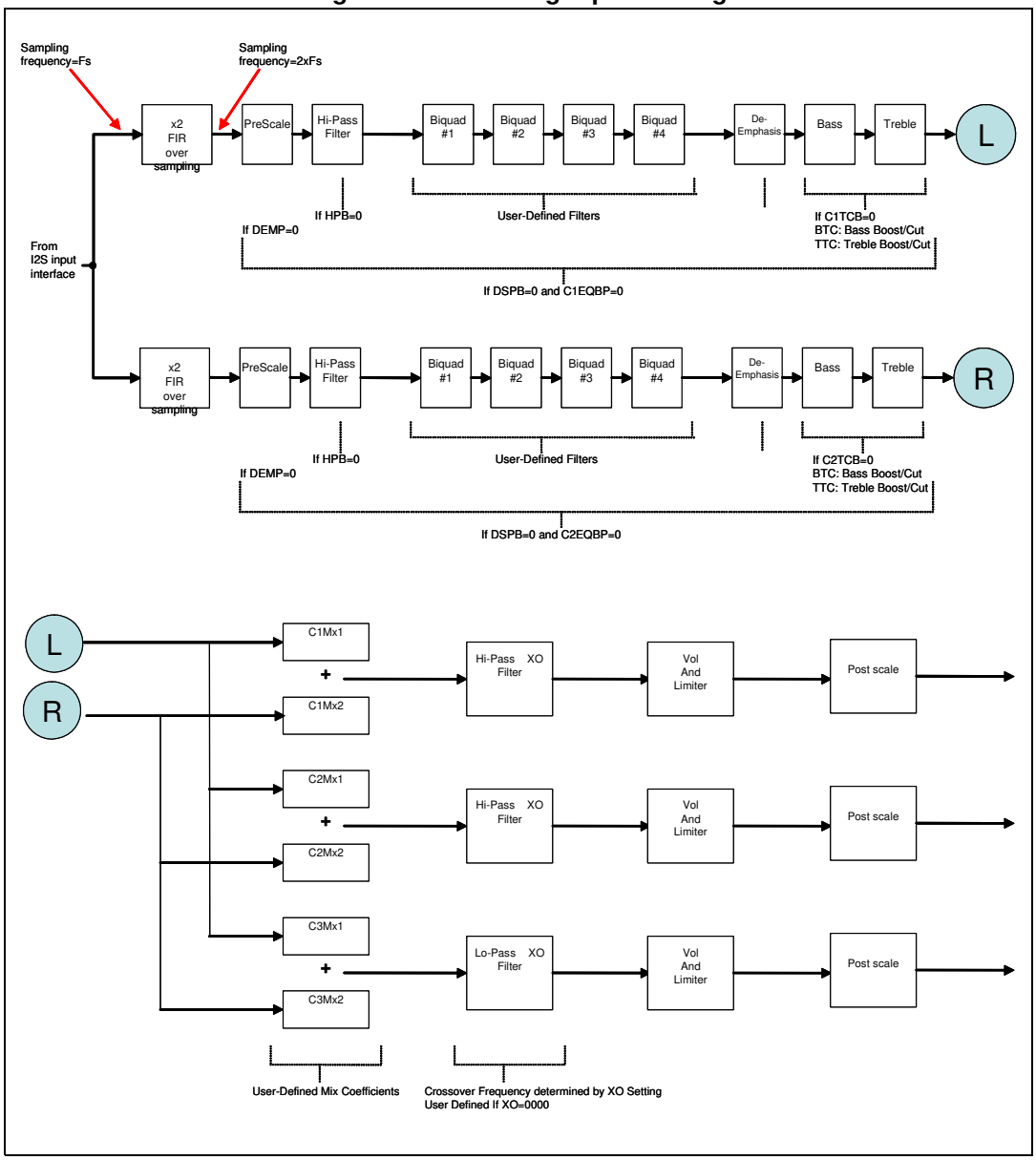
4 Processing data paths

Figure 6 below shows the data processing paths inside STA559BW. The whole processing chain can be considered as two consecutive sections. In the first one, dual-channel processing is implemented and in the second section each channel is fed into the post mixing block, either to generate a third channel (typically used in 2.1 output configuration and with crossover filters enabled) or to have the channels processed by the dual-band DRC block (2.0 output configuration with crossover filters used to define the cut-off frequency of the two bands).

The first section contains a 2x oversampling FIR filter providing 2 * f_S audio processing and a selectable high-pass filter to remove the DC level (enabled if HPB = 0).

If the coefficient sets for the two channels are linked (BQL = 1) it is possible to use the de-emphasis, bass and treble filters in a user defined configuration (provided the relevant BQx bits are set). In this case both channels use the same processing coefficients and can have up to seven filters each. If BQL = 0 the BQx bits are ignored and the fifth, sixth and seventh filters are configured as de-emphasis, bass and treble controls, respectively.

Figure 6. Left and right processing



5 I²C bus specification

The STA559BW supports the I²C protocol via the input ports SCL and SDA_IN (master to slave) and the output port SDA_OUT (slave to master). This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA559BW is always a slave device in all of its communications. It supports up to 400 kb/s (fast-mode bit rate).

For correct operation of the I²C interface ensure that the master clock generated by the PLL has a frequency at least 10 times higher than the frequency of the applied SCL clock.

5.1 Communication protocol

5.1.1 Data transition or change

Data changes on the SDA line must only occur when the clock SCL is low. A SDA transition while the clock is high is used to identify a START or STOP condition.

5.1.2 Start condition

START is identified by a high to low transition of the data bus, SDA, while the clock, SCL, is stable in the high state. A START condition must precede any command for data transfer.

5.1.3 Stop condition

STOP is identified by low to high transition of SDA while SCL is stable in the high state. A STOP condition terminates communication between STA559BW and the bus master.

5.1.4 Data input

During the data input the STA559BW samples the SDA signal on the rising edge of SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

5.2 Device addressing

To start communication between the master and the STA559BW, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode bit.

The seven most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA559BW the I²C interface has two device addresses depending on the SA pin configuration, 0x38 when SA = 0, and 0x3A when SA = 1.

The eighth bit (LSB) identifies a read or write operation (R/W); this is set to 1 for read and to 0 for write. After a START condition the STA559BW identifies the device address on the SDA bus and if a match is found, acknowledges the identification during the 9th bit time frame. The byte following the device identification is the address of a device register.

5.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA559BW acknowledges this and then waits for the byte of internal address. After receiving the internal byte address the STA559BW again responds with an acknowledgement.

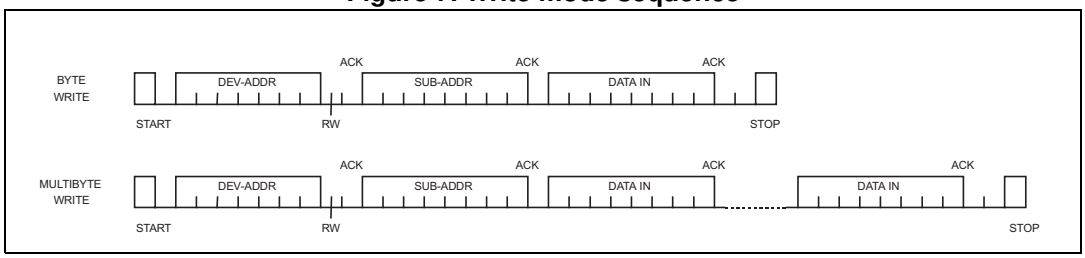
5.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by the STA559BW. The master then terminates the transfer by generating a STOP condition.

5.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 7. Write mode sequence



5.4 Read operation

5.4.1 Current address byte read

Following the START condition the master sends a device select code with the RW bit set to 1. The STA559BW acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

5.4.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA559BW. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

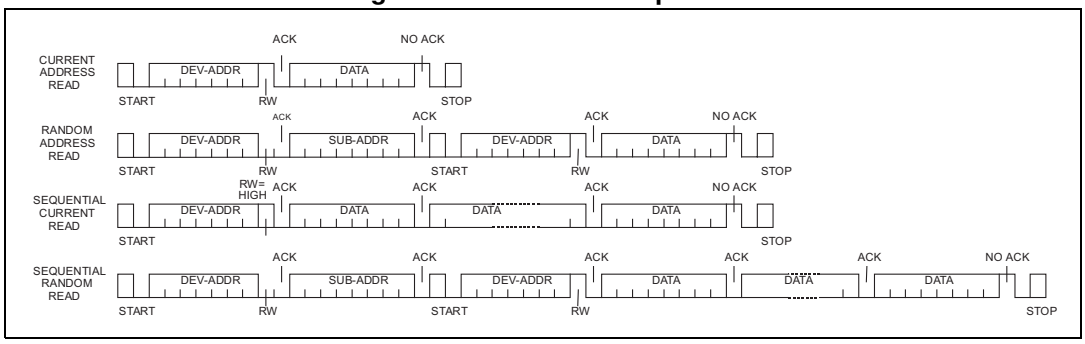
5.4.3 Random address byte read

Following the START condition the master sends a device select code with the RW bit set to 0. The STA559BW acknowledges this and then the master writes the internal address byte. After receiving, the internal byte address the STA559BW again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA559BW acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

5.4.4 Random address multi-byte read

The multi-byte read modes could start from any internal address. Sequential data bytes are read from sequential addresses within the STA559BW. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

Figure 8. Read mode sequence



6 Register description

Note: Addresses exceeding the maximum address number must not be written.

Table 8. Register summary

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	CONFA	FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0x01	CONFB	C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	CONFC	OCRB	Reserved	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x03	CONFD	SME	ZDE	DRC	BQL	PSL	DSPB	DEMP	HPB
0x04	CONFE	SVE	ZCE	DCCV	PWMS	AME	NSBW	MPC	MPCV
0x05	CONFF	EAPD	PWDN	ECLE	LDTE	BCLE	IDE	OCFG1	OCFG0
0x06	MUTELOC	LOC1	LOC0	Reserved	Reserved	C3M	C2M	C1M	Reserved
0x07	MVOL	MVOL[7:0]							
0x08	C1VOL	C1VOL[7:0]							
0x09	C2VOL	C2VOL[7:0]							
0x0A	C3VOL	C3VOL[7:0]							
0x0B	AUTO1	Reserved	Reserved	AMGC[1:0]		Reserved	Reserved	Reserved	Reserved
0x0C	AUTO2	XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0x0D	AUTO3	Reserved							
0x0E	C1CFG	C1OM1	C1OM0	C1LS1	C1LS0	C1BO	C1VBP	C1EQBP	C1TCB
0x0F	C2CFG	C2OM1	C2OM0	C2LS1	C2LS0	C2BO	C2VBP	C2EQBP	C2TCB
0x10	C3CFG	C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VBP	Reserved	Reserved
0x11	TONE	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0x12	L1AR	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x13	L1ATRT	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0x14	L2AR	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0x15	L2ATRT	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0x16	CFADDR	Reserved	Reserved	CFA[5:0]					
0x17	B1CF1	C1B[23:16]							
0x18	B1CF2	C1B[15:8]							
0x19	B1CF3	C1B[7:0]							
0x1A	B2CF1	C2B[23:16]							
0x1B	B2CF2	C2B[15:8]							
0x1C	B2CF3	C2B[7:0]							
0x1D	A1CF1	C3B[23:16]							
0x1E	A1CF2	C3B[15:8]							

Table 8. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x1F	A1CF3	C3B[7:0]							
0x20	A2CF1	C4B[23:16]							
0x21	A2CF2	C4B[15:8]							
0x22	A2CF3	C4B[7:0]							
0x23	B0CF1	C5B[23:16]							
0x24	B0CF2	C5B[15:8]							
0x25	B0CF3	C5B[7:0]							
0x26	CFUD	Reserved				RA	R1	WA	W1
0x27	MPCC1	MPCC[15:8]							
0x28	MPCC2	MPCC[7:0]							
0x29	DCC1	DCC[15:8]							
0x2A	DCC2	DCC[7:0]							
0x2B	FDRC1	FDRC[15:8]							
0x2C	FDRC2	FDRC[7:0]							
0x2D	STATUS	PLLUL	FAULT	UVFAULT	Reserved	OCFAULT	OCWARN	TFAULT	TWARN

6.1 Configuration registers (addr 0x00 to 0x05)

6.1.1 Configuration register A (addr 0x00)

D7	D6	D5	D4	D3	D2	D1	D0
FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0	1	1	0	0	0	1	1

Master clock select

Table 9. Master clock select

Bit	R/W	RST	Name	Description
0	R/W	1	MCS0	Selects the ratio between the input I²S sample frequency and the input clock.
1	R/W	1	MCS1	
2	R/W	0	MCS2	

The STA559BW supports sample rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz. Therefore the internal clock is:

- 32.768 MHz for 32 kHz
- 45.1584 MHz for 44.1 kHz, 88.2 kHz, and 176.4 kHz
- 49.152 MHz for 48 kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency (f_s).

The relationship between the input clock and the input sample rate is determined by both the MCSx and the IR (input rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IR bit determines the oversampling ratio used internally.

Table 10. Input sampling rates

Input sample rate *fs* (kHz)	IR	MCS[2:0]					
		101	100	011	010	001	000
32, 44.1, 48	00	576 * fs	128 * fs	256 * fs	384 * fs	512 * fs	768 * fs
88.2, 96	01	NA	64 * fs	128 * fs	192 * fs	256 * fs	384 * fs
176.4, 192	1X	NA	32 * fs	64 * fs	96 * fs	128 * fs	192 * fs

Interpolation ratio select

Table 11. Internal interpolation ratio

Bit	R/W	RST	Name	Description
4:3	R/W	00	IR [1:0]	Selects internal interpolation ratio based on input I²S sample frequency

The STA559BW has variable interpolation (oversampling) settings such that internal processing and FFX output rates remain consistent. The first processing block interpolates by either 2-times or 1-time (pass-through) or provides a 2-times downsample. The oversampling ratio of this interpolation is determined by the IR bits.

Table 12. IR bit settings as a function of input sample rate

Input sample rate fs (kHz)	IR	1st stage interpolation ratio
32	00	2-times oversampling
44.1	00	2-times oversampling
48	00	2-times oversampling
88.2	01	Pass-through
96	01	Pass-through
176.4	10	2-times downsampling
192	10	2-times downsampling

Thermal warning recovery bypass

Table 13. Thermal warning recovery bypass

Bit	R/W	RST	Name	Description
5	R/W	1	TWRB	0: thermal warning recovery enabled 1: thermal warning recovery disabled

This bit sets the behavior of the IC after a thermal warning disappears. If TWRB is enabled the device automatically restores the normal gain and output limiting is no longer active. If it is disabled the device keeps the output limit active until a reset is asserted or until TWRB set to 0. This bit works in conjunction with TWAB

Thermal warning adjustment bypass

Table 14. Thermal warning adjustment bypass

Bit	R/W	RST	Name	Description
6	R/W	1	TWAB	0: thermal warning adjustment enabled 1: thermal warning adjustment disabled

Bit TWAB enables automatic output limiting when a power stage thermal warning condition persists for longer than 400ms. When the feature is active (TWAB = 0) the desired output limiting, set through bit TWOCL (-3 dB by default) at address 0x37 in the RAM coefficients bank, is applied. The way the limiting acts after the warning condition disappears is controlled by bit TWRB.

Fault detect recovery bypass

Table 15. Fault detect recovery bypass

Bit	R/W	RST	Name	Description
7	R/W	0	FDRB	0: fault detect recovery enabled 1: fault detect recovery disabled

The on-chip power block provides feedback to the digital controller which is used to indicate a fault condition (either overcurrent or thermal). When fault is asserted the power control block attempts a recovery from the fault by asserting the 3-state output, holding it for period of time in the range of 0.1 ms to 1 second, as defined by the fault-detect recovery constant register (FDRC registers 0x2B-0x2C), then toggling it back to normal condition. This sequence is repeated as long as the fault indication exists. This feature is enabled by default but can be bypassed by setting the FDRB control bit to 1. The fault condition is also asserted by a low-state pulse of the normally high INT_LINE output pin.

6.1.2 Configuration register B (addr 0x01)

D7	D6	D5	D4	D3	D2	D1	D0
C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
1	0	0	0	0	0	0	0

Serial audio input interface format

Table 16. Serial audio input interface

Bit	R/W	RST	Name	Description
0	R/W	0	SAI0	Determines the interface format of the input serial digital audio interface.
1	R/W	0	SAI1	
2	R/W	0	SAI2	
3	R/W	0	SAI3	

Serial data interface

The STA559BW audio serial input interfaces with standard digital audio components and accepts a number of serial data formats. STA559BW always acts as slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using three inputs: left/right clock LRCKI, serial clock BICKI, and serial data SDI.

Bits SAI and bit SAIFB are used to specify the serial data format. The default serial data format is I²S, MSB first. Available formats are shown in the tables and figure that follow.

Serial data first bit

Table 17. Serial data first bit

SAIFB	Format
0	MSB-first
1	LSB-first

Table 18. Support serial audio input formats for MSB-first

BICKI	SAI [3:0]	SAIFB	Interface format
32 * fs	0000	0	I²S 15-bit data
	0001	0	Left/right-justified 16-bit data
48 * fs	0000	0	I²S 16 to 23-bit data
	0001	0	Left-justified 16 to 24-bit data
	0010	0	Right-justified 24-bit data
	0110	0	Right-justified 20-bit data
	1010	0	Right-justified 18-bit data
	1110	0	Right-justified 16-bit data
64 * fs	0000	0	I²S 16 to 24-bit data
	0001	0	Left-justified 16 to 24-bit data
	0010	0	Right-justified 24-bit data
	0110	0	Right-justified 20-bit data
	1010	0	Right-justified 18-bit data
	1110	0	Right-justified 16-bit data