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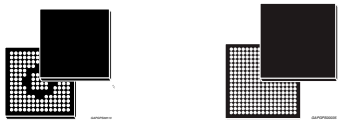
STA680

Automotive HD Radio™ baseband receiver

Datasheet - production data



LFBGA168 TFBGA289

Features

- AEC-Q100 qualified
- IBOC (in-band on-channel) digital audio broadcast signal decoding for AM/FM hybrid and all-digital modes
- Dual-channel HD 1.5 for background scanning and data services
- HD codec (HDC) audio decompression
- Metadata support for HD Radio reception
- MPS (main program service), SPS (supplemental program service) and PAD (program associated data) data decoding
- Advanced HD Radio feature support:
  - Apple ID3 tag
  - Multicasting
  - Electronic program guide (EPG)
  - Real-time traffic
- Automatic Audio Alignment (AAA) algorithm support
- Variable input base-band data-rate I2S-like interface supporting 650, 675, 744.1875, 912 kS/s data rates
- Secondary RF base-band interface for dual tuner applications
- Glueless interface to Synchronous SDRAM addressing up to 512 Mbit of SDRAM in x16 configuration
- Optional Serial Flash memory SPI interface for application code storage
- IIS serial audio interface with programmable sample rate converter
- Primary and secondary serial interfaces for host micro communication based on industry standard IIC and SPI
- Several General purpose IOs
- One Internal clock oscillator and two internal PLLs
- External clock input
- 1.2 V core supply; 3.3 V I/O supply

Description

The STA680 is an HD-radio base-band processor for car-radio applications. The STA680 functionality includes audio decompression and data processing, while multiple interfaces ensure flexible integration into the system.

The STA680 takes full advantage of HD 1.5 Radio benefits including CD-like audio quality from HD Radio FM broadcasts and FM-like audio quality using HD Radio AM, while program associated data or traffic information is received from the second channel.

STA680 supports FM/AM analog/digital AAA algorithm by mean of specific FW.

Table 1. Device summary

Order code	Package[1]	Packing
STA680	LFBGA 168 balls (12x12x1.4 mm)	Tray
STA680TR		Tape & Reel
STA680D	TFBGA 289 balls (15x15x1.2 mm)	Tray
STA680DTR		Tape & Reel

1. ECOPACK® compliant.

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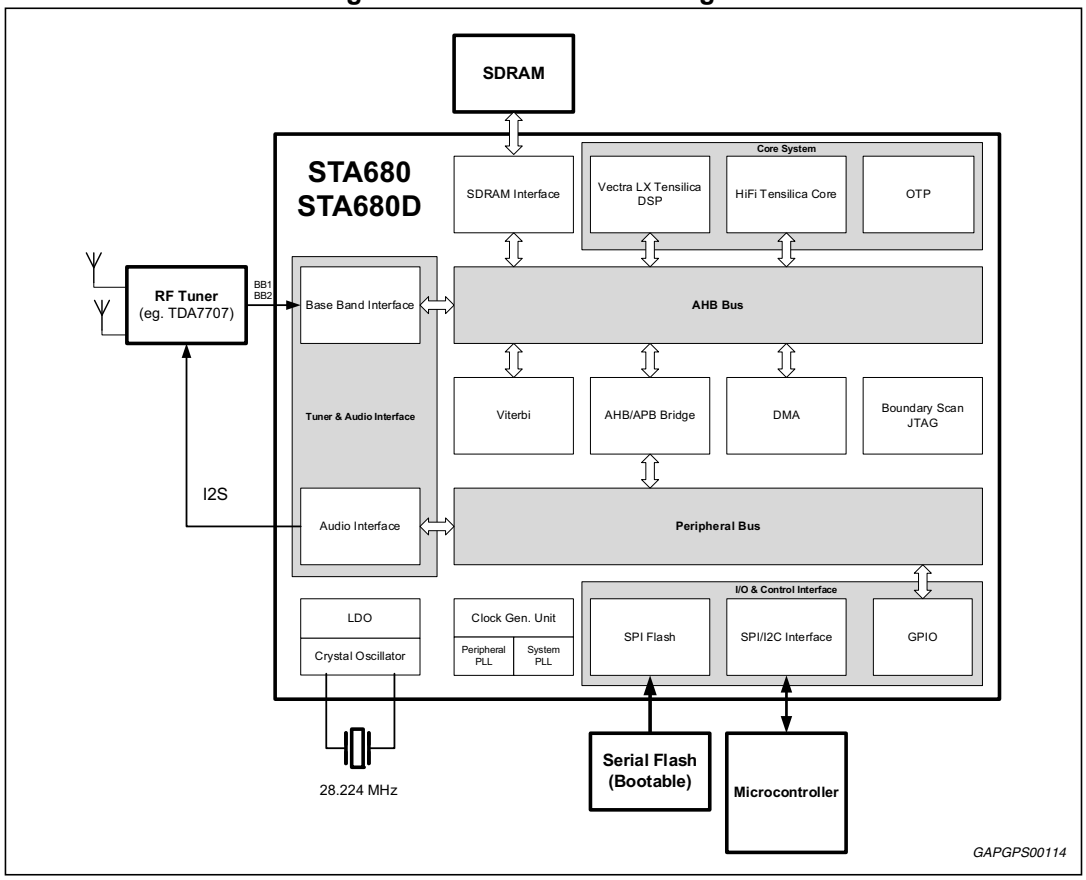
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Functional block diagram



1.2 Ball-out description

The STA680 is available in two different packages. It comes in a 12x12 mm LFBGA with 168 balls with 0.8 mm pitch and in 15x15 mm TFBGA with 289 balls with 0.8 mm pitch. TFBGA289 package option offers ball-to-ball compatibility with STA660 DAB/DRM digital decoder.

1.2.1 LFBGA description

Figure 2 presents the ball-out of the STA680 for the LFBGA package option. Different colors have been used for I/O signals from different interfaces according to *Table 2* reported in *Section 1.2.3*.

Figure 2. LFBGA ball-out (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		GPIO6	BB2_BCK	BB2_I	GND_GEN_IO	IIC1_SDA	SPI1_MISO	SPI1_SCK	RESET_N	TXD_GPIO2	RTS_GPIO0	VDD_GEN_IO	TESTMODE	
B	GPIO5	BB1_Q	BLEND	BB2_WS	GND_GEN_IO	BB2_Q	IIC1_SCL	SPI1_MOSI	SPI1_SS0_N	RXD_GPIO3	CTS_GPIO1	VDD_GEN_IO	SDR_A3	TRST_N
C	BB1_WS	BB1_I	ADAT2	IIC2_SDA	GPIO7	IIC2_SCL	IIC1_DA	SPI3_MOSI	SPI3_MISO	SPI3_SCK	TDI	TCK	SDR_A1	SDR_A2
D	VDD_GEN_IO	VDD_GEN_IO	BB1_BCK	IIC2_DA	VDD	VDD			SPI3_SS_N	GPIO4	TDO	TMS	SDR_A10	SDR_A0
E	AUDIO_IN_ ABCK	SPDIF	ADAT3	VDD_PLL_DIG							VDD	MODEOP_FSH	SDR_BA0	SDR_BA1
F	AUDIO_IN_ ADAT	AUDIO_IN_ AWS	GND_PLL_ DIG	GND_PLL_ DIG		GND	GND	GND	GND		VDD	MODEOP_GEN	SDR_RAS_N	SDR_CS_N
G	AWS	ADAT	DAC256X			GND	GND	GND	GND			SDR_CAS_N	SDR_WE_N	VDD_RAM_IO
H	GND_GEN_IO	GND_GEN_IO	ABCK			GND	GND	GND	GND			SDR_A4	SDR_A5	GND_RAM_IO
J	VDD_OSC	GND_OSC	GND_PLL1_ ANA	GND_PLL0_ ANA		GND	GND	GND	GND		VDD	VDD	SDR_A7	SDR_A6
K	OSC_OUT	CLK_IN	VDD	VDD_REG3V3							VDD	VDD	SDR_A9	SDR_A8
L	OSC_IN	GND_OSC	VDD	VDD_REG3V3	VDD_FSH_IO	GND_FSH_IO			VDD_RAM_IO _1V8	GND_RAM_IO _1V8	GND_RAM_IO	GND_RAM_IO	SDR_A12	SDR_A11
M	VDD_PLL1_ ANA	VDD_PLL0_ ANA	SPI2_SS1_N	SPI2_SS2_N	SPI2_SS3_N	RFU	SDR_D13	SDR_D10	VDD_RAM_IO	VDD_RAM_IO	GND_RAM_IO	GND_RAM_IO	SDR_DQM1	SDR_CKE
N	VDD_REG1V8	VDD_REG1V8	SPI2_MOSI	SPI2_SCK	SDR_CLK_ RAM3V3	SDR_D15	SDR_D12	SDR_D9	SDR_D0	SDR_D2	SDR_D4	SDR_D6	SDR_DQM0	
P			SPI2_SS0_N	SPI2_MISO	SDR_FEED_ CLK	SDR_D14	SDR_D11	SDR_D8	SDR_D1	SDR_D3	SDR_D5	SDR_D7		

Color legend:

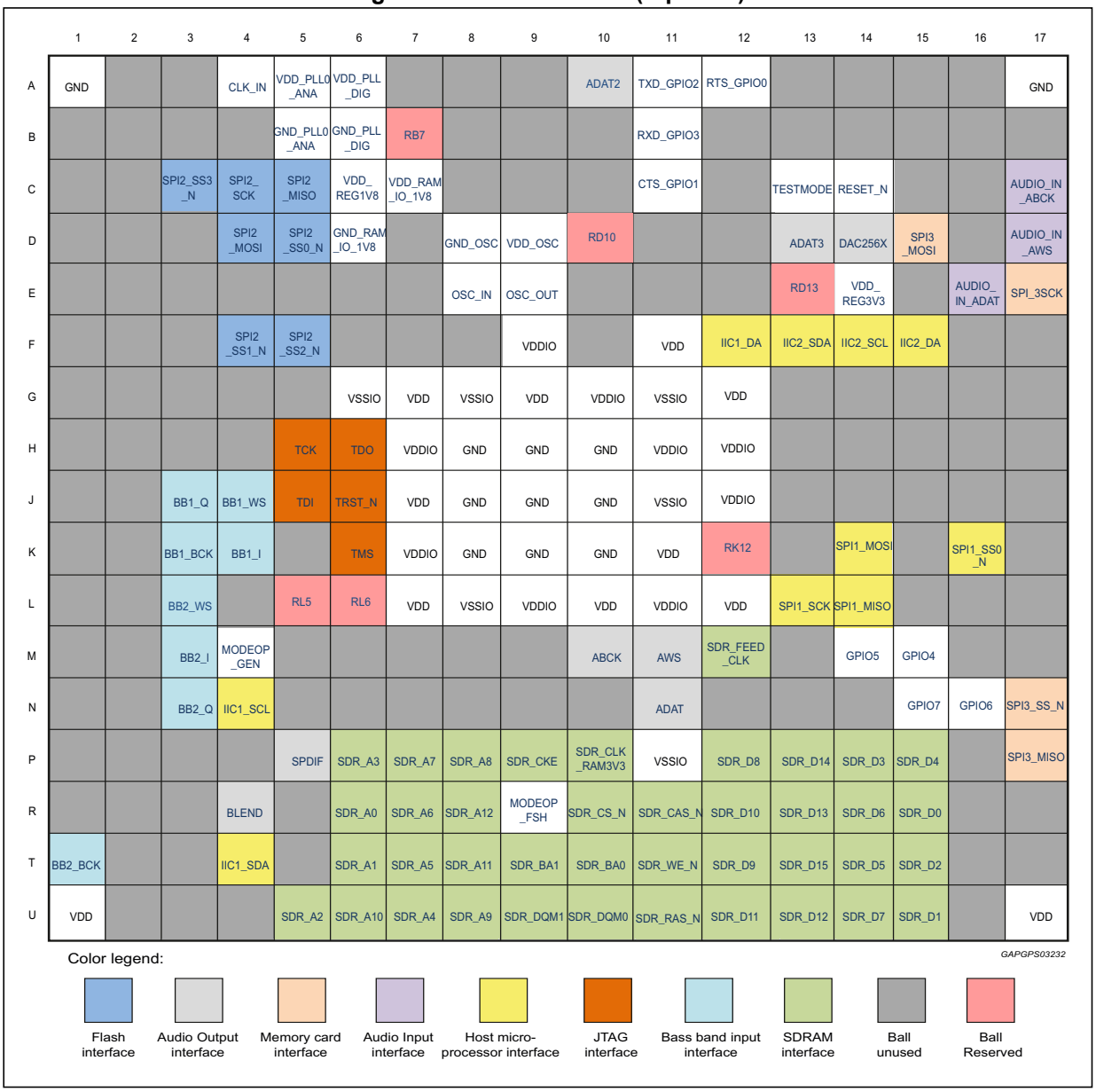
Ball unused | Ball not present | JTAG interface | UART GPIO interface | Host micro-processor interface | Memory card interface | Flash interface | Base band input interface | Audio Input interface | Audio Output interface | SDRAM interface

GAPGPS00116

1.2.2 TFBGA description

Figure 3 presents the ball-out of the STA680 for the TFBGA package option. Different colors have been used for I/O signals from different interfaces according to *Table 2* reported in *Section 1.2.3*.

Figure 3. TFBGA ball-out (top view)



1.2.3 Ball-out list

The *Table 2* describes the primary function and behavior of the STA680 pins.

Table 2. Ball-out description

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
Test							
A13	C13	TESTMODE	I	Pull-down	3.3 V	Generic IO supply	Factory test mode enable
Standard 1149.1 JTAG interface							
B14	J6	TRST_N	I	Pull-up	3.3 V	Generic IO supply	JTAG active-low test reset
C12	H5	TCK	I	Pull-down	3.3 V	Generic IO supply	JTAG test clock
D12	K6	TMS	I	Pull-up	3.3 V	Generic IO supply	JTAG test mode state
C11	J5	TDI	I	Pull-up	3.3 V	Generic IO supply	JTAG test data in
D11	H6	TDO	O	-	3.3 V	Generic IO supply	JTAG test data out
GPIO & UART interfaces							
A11	A12	RTS_GPIO0	I/O	Pull-up	3.3 V	Generic IO supply	UART ready to send / GPIO bit 0
B11	C11	CTS_GPIO1	I/O	Pull-up	3.3 V	Generic IO supply	UART clear to send / GPIO bit 1
A10	A11	TXD_GPIO2	I/O	Pull-up	3.3 V	Generic IO supply	UART transmit data / GPIO bit 2
B10	B11	RXD_GPIO3	I/O	Pull-up	3.3 V	Generic IO supply	UART receive data / GPIO bit 3
D10	M15	GPIO4	I/O	Pull-up	3.3 V	Generic IO supply	GPIO bit 4
B1	M14	GPIO5	I/O	Pull-up	3.3 V	Generic IO supply	GPIO bit 5
A2	N16	GPIO6	I/O	Pull-up	3.3 V	Generic IO supply	GPIO bit 6

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
C5	N15	GPIO7	I/O	Pull-up	3.3 V	Generic IO supply	GPIO bit 7
Reset							
A9	C14	RESET_N	I	Pull-up	3.3 V	Generic IO supply	Device active-low reset
Host microprocessor interfaces							
B9	K16	SPI1_SS0_N	I	Pull-up	3.3 V	Generic IO supply	SPI interface 1 active-low slave select
A8	L13	SPI1_SCK	I	Pull-up	3.3 V	Generic IO supply	SPI interface 1 serial clock
B8	K14	SPI1_MOSI	I	Pull-up	3.3 V	Generic IO supply	SPI interface 1 serial data master out/slave in
A7	L14	SPI1_MISO	O	Pull-up	3.3 V	Generic IO supply	SPI interface 1 serial data master in/slave out
B7	N4	IIC1_SCL	I/O	Pull-up	3.3 V	Generic IO supply	IIC interface 1 serial clock line
A6	T4	IIC1_SDA	I/O	Pull-up	3.3 V	Generic IO supply	IIC interface 1 serial data line
C7	F12	IIC1_DA	I/O	Pull-up	3.3 V	Generic IO supply	IIC interface 1 data acknowledged
C6	F14	IIC2_SCL	I/O	Pull-up	3.3 V	Generic IO supply	Reserved
C4	F13	IIC2_SDA	I/O	Pull-up	3.3 V	Generic IO supply	Reserved
D4	F15	IIC2_DA	I/O	Pull-up	3.3 V	Generic IO supply	Reserved

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
IIS tuner interfaces							
C2	K4	BB1_I	I	Pull-down	3.3 V	Generic IO supply	Primary baseband interface serial I data or Primary baseband interface I/Q multiplexed data
B2	J3	BB1_Q	I	Pull-down	3.3 V	Generic IO supply	Primary baseband interface serial Q data (not used in case of Primary data multiplexed on BB1_I)
C1	J4	BB1_WS	I	Pull-down	3.3 V	Generic IO supply	Primary baseband interface word strobe
D3	K3	BB1_BCK	I	Pull-down	3.3 V	Generic IO supply	Primary baseband interface bit clock
A4	M3	BB2_I	I	Pull-down	3.3 V	Generic IO supply	Secondary baseband interface serial I data or Secondary baseband interface I/Q multiplexed data
B6	N3	BB2_Q	I	Pull-down	3.3 V	Generic IO supply	Secondary baseband interface serial Q data (not used in case of Secondary data multiplexed on BB2_I)
B4	L3	BB2_WS	I	Pull-down	3.3 V	Generic IO supply	Secondary baseband interface word strobe
A3	T1	BB2_BCK	I	Pull-down	3.3 V	Generic IO supply	Secondary baseband interface bit clock
IIS audio input interface							
F2	D17	AUDIO_IN_AWS	I/O	Pull-up	3.3 V	Generic IO supply	Digital audio input word strobe
E1	C17	AUDIO_IN_ ABCK	I/O	Pull-up	3.3 V	Generic IO supply	Digital audio input clock
F1	E16	AUDIO_IN_ ADAT	I	Pull-down	3.3 V	Generic IO supply	Digital audio input serial data
Audio output interfaces							
G1	M11	AWS	I/O	Pull-up	3.3 V	Generic IO supply	Digital audio output word strobe

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
H3	M10	ABCK	I/O	Pull-up	3.3 V	Generic IO supply	Digital audio output clock
G2	N11	ADAT	O	-	3.3 V	Generic IO supply	Digital audio output serial data
C3	A10	ADAT2	O	-	3.3 V	Generic IO supply	Reserved
E3	D13	ADAT3	O	-	3.3 V	Generic IO supply	Reserved. Reference clock configuration pin, works in input mode till RESET_N release
E2	P5	SPDIF	O	-	3.3 V	Generic IO supply	Reserved
B3	R4	BLEND	O	-	3.3 V	Generic IO supply	Digital audio blend output. Reference clock configuration pin, works in input mode till RESET_N release
G3	D14	DAC256X	O	-	3.3 V	Generic IO supply	Digital audio output oversampling clock. Reference clock configuration pin, works in input mode till RESET_N release
Clock & oscillator							
K2	A4	CLK_IN	I	-	3.3 V	Generic IO supply	Reference digital clock
L1	E8	OSC_IN	ana	-	1.8 V	Osc supply	28,224MHz crystal in or digital clock input
K1	E9	OSC_OUT	ana	-	1.8 V	Osc supply	Crystal output
SPI Flash interface							
P4	C5	SPI2_MISO	I	Pull-up	3.3 V	Flash IO supply	SPI interface 2 serial data master in/slave out
N3	D4	SPI2_MOSI	O	Pull-up	3.3 V	Flash IO supply	SPI interface 2 serial data master out/slave in
P3	D5	SPI2_SS0_N	O	Pull-up	3.3 V	Flash IO supply	SPI interface 2 active-low slave select 0

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
M3	F4	SPI2_SS1_N	O	Pull-up	3.3 V	Flash IO supply	Reserved
M4	F5	SPI2_SS2_N	O	Pull-up	3.3 V	Flash IO supply	Reserved
M5	C3	SPI2_SS3_N	O	Pull-up	3.3 V	Flash IO supply	Reserved
N4	C4	SPI2_SCK	O	Pull-up	3.3 V	Flash IO supply	SPI interface 2 serial clock
SPI SD/MMC interface							
C9	P17	SPI3_MISO	I	Pull-up	3.3 V	Generic IO supply	Reserved
C8	D15	SPI3_MOSI	O	Pull-up	3.3 V	Generic IO supply	Reserved
D9	N17	SPI3_SS_N	O	Pull-up	3.3 V	Generic IO supply	Reserved
C10	E17	SPI3_SCK	O	Pull-up	3.3 V	Generic IO supply	Reserved
SDRAM interface							
P5	M12	SDR_FEED_ CLK	I	-	3.3 V	SDRAM IO supply	Feedback clock from SDRAM interface
N5	P10	SDR_CLK_ RAM3V3	O	-	3.3 V	SDRAM IO supply	Clock to SDRAM for 3.3 V interface
N9	R15	SDR_D0	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 0
P9	U15	SDR_D1	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 1
N10	T15	SDR_D2	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 2
P10	P14	SDR_D3	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 3

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
N11	P15	SDR_D4	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 4
P11	T14	SDR_D5	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 5
N12	R14	SDR_D6	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 6
P12	U14	SDR_D7	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 7
P8	P12	SDR_D8	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 8
N8	T12	SDR_D9	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 9
M8	R12	SDR_D10	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 10
P7	U12	SDR_D11	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 11
N7	U13	SDR_D12	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 12
M7	R13	SDR_D13	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 13
P6	P13	SDR_D14	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 14
N6	T13	SDR_D15	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 15
N13	U10	SDR_DQM0	O	-	3.3 V	SDRAM IO supply	Low-byte data input/output mask
M13	U9	SDR_DQM1	O	-	3.3 V	SDRAM IO supply	High-byte data input/output mask
G13	T11	SDR_WE_N	O	-	3.3 V	SDRAM IO supply	Active-low write enable

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
G12	R11	SDR_CAS_N	O	-	3.3 V	SDRAM IO supply	Active-low column address strobe
F13	U11	SDR_RAS_N	O	-	3.3 V	SDRAM IO supply	Active-low row address strobe
M14	P9	SDR_CKE	O	-	3.3 V	SDRAM IO supply	Clock enable
F14	R10	SDR_CS_N	O	-	3.3 V	SDRAM IO supply	Active-low chip select
E13	T10	SDR_BA0	O	-	3.3 V	SDRAM IO supply	Bank select address 0
E14	T9	SDR_BA1	O	-	3.3 V	SDRAM IO supply	Bank select address 1
D14	R6	SDR_A0	O	-	3.3 V	SDRAM IO supply	Address bit 0 to SDRAM
C13	T6	SDR_A1	O	-	3.3 V	SDRAM IO supply	Address bit 1 to SDRAM
C14	U5	SDR_A2	O	-	3.3 V	SDRAM IO supply	Address bit 2 to SDRAM
B13	P6	SDR_A3	O	-	3.3 V	SDRAM IO supply	Address bit 3 to SDRAM
H12	U7	SDR_A4	O	-	3.3 V	SDRAM IO supply	Address bit 4 to SDRAM
H13	T7	SDR_A5	O	-	3.3 V	SDRAM IO supply	Address bit 5 to SDRAM
J14	R7	SDR_A6	O	-	3.3 V	SDRAM IO supply	Address bit 6 to SDRAM
J13	P7	SDR_A7	O	-	3.3 V	SDRAM IO supply	Address bit 7 to SDRAM
K14	P8	SDR_A8	O	-	3.3 V	SDRAM IO supply	Address bit 8 to SDRAM

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
K13	U8	SDR_A9	O	-	3.3 V	SDRAM IO supply	Address bit 10 to SDRAM
D13	U6	SDR_A10	O	-	3.3 V	SDRAM IO supply	Address bit 10 to SDRAM
L14	T8	SDR_A11	O	-	3.3 V	SDRAM IO supply	Address bit 11 to SDRAM
L13	R8	SDR_A12	O	-	3.3 V	SDRAM IO supply	Address bit 12 to SDRAM
Supplies							
F12	M4	MODEOP_GEN	I	Pull-up	3.3 V	SDRAM IO supply	Define the operating voltage of the "Generic I/O" supply group. Value is 3.3V.
E12	R9	MODEOP_FSH	I	Pull-up	3.3 V	SDRAM IO supply	Define the operating voltage of the "Generic I/O" supply group. Value is 3.3V.
D5, D6, E11, F11, J11, J12, K3, K11, K12, L3	F11, G7, G9, G12, J7, K11, L7,L10, L12, U1, U17	VDD	n/a	-	1.2 V	Core supply	Power supply for core logic
F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9	A1,A17, H8, H9, H10, J8, J9, J10, K8, K9, K10,	GND	n/a	-	-	Core supply	Ground for core logic
A5, B5, H1, H2	-	GND_GEN_IO	n/a	-	-	Generic IO supply	Generic I/Os ground
A12, B12, D1, D2	-	VDD_GEN_IO	n/a	-	3.3 V	Generic IO supply	Generic I/Os power supply
L6	-	GND_FSH_IO	n/a	-	-	Flash IO supply	Ground for Flash Interface I/Os
L5	-	VDD_FSH_IO	n/a	-	3.3 V	Flash IO supply	Power supply for Flash Inteface I/Os

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
H14, L11, L12, M11, M12	-	GND_RAM_IO	n/a	-	-	SDRAM IO supply	Ground for SDRAM Interface I/Os
G14, M9, M10	-	VDD_RAM_IO	n/a	-	3.3 V	SDRAM IO supply	Power supply for SDRAM Interface I/Os
-	F9, G10, H7, H11, K7, L9, L11, H12, J12	VDDIO	n/a	-	3.3 V	I/O supply	Generic I/Os power supply
-	G6, G8, G11, J11, L8, P11	VSSIO	n/a	-	-	I/O supply	Generic I/Os ground
F3, F4	B6	GND_PLL_DIG	n/a	-	-	PLL digital supply	Ground for PLL digital part
E4	A6	VDD_PLL_DIG	n/a	-	1.2 V	PLL digital supply	Power supply for PLL digital part
J4	B5	GND_PLL0_ ANA	n/a	-	-	PLL analog supply	Ground for PLL0 analog part
J3	-	GND_PLL1_ ANA	n/a	-	-	PLL analog supply	Ground for PLL1 analog part
M2	A5	VDD_PLL0_ ANA	n/a	-	1.8 V	PLL analog supply	Power supply for PLL0 analog part
M1	-	VDD_PLL1_ ANA	n/a	-	1.8 V	PLL analog supply	Power supply for PLL1 analog part
J2, L2	D8	GND_OSC	n/a	-	-	Osc supply	Ground for oscillator core
J1	D9	VDD_OSC	n/a	-	1.8 V	Osc supply	Power supply for oscillator core
K4, L4	E14	VDD_REG3V3	n/a	-	3.3 V	LDO supply	Voltage regulator input power supply @ 3.3 V
N1, N2	C6	VDD_REG1V8	n/a	-	1.8 V	LDO supply	Voltage regulator output power supply @ 1.8 V
L9	C7	VDD_RAM_IO _1V8	n/a	-	1.8 V	n/a	Reserved - connect to 1.8 V supply
L10	D6	GND_RAM_IO _1V8	n/a	-	-	n/a	Reserved - Connect to ground
Others							
M6	-	RFU	n/a	-	n/a	n/a	Reserved for future use - do not connect

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up /down(1)	Electrical	Supply group	Description
Reserved							
-	B7, D10, E13, K12, L5, L6	RB7, RD10, RE13, RK12, RL5, RL6	n/a	-	n/a	n/a	Reserved
Unused							
A1, A14, N14, P1, P2, P13, P14	A2, A3, A7, A8, A9, A13, A14, A15, A16, B1, B2, B3, B4, B8, B9, B10, B12, B13, B14, B15, B16, B17, C1, C2, C8, C9, C10, C12, C15, C16,D1, D2, D3, D7, D11, D12, D16,E1, E2, E3, E4, E5, E6, E7, E10, E11, E12, E15, F1, F2, F3, F6, F7, F8, F10, F16, F17, G1, G2, G3, G4, G5, G13, G14, G15, G16, G17, H1, H2, H3, H4, H13, H14, H15, H16, H17,J1, J2, J13, J14, J15, J16, J17, K1, K2, K5, K13, K15, K17, L1, L2, L4, L15, L16, L17, M1, M2, M5, M6, M7, M8, M9, M13, M16, M17, N1, N2, N5, N6, N7, N8, N9, N10, N12, N13, N14, P1, P2, P3, P4, P16, R1, R2, R3, R5, R16, R17, T2, T3, T5, T16, T17, U2, U3, U4, U16	Unused	n/a	-	n/a	n/a	Unused balls have to be left unconnected or connected to GND. Unused balls can be shorted together but they cannot be connected to any supply or other signal trace on the application PCB.

1. Each input pin has a pull-up/down resistor to its default value. Unless otherwise specified, signal balls not used in application can be left unconnected after verifying that the impedance value of the pull-up/down resistor (see *Table 20*) is sufficient to guarantee noise immunity in user application environment.

1.2.4 I/Os supply groups

The STA680 I/O signals can be grouped into three different supply domains, as shown in (see *Table 2*):

- Generic IO supply
- Flash IO supply
- SDRAM IO supply group

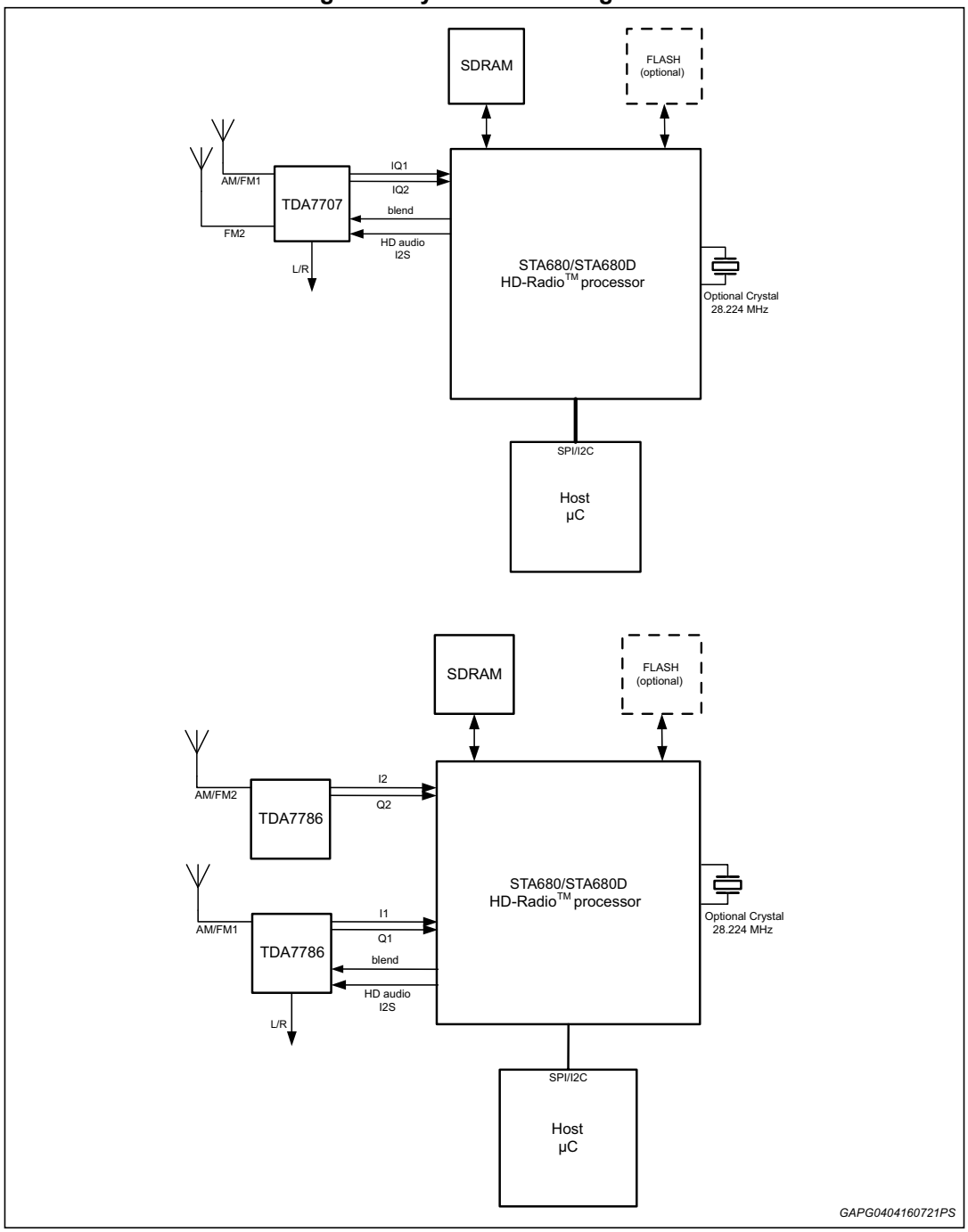
In the LFBGA and TFBGA packages the three supply groups operate at 3.3 V.

2 General description

The STA680 is a system-on-chip designed for demodulating and decoding HD Radio signals.

The STA680 is the base-band signal processor needed by an HD Radio receiver: it includes the OFDM demodulator, error correction, audio and data decoding of the digital channel.

Figure 4. System block diagrams



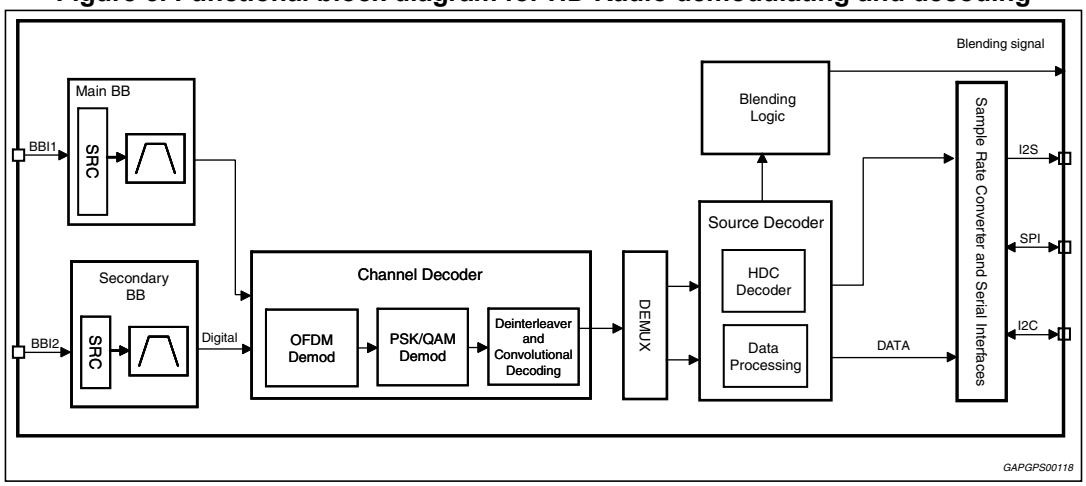
The architecture of STA680 consists of a mixed hardware/software implementation. Computation-intensive functional blocks are implemented using custom logic. Software implementation is more efficient for functional blocks where flexibility is needed.

2.1 Receiver system overview

Such flexibility enables the STA680 to support both the HD 1.0 single-channel, and HD 1.5 double-channel applications, as shown in *Figure 4*.
Figure 5 shows the internal simplified block diagram of the STA680.

The STA680 receives the digital base-band signal from the digital tuner (e.g. TDA7786 or TDA7707) and extracts the HD-encoded audio and data services as shown in *Figure 5*. STA680 is compatible with conventional base-band radio reception tuners (e.g. TDA7786 or TDA7707).

Figure 5. Functional block diagram for HD Radio demodulating and decoding



2.2 HD Radio processing

The STA680 HD Radio decoder performs the processing of the IBOC signal. The native internal processing data rate is 744.1875 kS/s for FM and 46.51171875 kS/s for AM.

The input I^2S base-band interface accepts several input sample rates thanks to the availability of a reconfigurable sample rate converter.The supported rates are: 650 kS/s, 675 kS/s, 744.1875 kS/s and 912 kS/s.

The STA680 is responsible for the detection, acquisition and demodulation of the IBOC signal. This processing is mainly performed inside the Vectra DSP core. The demodulated signal is then passed to the Hi-Fi processor for decoding and handling of data services. The digital 44.1 kHz decompressed audio is streamed out by means of the Digital Audio Interface.

The STA680 requires a 4Mwords x16bits external SDRAM (with up to 32Mword x16bits supported) for data storage in order to process the HD Radio stream

2.3 Dual channel HD 1.5 Radio processing

The STA680 is capable of simultaneously demodulating two different HD Radio streams. This feature enables the device to decode the main HD Radio audio stream in parallel with the data service broadcasted by a different radio channel (for instance this feature allows to continue receiving traffic information provided by one radio station while listening to music from a different station).

An example of implementation of the dual stream HD Radio processing is shown in *Figure 4*.

2.4 Overview of main functional blocks

2.4.1 Adjacent channel filter

This module performs digital filtering of the IBOC channel. It receives the complex base-band I/Q IBOC signal input from the tuner and pre-conditions the signal for subsequent modem processing.

2.4.2 HiFi2 core

The HiFi2 is a signal processing engine specifically designed to provide high quality 24-bit audio processing. The HiFi2 uses the Tensilica Xtensa LX engine with additional useful hardware capabilities such as:

- Specialized instructions for 24-bit Audio MAC & stream coding
- Dual MAC (each supports 24 x 24 and 32 x 16 bit format)
- Huffman Encode / Decode and truncate functions
- Two way Single-Instruction-Multiple-Data arithmetic and logic operations

2.4.3 Vectra core

The Vectra LX is an on-chip, powerful, 32-bit RISC engine optimized for DSP with VLIW capabilities. The Vectra LX includes eight MAC units, sixteen 160-bit vector operation registers, and a number of SIMD arithmetic instructions. Custom instructions in the Vectra are tailored to DSP applications such as filters and FFTs. The Vectra processor has been further configured with specific instructions for efficient performance on the HD Radio application.

2.4.4 DMA

A ten-channel DMA controller is attached to the AHB bus to allow the Vectra and HiFi2 processor cores to efficiently move large data-blocks.

2.4.5 Hardware accelerator (VITERBI)

The complex convolutional Viterbi hardware accelerator supports both K constants of 7 and 9, for IBOC digital FM and AM processing respectively.

3 Operation and general remarks

3.1 Clock schemes

The STA680 needs an external clock source to drive the internal Phase Locked Loops (PLLs) that generate the clocks needed by the DSP cores and their peripherals.

The STA680 accepts several external reference clock sources, as listed below:

- The reference clock can be supplied through the use of an external crystal or as a digital signal coming from an external IC.
- The reference clock can have different frequencies and different input pins can be used.

The selection of the clock input mode is performed during the power-on phase of the device by latching the value of the pins ADAT3, BLEND and DAC256X on the rising edge of the RESET_N signal (see *Section 3.2*); these values shall be selected according to *Table 3*.

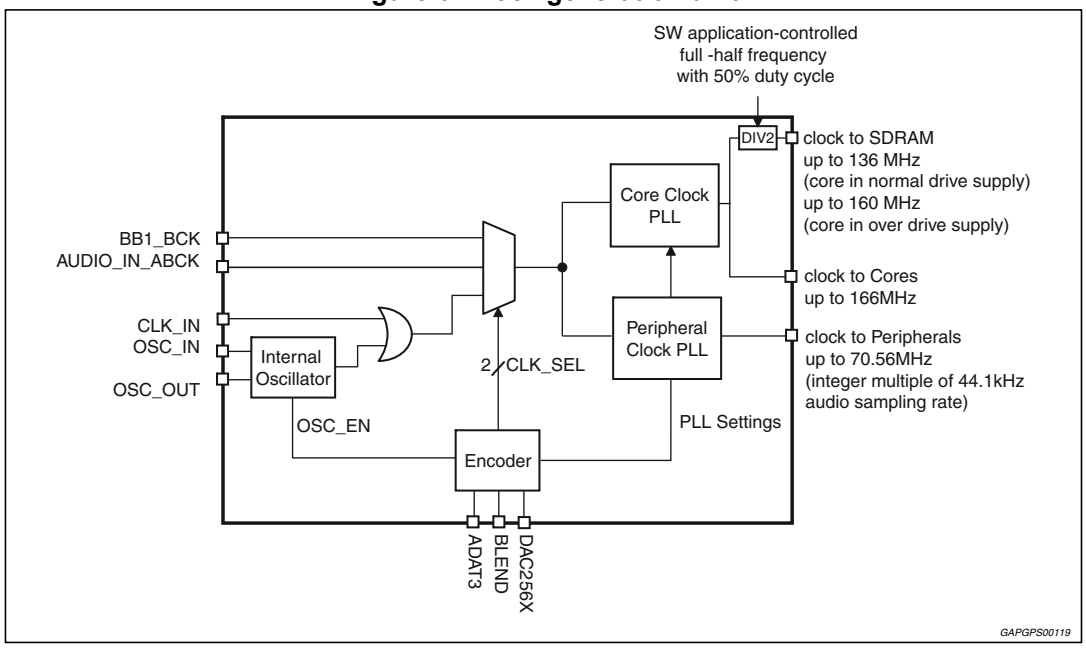
Table 3. Reference clock configuration

[ADAT3, BLEND, DAC256X]	Clock type	Input pin	Clock frequency (MHz)
[0,0,0] (1)	Crystal	OSC_IN	28.224
[0,0,1]	Digital	OSC_IN or CLK_IN (2)	23.3472
[0,1,0]	Digital	OSC_IN or CLK_IN (2)	36.48
[0,1,1]	Digital	OSC_IN or CLK_IN (2)	2.9184
[1,0,0]	Digital	BB1_BCK(3)	10.4
[1,0,1]	Digital	BB1_BCK(3)	10.8

1. Default setting.
2. When using OSC_IN pin to input the reference clock the CLK_IN pin must be connected to ground and vice versa.
3. When using BB1_BCK to input the reference clock it is suggested to connect the OSC_IN to ground and to tie the CLK_IN pin to high value (3.3 V).

Figure 6 shows a simplified version of the internal clock generation unit.

Figure 6. Clock generation unit



Clock generation unit

Some remarks on the clock input pin follow:

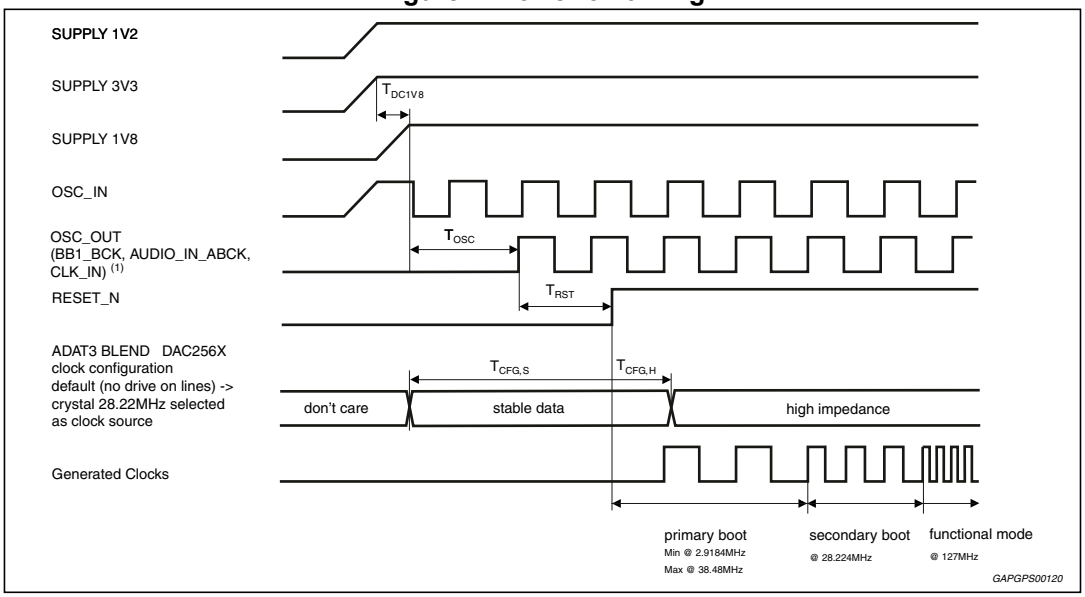
- OSC_IN is always a 1.8 V input pin;
- CLK_IN, BB1_BCK are 3.3 V;
- When the clock is fed through the CLK_IN pin, the OSC_IN pin must be connected to ground (and vice versa);
- The BB1_BCK pin is the bit clock of the digital interface to the baseband Tuner. When this pin is selected as input for the reference clock, the selected clock frequency must be chosen compatibly with the Primary baseband Interface settings (see *Section 5.2*):
  - 10.4 MHz = 16 * 650 kHz → BBI set to 650 Ksample/s
  - 10.8 MHz = 16 * 675 kHz → BBI set to 675 Ksample/s;
- When the device reference clock comes from BB1_BCK it is suggested to connect the OSC_IN to ground and to tie the CLK_IN pin to its high value (3.3 V).

3.2 Power on

This chapter describes the power-on procedure for the cold start (i.e. when the device is not supplied before being turned on). *Figure 7* and *Table 4* show the timing for the cold start power up sequence.

Boot pins are latched at startup. Their default value is logic 0, in case logic 1 is needed a 6K2 pull-up resistor should be connected on the corresponding boot line. After reset release, the boot selection lines become outputs.

Figure 7. Power on timing



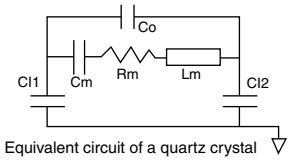
1. In case the Reference Clock is fed through BB1_BCK or CLK_IN the Power On timing diagram is the same as *Figure 7* where OSC_OUT is substituted by the external supplied stable reference clock.

Table 4. Power on timing parameters

Symbol	Parameter	Min	Max	Unit
$T_{ramp-up}$	External supply ramp-up time	Same ramp-up time for 3.3 V and 1.2 V supply		-
T_{DC1V8}	DC1V8 regulator start-up time	-	1	ms
T_{OSC} (1)	Oscillator start-up time	-	400	µs
T_{RST}	Reset release time	2	-	ms
$T_{CFG,S}$	Setup time for clock configuration	0.1	-	µs
$T_{CFG,H}$	Hold time for clock configuration	10	-	ns

1. The oscillator start-up time depends on the crystal connected to the internal oscillator. The given value is estimated for a crystal with characteristic shown in *Figure 8*.

Figure 8. Crystal characteristics



Model	Value
Rm	50 Ohm
Lm	1.33 mH
Cm	26 fF
CO	7 pF
Ci = CI1 = CI3	38pF (33pF + 5pF parasitic)

GAPGPS00121