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DATA SHEET

TWO-CHANNEL HD AUDIO CODEC WITH MODEM & DUAL DIGITAL MICROPHONE INTERFACES

STAC9250/9251

DESCRIPTION

The STAC9250/9251 are high fidelity, 2-channel audio CODECs compliant with the High Definition Audio (HD Audio) specification defined by Intel. The STAC9250/9251 enables a two-chip audio and modem implementation by integrating the “System Side” functionality of Silicon Labs’ modem solution. The STAC9250/9251 provides a direct interface to Silicon Labs’ “Line Side” integrated circuit. This integration results in cost savings without sacrificing audio fidelity or modem functionality. The STAC9251 also implements a direct interface to two digital microphones, supporting advanced beam forming applications and resulting in increased quality of voice applications.

FEATURES

- **High-integration HD Audio Product**
  - 2-channel PC Audio CODEC
  - Modem “System-side” functionality[1]
  - Dual Digital Microphone interface(STAC9251)
- **Two-Channel DACs and ADCs with 24-bit sample resolution**
  - High performance ΣΔ technology
  - Sample rates up to 192 KHz
  - 100dB DAC SNR
- **Integrated modem functionality from Silicon Labs[1] supports reduced BOM costs**
  - Interfaces directly to Line Side integrated circuit from Silicon Labs
  - Supports two-chip audio plus modem functionality
  - Supports Software modem implementations from Motorola and others compatible with the Silicon Labs chipset
  - Supports Motherboard implementations eliminating MDC card and connector costs
  - Reduced board space
  - Reduced external component count
- **Integrated Headphone Amps**
- **Stereo Analog Microphone**
  - Supports Stereo Microphone
  - Microphone Boost 0, 10, 20, 30, 40dB
-
- **S/PDIF In and Out**
- **Universal Jacks™ Functionality for jack retasking**
- **Adjustable VREF Out**
- **Digital PC Beep to all outputs**
- **48-pin LQFP Environmental Package**
- **Two-Channel High Definition Audio CODEC with Modem and Dual Digital Microphone Interfaces**

1. Modem functionality can only be used with a “Line Side” DAA integrated circuit, Si3080 or similar, available from Silicon Labs (www.silabs.com).

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1. DESCRIPTION

1.1. Overview

The STAC9250/9251 are high fidelity, 2-channel audio CODECs compliant with the High Definition Audio (HD Audio) specification defined by Intel. The STAC9250/9251 enables a two-chip audio and modem implementation by integrating the “System Side” functionality of Silicon Labs’ modem solution. The STAC9250/9251 provides a direct interface to Silicon Labs’ “Line Side” integrated circuit. This integration results in cost savings without sacrificing audio fidelity or modem functionality. The STAC9251 also implements a direct interface to two digital microphones supporting advanced beam forming applications resulting in increased quality of voice applications.

1.2. Features

- High-integration HD Audio Product
  - 2-channel PC Audio CODEC
  - Modem “System-side” functionality[1]
  - Dual Digital Microphone interface (STAC9251)
- Two-Channel DACs and ADCs with 24-bit sample resolution
  - High performance ΣΔ technology
  - Sample rates up to 192 KHz
  - 100dB DAC SNR
- Integrated modem functionality from Silicon Labs[1] supports reduced BOM costs
  - Interfaces directly to Line Side integrated circuit from Silicon Labs
  - Supports two-chip audio plus modem functionality
  - Supports software modem implementations from Motorola and others compatible with the Silicon Labs chipset
  - Supports motherboard implementations eliminating MDC card and connector costs
  - Reduced board space
  - Reduced external component count
- Integrated Headphone Amps
- Stereo Analog Microphone
  - Supports Stereo Microphone
  - Microphone Boost 0, 10, 20, 30, 40dB
- Dual Digital Microphone Interface optimized for use with Akustica Digital Microphones. (STAC9251 only)
- S/PDIF In and Out
- Universal Jacks™ Functionality for jack retasking
- Adjustable VREF Out
- Digital PC Beep to all outputs
- 48-pin LQFP Environmental Package

1. Modem functionality can only be used with a “Line Side” DAA integrated circuit, Si3080 or similar, available from Silicon Labs (www.silabs.com).

1.3. Description

The STAC9250/9251 are high fidelity, 2-channel audio CODECs compatible with the Intel High Definition (HD) Audio Interface. The STAC9250/92511 provide high quality, HD Audio capability to notebook and cost sensitive desktop PC applications.

The STAC9250/9251 incorporate IDT's proprietary $\Sigma\Delta$ technology to achieve a DAC SNR of 100dB. The higher performance and quality of IDT's audio solutions brings consumer electronics level performance to the notebook, desktop and media center PC.

The STAC9250/9251 provide stereo 24-bit, full duplex resolution supporting sample rates up to 192 KHz by the DAC and ADC. The STAC9250/9251 SPDIF In/Out support sample rates of 96 KHz, 48 KHz and 44.1 KHz plus SPDIF_OUT supports 88.2 KHz. Additional sample rates are supported by the driver software.

The STAC9250/9251 supports flexible configurations including switchable Headphone Out and Universal Jacks™ functionality for jack detection and re-tasking. The SPDIF interface provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini-disk drives or to a home entertainment system. All analog I/O pairs support LINE_IN, LINE_OUT and MIC.

MIC inputs can be programmed with 0/10/20/30/40dB boost. For more advanced configurations, the STAC9250/9251 have four General Purpose I/O (GPIO) pins. The STAC9250/9251 also provide a single ended CD input for compatibility with DRM solutions and to support legacy OS issues.

The STAC9250/9251 integrate a headphone amplifier, which is available on Ports A and D. The headphone amplifier is switchable between these two outputs for increased flexibility, enhanced user experience, and reduced implementation costs.

The Universal Jack capabilities allow the CODECs to detect when audio devices are connected, and allow the CODECs to be reconfigured to support these devices regardless of which port they are connected to. SPDIF input sensing is also supported. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

Note: The Jack Detect circuit and component selection are critical for accurate detection of audio jacks on individual ports. Please see the IDT STAC9250/9251 reference design for circuit implementation details.

The STAC9250/9251 operate with a 3.3 V digital supply and a 3.3 V, 4 V, and 5 V analog supply.

The STAC9250/9251 are available in a 48-pin LQFP Environmental (ROHS) package.

2. CHARACTERISTICS

2.1. Audio Fidelity

DAC SNR: 100dB
ADC SNR: 90dB

2.2. Electrical Specifications

2.2.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9250/9251. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0^{o}C to +70^{o}C
Storage temperature		-55 ^{o}C to +125 ^{o}C
Soldering temperature		260 ^{o}C for 10 seconds * Soldering temperature information for all available packages begins on page 134.

2.2.2. Recommended Operation Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
(Note: The +4 V Analog voltage is supported by the +5 V version of the STAC9250/9251.)	Analog - 4 V	3.8	4	4.2	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (48-LQFP)			+90	°C

ESD: The STAC9250/9251 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the STAC9250/9251 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.3. STAC9250/9251 5V Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 5.0 V ± 5%, DVdd = 3.3 V ± 5%, AVss = DVss = 0 V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 VRMS, 10 KΩ / 50 pF load, Testbench Characterization BW: 20 Hz – 20 KHz, 0dB settings on all gain stages)

Min and Max performance targets are not included here, as specific system characteristics, such as layout, routing and external CODEC component selection, influence the performance of the CODEC. To receive min/max levels for your system, please send us a unit and IDT will perform a full audio test suite and provide you with the results. Contact IDT for more information.

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs with out boost	-	1.00	-	Vrms
All Analog Inputs with boost (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
PCM (DAC) to All Analog Outputs	-	1.00	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel (peak)	-	50	-	mW
Dynamic Range: -60dB signal level (Note 2)				
PCM to All Analog Outputs	-	99	-	dB
All Analog Inputs to A/D (1 VRMS Input Referenced)	-	88	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
PCM to All Analog Outputs	-	-90	-	dB
All Analog Inputs to A/D (-3dBV input Level)	-	-87	-	dB
HEADPHONE_OUT (32 Ω load)	-	-87	-	dB
HEADPHONE_OUT (10 KΩ load)	-	-90	-	dB
SNR (idle channel) (Note 5)				
DAC to All Analog Outputs	-	100	-	dB
All Analog Inputs to A/D with High Pass Filter enabled	-	89	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to ADC (10 KHz Signal Frequency) Crosstalk	-	-90	-	dB
Any Analog Input to ADC (1 KHz Signal Frequency) Crosstalk	-	-90	-	dB
Spurious Tone Rejection	-	-100	-	dB

Parameter	Min	Typ	Max	Unit
Attenuation, Gain Step Size ANALOG	-	1.5	-	dB
Attenuation, Gain Step Size DIGITAL	-	0.75	-	dB
Input Impedance	-	50	-	KW
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45 X AVdd	0.5	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	-	dB
Gain Drift	-	100	-	ppm/ºC
DAC Offset Voltage	-	5	10	mV
Deviation from Linear Phase	-	10	1	deg.
All Analog Outputs Load Resistance	-	10	-	KΩ
All Analog Outputs Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-	100	-	pF
Mute Attenuation	-	-	-	dB
PLL lock time	-	96	200	μsec
PLL (or HD Audio Bit CLK) 24.576 MHz clock jitter	-	100	300	psec

1. With +30dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured “A weighted” over a 20 Hz to a 20 KHz bandwidth.
3. ± 1dB limits for Line Output & 0dB gain, at -20dBV
4. Amplitude of THD+N, measured with A-weighting filter, over 20 Hz to 20 KHz bandwidth.
5. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

2.4. STAC9250/9251 4V Analog Performance Characteristics

If you are interested in using the STAC9250/9251 at 4V Analog, please contact IDT for more information.

2.5. STAC9250/9251 3.3V Analog Performance Characteristics

If you are interested in using the STAC9250/9251 at 3.3V Analog, please contact IDT for more information.

2.6. Power Consumption

2.6.1. Digital

Audio Power State	Modem Power State	Typical	Max	units
D0	D0 INIT	41	43	mA
D1	D0 UN INIT	28	29	mA
D2	D3 HOT	34	36	mA
D3	D3 COLD	27	28	mA

Table 1. Digital Power Consumption

2.6.2. 5V Analog

Audio Power State	Modem Power State	Typical	Max	units
D0	D0 INIT	30	36	mA
D1	D0 UN INIT	12	26	mA
D2	D3 HOT	12	26	mA
D3	D3 COLD	11	26	mA

Table 2. 5V Analog Power Consumption

3. DETAILED DESCRIPTION

3.1. SPDIF Input

SPDIF IN can operate at 44.1 KHz or 96 KHz, and implements internal Jack Sensing. A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to directly accept consumer SPDIF voltage levels eliminates the need for costly external receiver ICs. Advanced features such as record slot select and SPDIF_IN routing to the DAC allows for simultaneous record and play.

3.2. SPDIF Output

SPDIF OUT can operate at 44.1 KHz, 48 KHz, 88.2 KHz, and 96 KHz, as defined in the Intel High Definition Audio Specification, with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

3.3. Digital Microphone Support (STAC9251 only)

The STAC9251 has a three-pin digital microphone interface that accepts high-rate, single-bit data streams from two digital microphones. Each microphone requires only one data line. Both microphones share a single clock line. This robust digital interface gives designers the flexibility to place the microphones in the optimum location on a system (such as along the top of the screen bezel) and use a simple, 3-wire ribbon cable to directly connect the microphones to the STAC9251 CODEC.

3.4. SiLabs System Side Modem

A licensed Silicon Labs System Side modem based on the Si3054 architecture is integrated into STAC9250/9251. Combined with a Silicon Labs Line Side IC (Si3080 or similar), the STAC9250/9251 allows designers to implement a two-chip HD Audio and HD Modem solution for significant cost and board space savings.

3.5. Mono Out

The MONO Output is connected to pin 37 and has independent volume and mute control (see the Widget listing for details). The MONO Output derives it's input from the output of the summing node that drives PORT A and PORT D. The following analog signals feed the summing amplifier that feeds the MONO Out summing amplifier:

- DAC Output: When enabled, both DAC Outputs are summed together.
- Analog PC Beep: Source from Pin 12
- ADC Input: Stereo analog feed into the stereo ADC input.

The combination of the stereo channels from DAC are combined into a single analog signal with a -6dB degradation in signal strength.

3.6. Headphone Drivers (Restrictions)

It is not recommended that users operate both Port A and Port D as headphone drivers simultaneously. Using both ports as headphone drivers degrades the signal quality of both outputs.[1]

Note: 1) Headphone capabilities are on Port A (pins 39/41) and Port D (pins 35/36). Do NOT put headphone loads on both sets of pins at the same time.

3.7. Universal Jacks™

IDT's Universal Jacks™ technology allows for flexibility in board design and implementation.

On the STAC9250/9251, only one function can be selected at a time. A set of pins cannot be set as input and output at the same time. However, the selected function can be changed at any time.

For the STAC9250/9251, the Universal Jacks capabilities are as follows

- All of the STAC9250/9251 ports support:
  - Line Out
  - Line In
  - Mic with 0/10/20/30/40[2] dB Mic Boost
- Ports A and D also support:
  - Headphone Out[1]

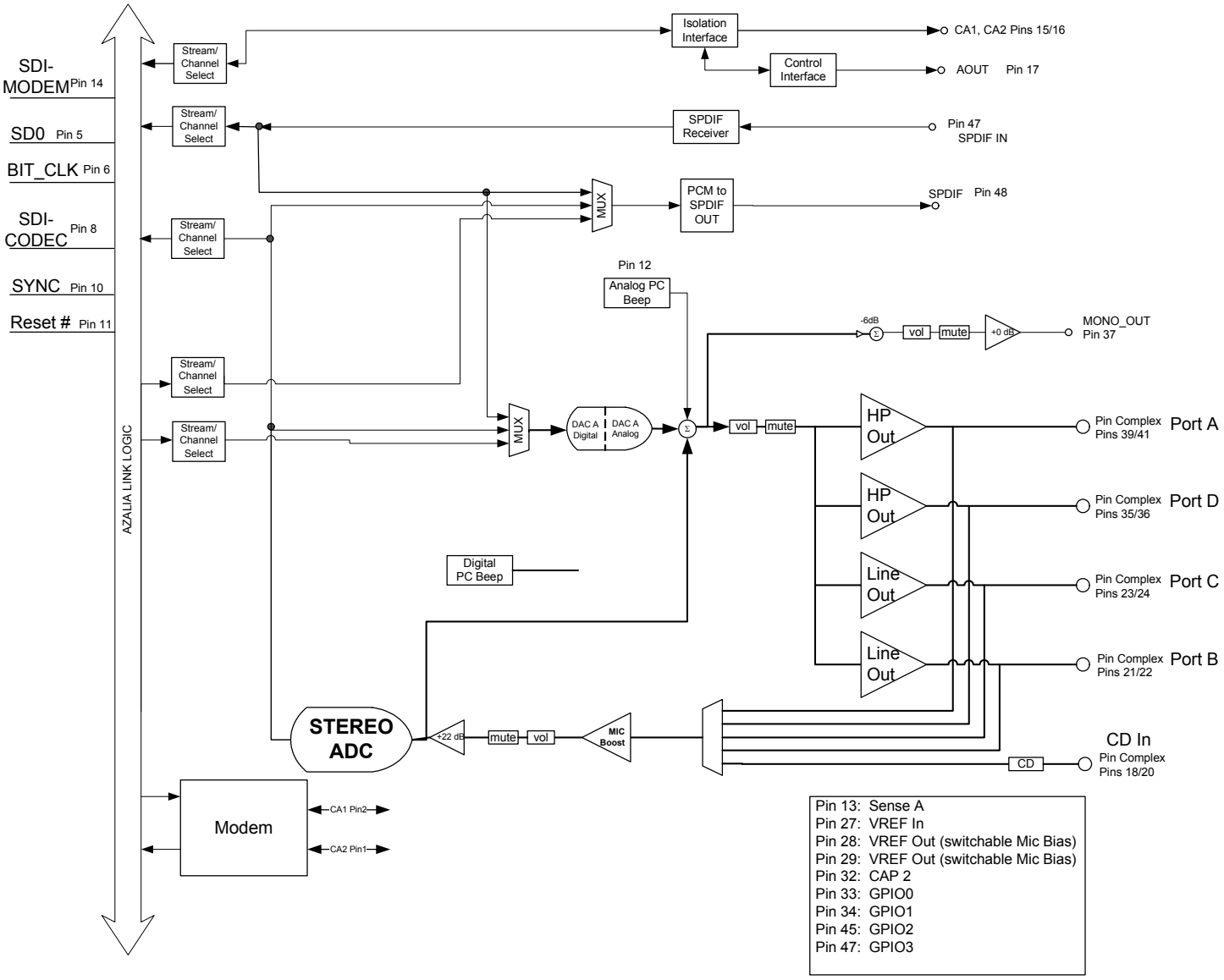
Note: 1) Headphone capabilities are on Port A (pins 39/41) and Port D (pins 35/36). Do NOT put headphone loads on both sets of pins at the same time.

Note: 2) When the 40dB mic boost feature is enabled, additional gain increases greater than 6dB may result in significant audio quality degradation of the microphone audio input. In particular, when the 40dB MIC boost is active, the SNR, THD+N and DC offset will significantly degrade regardless of the input signal level.

4. FUNCTIONAL BLOCK DIAGRAMS

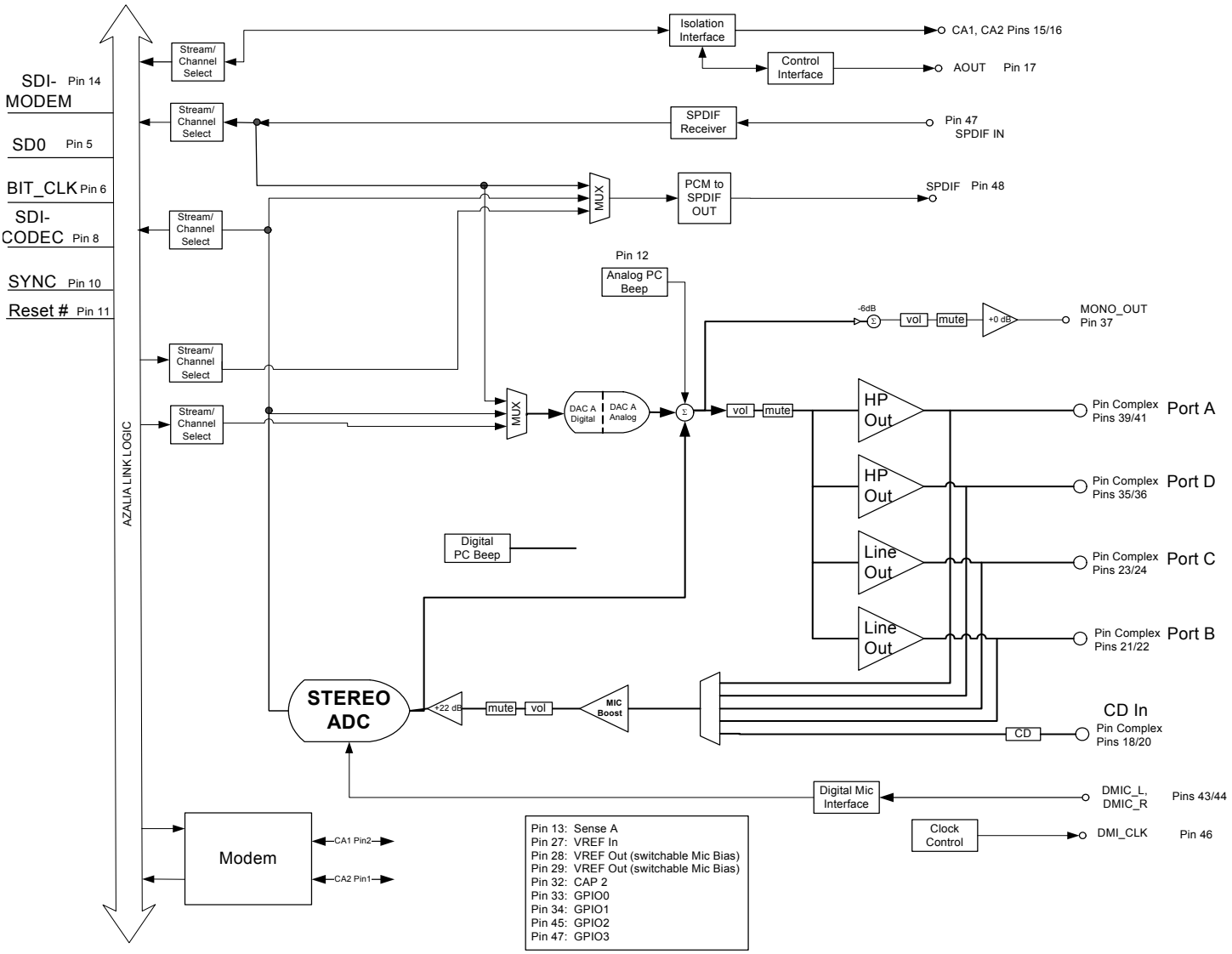
4.1. STAC9250

Figure 1. STAC9250 Functional Block Diagram



4.2. STAC9251

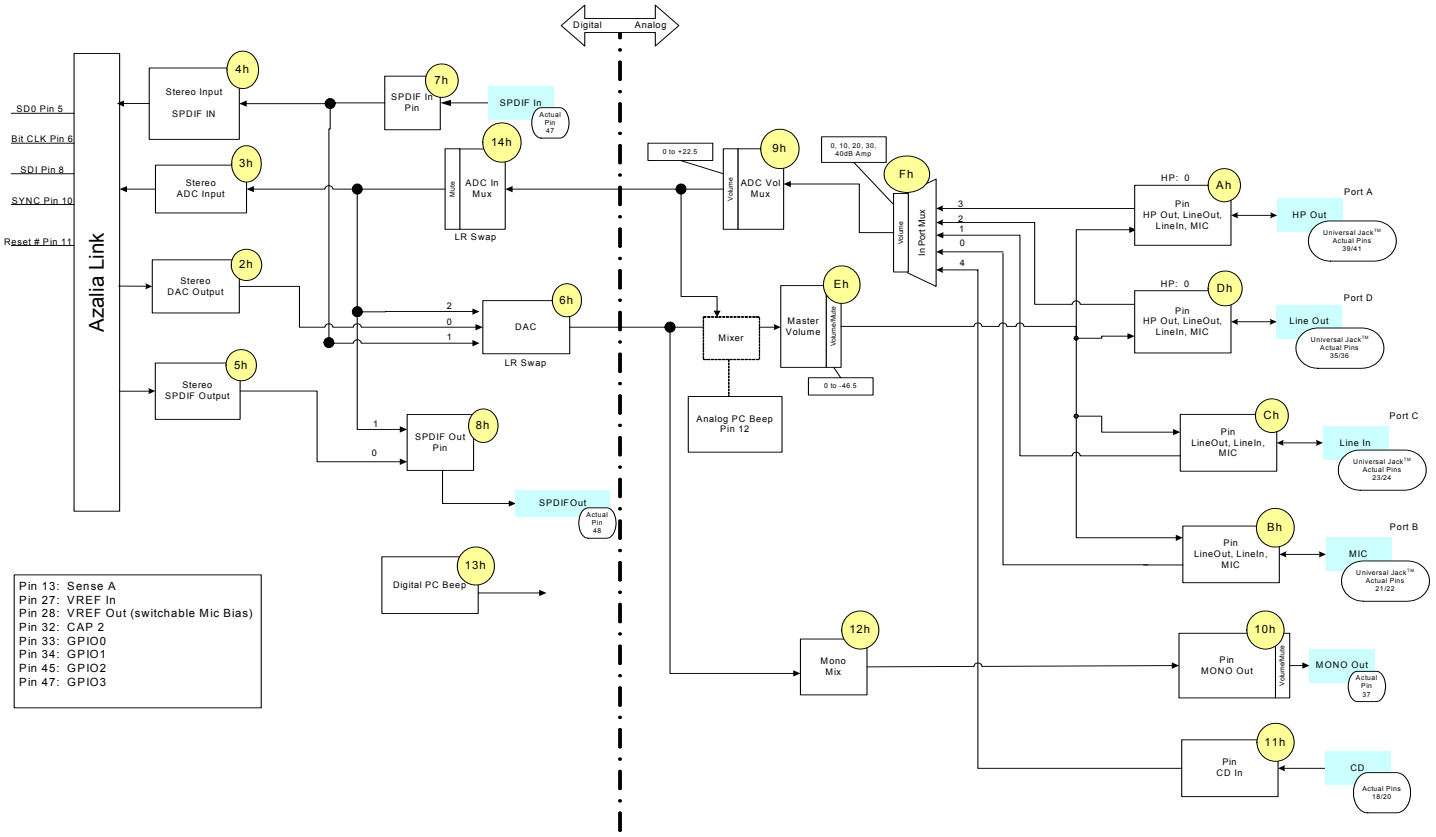
Figure 2. STAC9250 Functional Block Diagram



5. WIDGET INFORMATION

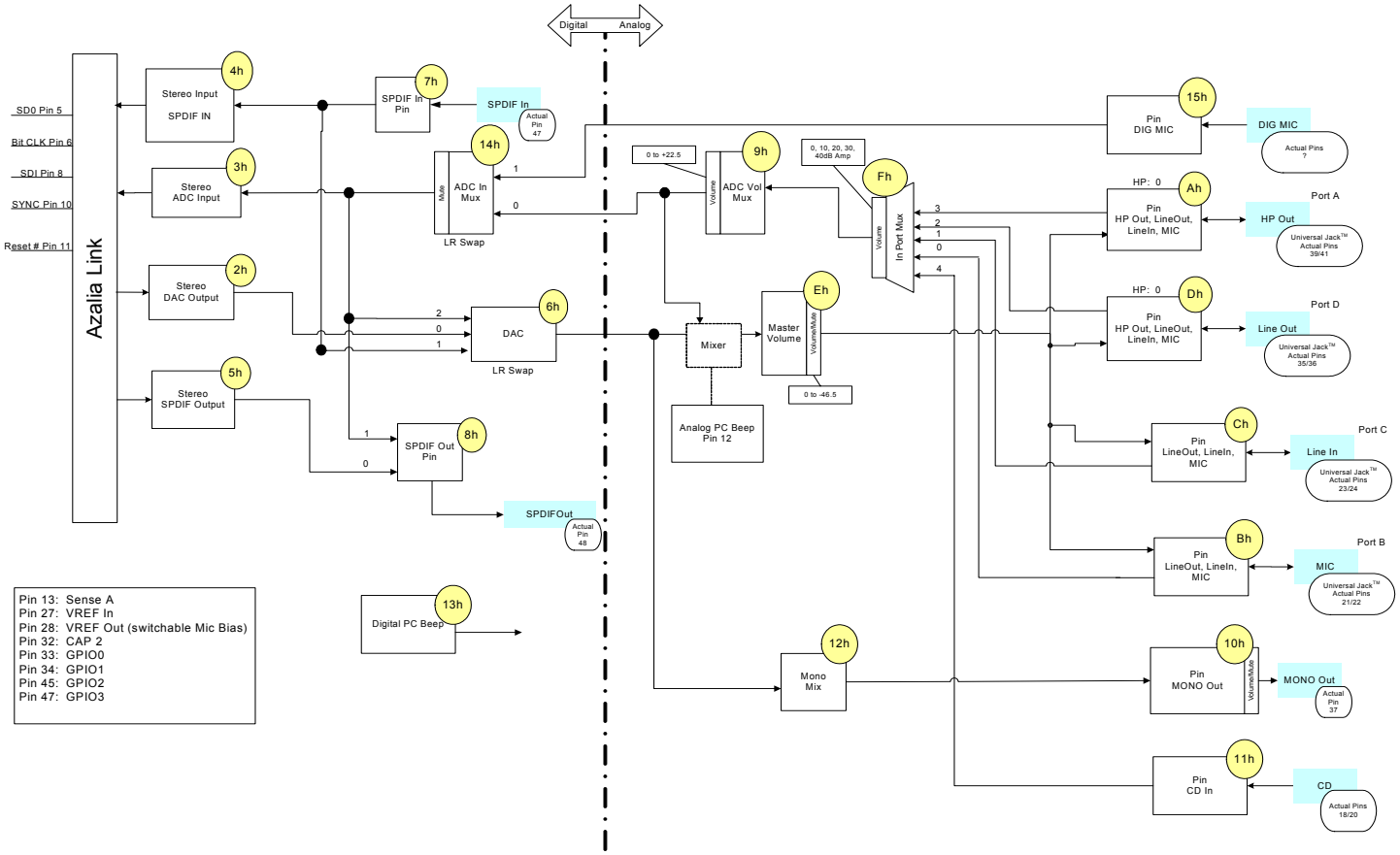
5.1. Widget Diagram - STAC9250

Figure 3. STAC9250 Widget Diagram



5.2. Widget Diagram - STAC9251

Figure 4. STAC9251 Widget Diagram



5.3. Widget List - STAC9250/9251

Table 3. High Definition Audio Widget

ID	Widget Name	Description
00h	Root	Root Node
01h	Audio Function Group	Audio Function Group (AFG)
02h	DAC0	Stereo Ouput to DAC
03h	ADC0	Stereo Input from ADC
04h	SPDIF_IN	Stereo Input for SPDIF_In
05h	SPDIF_OUT	Stereo Output for SPDIF_Out
06h	DAC0Mux	DAC Mux and Boost for outputs for DAC
07h	DigPin1	Pin Widget for SPDIF_In (pin 47)
08h	DigPin0	Pin Widget for SPDIF_Out (pin 48)
09h	ADC0VolMux	ADC0 Volume
0Eh	MasterVolume	Master Volume Controls
0Fh	InPortMux	Port Mux for ADC0
0Ah	Port A	Port A Pin Widget (Pins 39/41, configurable as HP, Line In, Line Out, Mic)
0Dh	Port D	Port D Pin Widget (Pins 35/36, configurable as HP, Line In, Line Out, Mic)
0Ch	Port C	Port C Pin Widget (Pins 23/24, configurable as Line Out, Mic)
0Bh	Port B	Port B Pin Widget (Pins 21/22, configurable as Line Out, Mic)
10h	MonoOut	Mono Output from DAC
11h	CD	CD Pin Widget pins 18/19/20
12h	MonoOutMix	Mixer for Mono Ouput
13h	Digital PC Beep	Digital PC Beep
14h	ADC0InMux	Input Mux for ADC converter
15h	DigMicPin	Pin Widget for Digital Microphone (Pins 43/44/46 configurable as a Mic) (STAC9251 only)

5.4. Root Node (NID = 0x00)

5.4.1. Root PnpID

Table 4. Root PnpID Command Verb Format

	Verb ID	Payload	Response
Get	F00	00	See bitfield table

Table 5. Root PnpID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Vendor	R	0x8384	Vendor ID = 8384h
[15:0]	Device	R	0x7630	Device ID for: STAC9250 = 7634 STAC9251 = 7636

5.4.2. Root RevID

Table 6. Root RevID Command Verb Format

	Verb ID	Payload	Response
Get	F00	02	See bitfield table

Table 7. Root RevID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd	R	0x00	Reserved
[23:20]	Major	R	0x1	Major rev number of compliant HD Audio specification
[19:16]	Minor	R	0x0	Minor rev number of compliant HD Audio specification
[15:8]	Vendor	R	0x01	Vendor rev number for this device ID
[7:0]	Stepping	R	0x01	Vendor stepping number within the given Vendor RevID

5.4.3. Root NodeInfo

Table 8. Root NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table

Table 9. Root NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x00	Reserved
[23:16]	StartNID	R	0x01	Starting node number (NID) of first function group
[15:8]	Rsvd1	R	0x00	Reserved
[7:0]	TotalNodes	R	0x01	Total number of nodes

5.5. AFG Node (NID = 0x01)

5.5.1. AFG Reset

Table 10. AFG Reset Command Verb Format

	Verb ID	Payload	Response
Get	7FF	00	See bitfield table
Set1	7FF	See bits [7:0] of bitfield table	0000_0000h

Table 11. AFG Reset Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:0]	Response	R	0x0	Reserved. Overlaps Execute.
[0]	Execute	W	0x0	Function Reset. Function Group reset is executed when the Set verb 7FF is written with 8-bit payload of 00h. The CODEC should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response.

5.5.2. AFG NodeInfo

Table 12. AFG NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table

Table 13. AFG NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:16]	StartNID	R	0x02	Starting node number for function group subordinate nodes.
[15:8]	Rsvd1	R	0x0	Reserved
[7:0]	TotalNodes	R	0x14	Total number of nodes. 13h for STAC9250 14h for STAC9251