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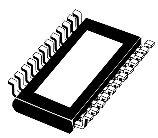
STAP16DPPS05

Low voltage 16-bit constant current LED sink driver with output error detection and auto power-saving for automotive applications

Datasheet - production data



HTSSOP24 (exposed pad)

Features

- AECQ100 qualification
- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Short and open output error detection
- Serial data IN/parallel data OUT
- 3.3 V micro driver-able
- Auto power-saving
- Output current: 3 - 40 mA
- Auto power-saving
- Max. clock frequency: 30 MHz
- 20 V current generator rated voltage
- Power supply voltage: from 3 V to 5.5 V
- Thermal shutdown for overtemperature protection
- ESD protection 2.0 KV HBM

Applications

- Dashboard and infotainment backlighting
- Exterior/interior lighting
- DTRLs

Description

The STAP16DPPS05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The device contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit D-type storage register. In the output stage, sixteen regulated current sources are designed to provide 3 to 40 mA of constant current to drive the LEDs.

The STAP16DPPS05 features the open and short LED detection on the outputs. The detection circuit checks 3 different conditions which may occur on the output line: short to GND, short to V_O or open line. The data detection results are loaded in the shift register and shifted out via the serial line output. The detection functionality is implemented without increasing the pin number through a secondary function of the output enable and latch pin (DM1 and DM2 respectively). A dedicated logic sequence allows the device to enter or leave detection mode. Through an external resistor, users can adjust the output current of the STP16DPPS05 thus controlling the light intensity of the LEDs. In addition, the user can adjust the intensity of the brightness of the LED's from 0% to 100% through the $\overline{OE/DM2}$ pin. The auto power shutdown and auto power-ON feature allows the device to save power with no external intervention. The STAP16DPPS05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz also satisfies the system requirement of high volume data transmission. The 3.3 V of voltage supply is very useful for applications interfacing any microcontroller from 3.3 V micro. Compared with a standard TSSOP package, the TSSOP exposed pad increases the capability of heat dissipation by a factor of 2.5.

Table 1. Device summary

Order code	Package	Packing
STAP16DPPS05XTTR	HTSSOP24 (exposed pad)	2500 parts per reel

Contents

1 **Summary description** 5

1.1 Pin connections and description 5

2 **Electrical ratings** 7

2.1 Absolute maximum ratings 7

2.2 Thermal data 7

2.3 Recommended operating conditions 8

3 **Electrical characteristics** 9

4 **Equivalent circuit and outputs** 11

5 **Timing diagrams** 13

6 **Typical characteristics** 16

7 **Error detection mode functionality** 20

7.1 Phase one: entering error detection mode 20

7.2 Phase two: error detection 21

7.3 Phase three: resuming normal mode 23

7.4 Error detection conditions 23

7.5 Auto power-saving 25

8 **Package information** 27

8.1 TSSOP24 exposed pad package information 28

8.2 TSSOP24 exposed pad packing information 30

9 **Revision history** 32

List of tables

Table 1. Device summary 1
Table 2. Typical current accuracy 5
Table 3. Pin description 5
Table 4. Absolute maximum ratings 7
Table 5. Thermal data 7
Table 6. Recommended operating conditions 8
Table 7. Electrical characteristics 9
Table 8. Switching characteristics 10
Table 9. Truth table 13
Table 10. Enable IO: shutdown truth table 14
Table 11. Output current vs. REXT resistor 16
Table 12. ISET vs. dropout voltage (Vdrop) 17
Table 13. Entering error detection mode - truth table 20
Table 14. Resuming normal mode - timing diagram 23
Table 15. Detection conditions (VDD = 3.3 to 5 V, temperature range -40 to 125 °C) 23
Table 16. TSSOP24 exposed pad mechanical data 29
Table 17. TSSOP24 exposed pad tape and reel mechanical data 31
Table 18. Document revision history 32

List of figures

Figure 1. Pin connections . . . 5
Figure 2. OE/DM2 terminal . . . 11
Figure 3. LE/DM1 terminal . . . 11
Figure 4. CLK, SDI terminal . . . 11
Figure 5. SDO terminal . . . 12
Figure 6. Block diagram . . . 12
Figure 7. Timing diagram . . . 13
Figure 8. Clock, serial-in, serial-out . . . 14
Figure 9. Clock, serial-in, latch, enable, outputs . . . 15
Figure 10. Outputs . . . 15
Figure 11. Output current vs. REXT resistor . . . 16
Figure 12. ISET vs. dropout voltage (Vdrop) . . . 17
Figure 13. Output current vs. ± ΔIOL(%) . . . 18
Figure 14. Idd ON/OFF . . . 18
Figure 15. Power dissipation vs. package temperature . . . 19
Figure 16. Turn-ON output current characteristics . . . 19
Figure 17. Turn-OFF output current characteristics . . . 19
Figure 18. Entering error detection mode - timing diagram . . . 20
Figure 19. Detection diagram . . . 21
Figure 20. Timing example for open and/or short-circuit detection . . . 22
Figure 21. Detection circuit . . . 23
Figure 22. Error detection sequence . . . 24
Figure 23. Auto power-saving feature . . . 25
Figure 24. Auto power-saving feature: first output TON . . . 26
Figure 25. TSSOP24 exposed pad package outline . . . 28
Figure 26. TSSOP24 exposed pad tape and reel outline . . . 30

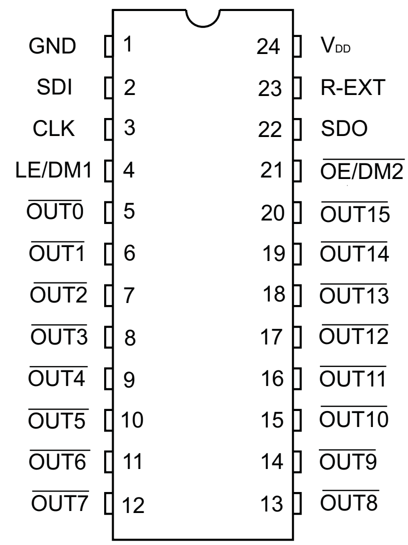
1 Summary description

Table 2. Typical current accuracy

Output voltage	Current accuracy		Output current	V_{DD}	Temperature
	Between bits	Between ICs			
≥ 1.3 V	± 1%	± 2%	5 to 40 mA	3.3 V to 5 V	25 °C

1.1 Pin connections and description

Figure 1. Pin connections



Note: The exposed pad is electrically connected to a metal layer electrically isolated or connected to ground.

Table 3. Pin description

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE/DM1	Latch input terminal - detect mode 1 (see operation principle)
5-20	OUT-15	Output terminal
21	$\overline{OE/DM2}$	Input terminal of output enable (active low) - detect mode 1 (see operation principle)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal for an external resistor for constant current programming
24	V_{DD}	Supply voltage terminal

2 Electrical ratings

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{dd}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	50	mA
V_I	Input voltage	-0.4 to V_{dd}	V
I_{GND}	GND terminal current	800	mA
f_{CLK}	Clock frequency	50	MHz
T_{OPR}	Operating temperature range	-40 to +150	°C
T_{STG}	Storage temperature range	-55 to +150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter		Value	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient (1)	TSSOP24(2) exposed pad	37.5	°C/W

1. According to JEDEC standard 51-7B.
2. The exposed pad should be soldered to the PCB in order to derive the thermal benefits.

2.3 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.0	-	5.5	V
V_O	Output voltage			-	20	V
I_O	Output current	OUTn	3	-	40	mA
I_{OH}	Output current	SeriaL-OUT		-	+1	mA
I_{OL}	Output current	Serial-OUT		-	-1	mA
V_{IH}	Input voltage		0.7 V_{DD}	-	V_{DD}	V
V_{IL}	Input voltage		-0.3	-	0.3 V_{DD}	V
t_{wLAT}	LE/DM1 pulse width	V_{DD} = 3.0 V to 5.0 V	20	-		ns
t_{wCLK}	CLK pulse width		10	-		ns
t_{wEN}	$\overline{OE/DM2}$ pulse width		100	-		ns
$t_{SETUP(D)}$	Setup time for DATA		8	-		ns
$t_{HOLD(D)}$	Hold time for DATA		5	-		ns
$t_{SETUP(L)}$	Setup time for LATCH		8	-		ns
f_{CLK}	Clock frequency	Cascade operation (1)		-	30	MHz

1. If the device is connected in cascade, it may not be possible to achieve the maximum data transfer. Please consider the timings carefully.

3 Electrical characteristics

V_{DD} = 5 V, T_j = -40 °C to 125 °C, unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input voltage high level		$0.7 \cdot V_{DD}$		V_{DD}	V
V_{IL}	Input voltage low level		GND		$0.3 \cdot V_{DD}$	
V_{OL}	Serial data output voltage (SDO)	I_{OL} = + 1 mA		0.03	0.4	
V_{OH}		I_{OH} = - 1 mA	V_{DD}-0.4			
I_{OH}	Output leakage current	Vo =19 V, OUTn = OFF		0.5	2	µA
ΔI_{OL1}	Current accuracy channel-to-channel (1) (2)	V_{DD} = 3.3 V, V_O = 0.3 V, R_{ext} = 3.9 kΩ		±1	±5	%
ΔI_{OL2}		V_{DD} = 3.3 V, V_O = 0.6 V, R_{ext} = 980 Ω		±0.5	±4	
ΔI_{OL3}		V_{DD} = 3.3 V, V_O = 1.3 V, R_{ext} = 490 Ω		±0.5	±4	
ΔI_{OL2}	Current accuracy device-to-device(1)	V_{DD} = 3.3 V, V_O = 0.6 V, R_{ext} = 980 Ω			±5	
ΔI_{OL3}		V_{DD} = 3.3 V, V_O = 1.3 V, R_{ext} = 490 Ω			±6	
R_{IN}(up)	Pull-up resistor for OE pin		150	300	600	kΩ
R_{IN}(down)	Pull-down resistor for LE pin		100	200	400	
IDD(AutoOff)	Supply current (OFF)	R_{ext} = 980 Ω, OE = low, OUT0 to OUT7 = OFF		200	300	µA
IDD(OFF1)		R_{ext} = 980 Ω, OE = high, OUT0 to OUT7 = ON		5	7.5	mA
IDD(OFF2)		R_{ext} = 490 Ω, OE = high, OUT0 to OUT15 = ON		8	11	
IDD(ON1)	Supply current (ON)	R_{ext} = 980 Ω, OE = low, OUT0 to OUT15 = ON		6	7.5	
IDD(ON2)		R_{ext} = 490 Ω, OE = low, OUT0 to OUT15 = ON		8	11	
Tsd	Thermal shutdown(3)			170		°C

1. Test performed with all outputs turned on, but only one output loaded at a time.
2. $\Delta_{IOL}+ = ((I_{OLmax} - I_{OLmean}) / I_{OLmean}) * 100$, $\Delta_{IOL} - = ((I_{OLmin} - I_{OLmean}) / I_{OLmean}) * 100$, where $I_{OLmean} = (I_{OLout1} + I_{OLout2} + \ldots + I_{OLout16}) / 16$.
3. Not tested, guaranteed by design.

V_{DD} = 5 V, T_j = 25 °C, unless otherwise specified.

Table 8. Switching characteristics(1)(2)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
f_{clk}	Clock frequency	Cascade operation				30	MHz
t_{PLH1}	CLK-$\overline{\text{OUTn}}$, LE/DM1 = H, $\overline{\text{OE/DM2}}$ = L	$V_{IH} = V_{DD}$ V_{IL} = GND C_L = 10 pF I_O = 20 mA V_L = 3.0 V R_L = 60 Ω	V_{DD} = 3.3 V		55	90	ns
			V_{DD} = 5 V		30	50	
t_{PLH2}	LE/DM1-$\overline{\text{OUTn}}$, $\overline{\text{OE/DM2}}$ = L		V_{DD} = 3.3 V		48	80	ns
			V_{DD} = 5 V		30	45	
t_{PLH3}	$\overline{\text{OE/DM2}}$-$\overline{\text{OUTn}}$, LE\DM1 = H		V_{DD} = 3.3 V		70	120	ns
			V_{DD} = 5 V		45	65	
t_{PLH}	CLK-SDO		V_{DD} = 3.3 V		21	35	ns
			V_{DD} = 5 V		15	25	
t_{PHL1}	CLK-$\overline{\text{OUTn}}$, LE/DM1 = H, $\overline{\text{OE/DM2}}$ = L		V_{DD} = 3.3 V		28	35	ns
			V_{DD} = 5 V		22	40	
t_{PHL2}	LE/DM1-$\overline{\text{OUTn}}$, $\overline{\text{OE/DM2}}$ = L		V_{DD} = 3.3 V		13	35	ns
			V_{DD} = 5 V		12	18	
t_{PHL3}	$\overline{\text{OE/DM2}}$-$\overline{\text{OUTn}}$, LE/DM1 = H		V_{DD} = 3.3 V		24	35	ns
			V_{DD} = 5 V		21	30	
t_{PHL}	CLK-SDO		V_{DD} = 3.3 V		24	40	ns
			V_{DD} = 5 V		17	25	
t_{ON}	Output rise time 10~90% of voltage waveform		V_{DD} = 3.3 V		30	55	ns
			V_{DD} = 5 V		10	20	
t_{OFF}	Output fall time 90~10% of voltage waveform		V_{DD} = 3.3 V		4	10	ns
			V_{DD} = 5 V		3	8	
t_r	CLK rise time (3)					5	µs
t_f	CLK fall time (3)					5	

1. All table limits are guaranteed by design.
2. Not tested in production.
3. If devices are connected in cascade and tr or tf is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

4 Equivalent circuit and outputs

Figure 2. $\overline{\text{OE}}$/DM2 terminal

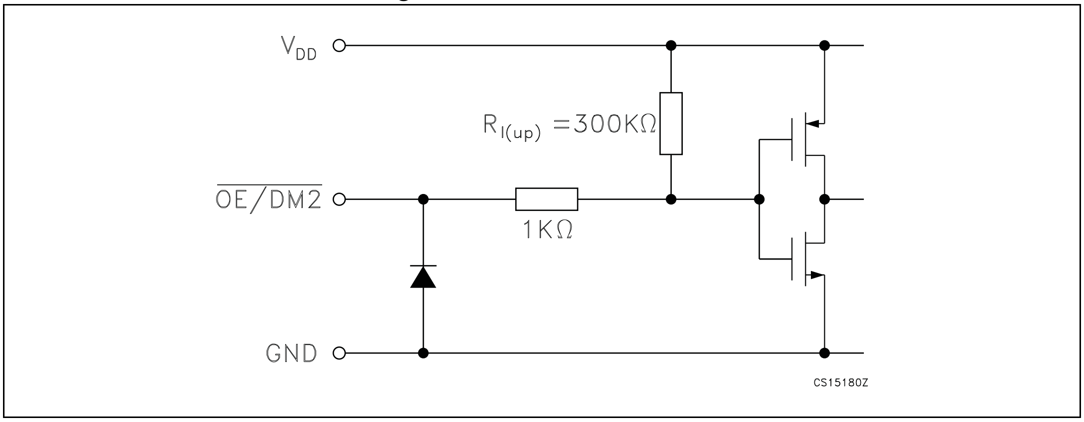


Figure 3. LE/DM1 terminal

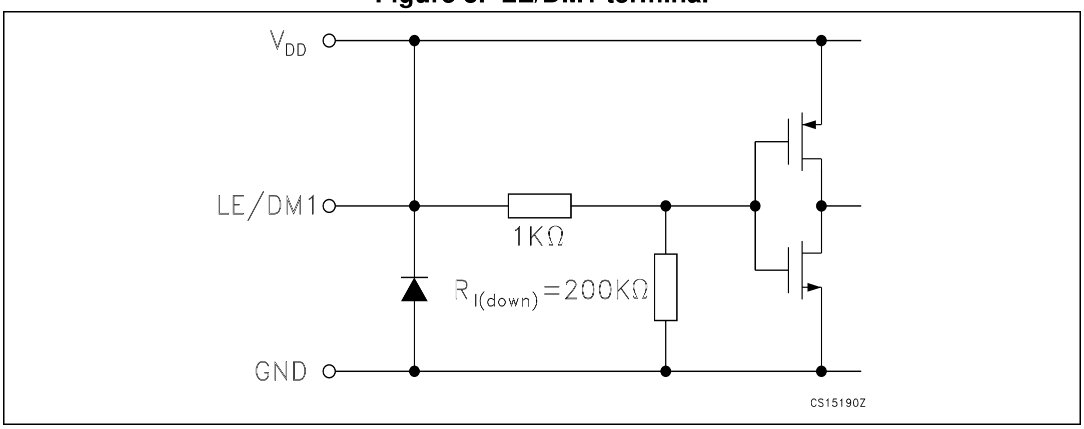


Figure 4. CLK, SDI terminal

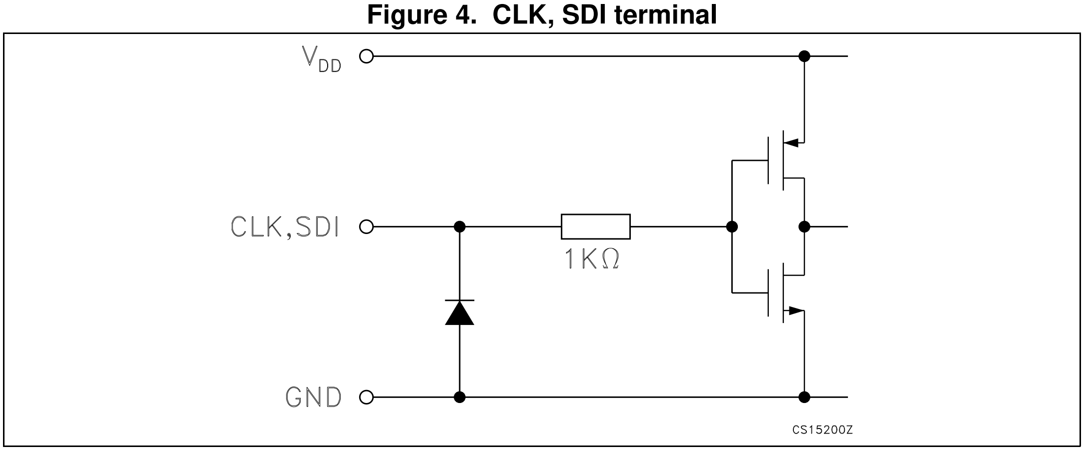


Figure 5. SDO terminal

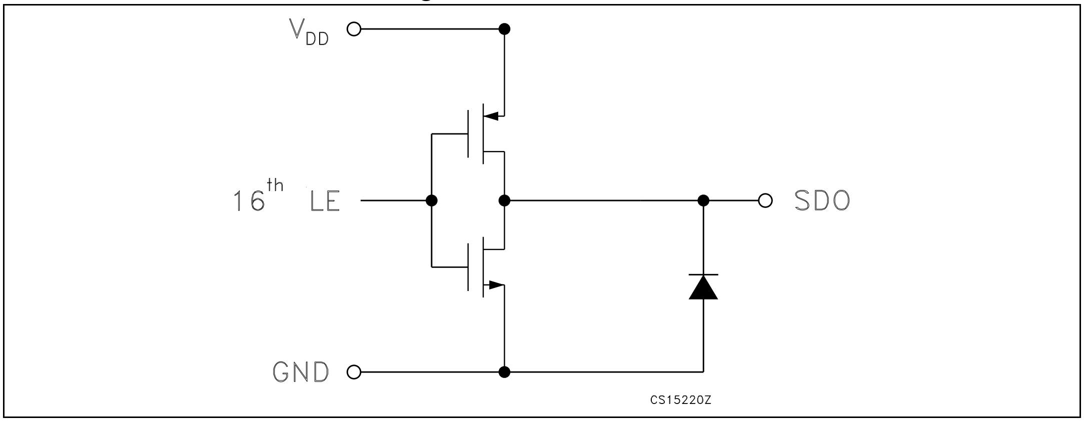
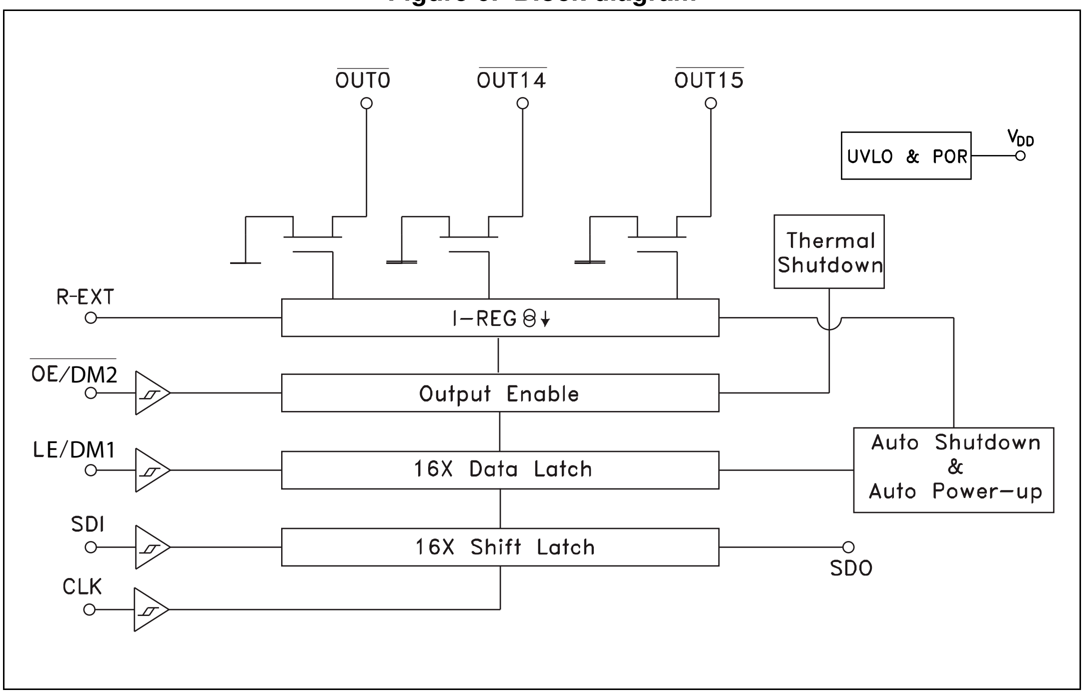


Figure 6. Block diagram



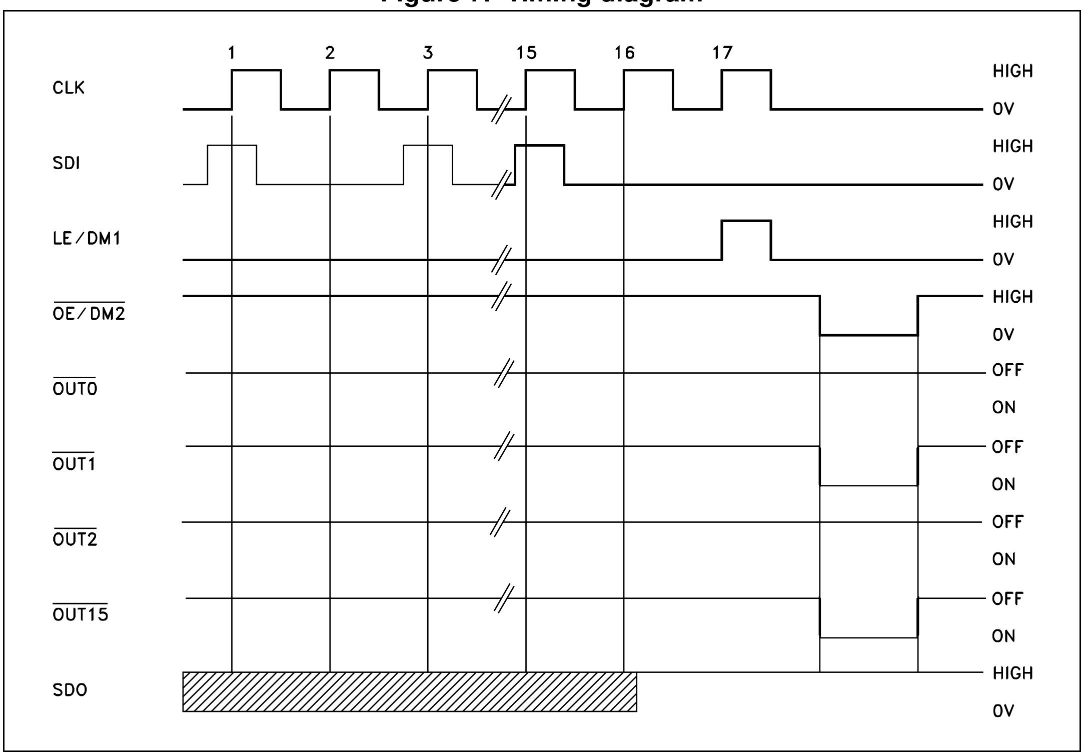
5 Timing diagrams

Table 9. Truth table

CLOCK	LE/DM1	$\overline{\text{OE/DM2}}$	SERIAL-IN	$\overline{\text{OUT0}}$............ $\overline{\text{OUT7}}$............... $\overline{\text{OUT15}}$	SDO
↑	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
↑	L	L	Dn + 1	No change	Dn - 14
↑	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
↓	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
↓	X	H	Dn + 3	OFF	Dn - 13

Note: OUTn = ON when Dn = H OUTn = OFF when Dn = L.

Figure 7. Timing diagram



Note: Latch and output enable terminals are level-sensitive and are not synchronized with rising or falling edge of LE/DM1 signal. When LE/DM1 terminal is low level, the latch circuit holds previous set of data. When LE/DM1 terminal is high level, the latch circuit refreshes new set of data from SDI chain. When $\overline{\text{OE/DM2}}$ terminal is at low level, the output terminals Out 0 to Out 15 respond to data in the latch circuits, either '1' ON or '0' OFF. When $\overline{\text{OE/DM2}}$ terminal is at high level, all output terminals are switched OFF.

Table 10. Enable IO: shutdown truth table

CLOCK	LE/DM1	SDI_0........... SDI_7............ SDI_{15}	SH	Auto power-up	$\overline{OUTn}$
↑	H	All = L	Active	Not active (1)	OFF
↑	L	No change	No change	No change	No change
↑	H	One or more = H	Not active	Active	X(2)

1. At power-up, the device starts in shutdown mode.
2. Undefined.

Figure 8. Clock, serial-in, serial-out

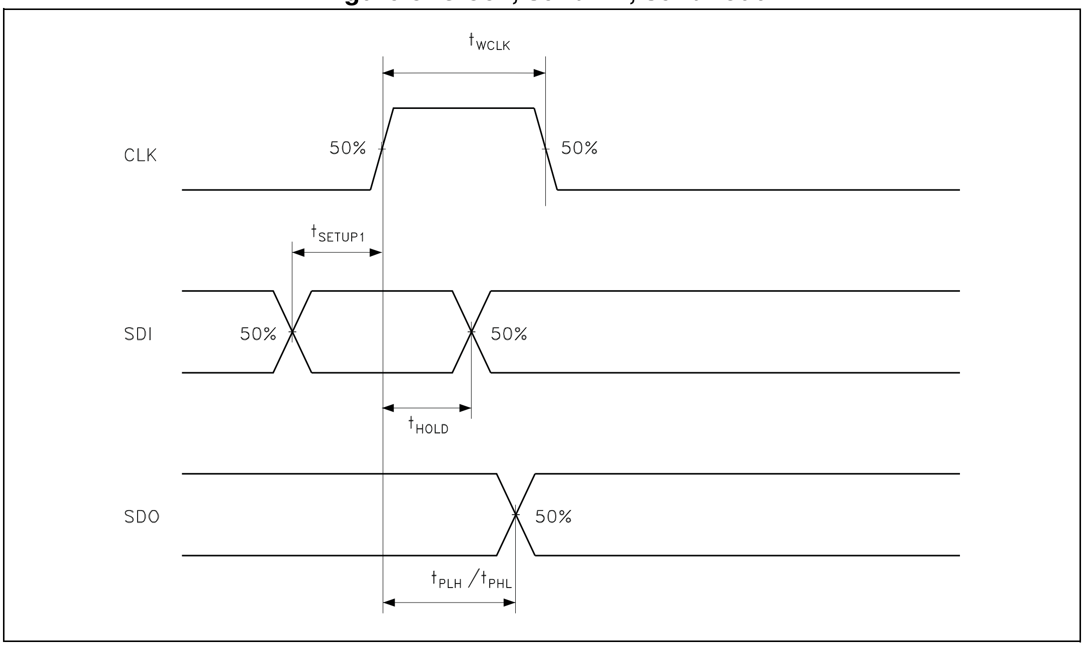


Figure 9. Clock, serial-in, latch, enable, outputs

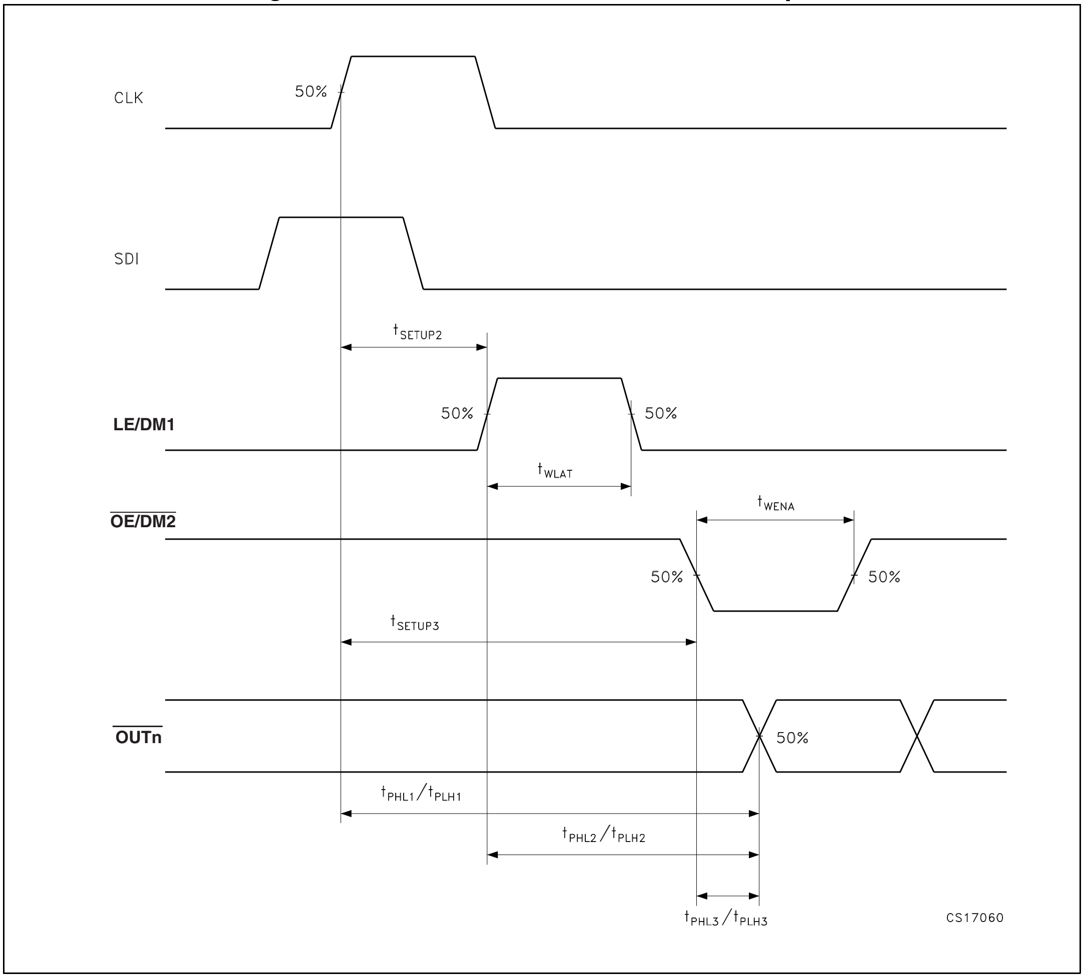
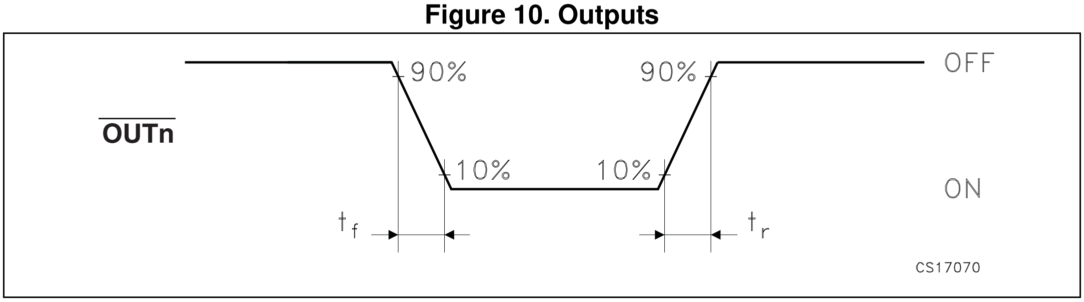


Figure 10. Outputs



6 Typical characteristics

Figure 11. Output current vs. R_{EXT} resistor

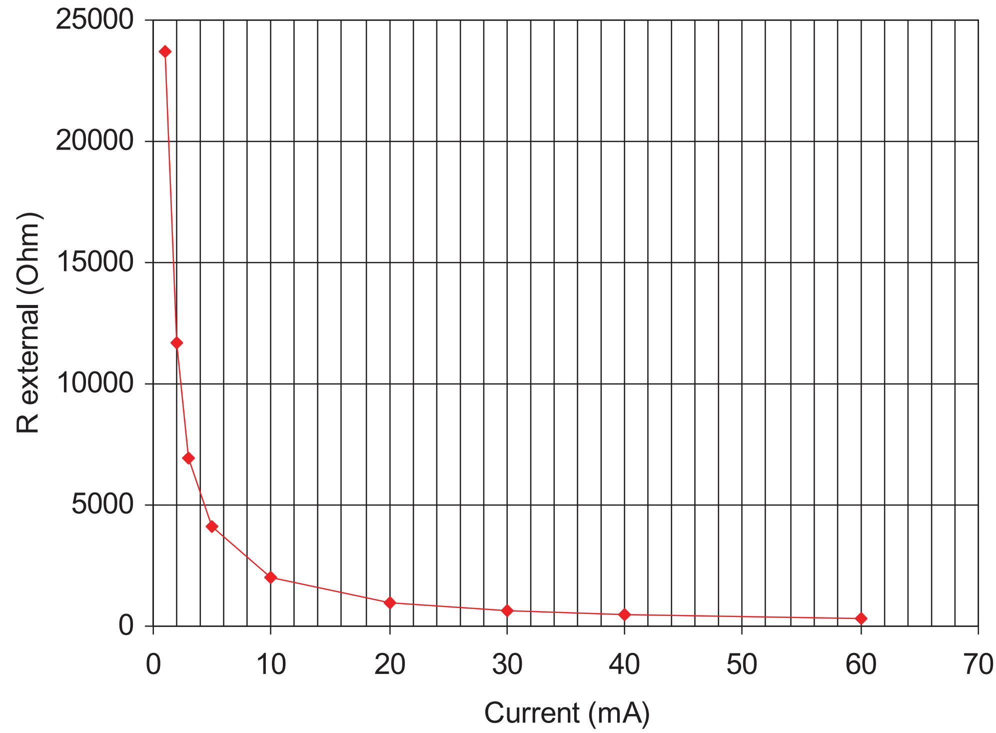


Table 11. Output current vs. R_{EXT} resistor

R_{EXT} (Ω)	Output current (mA)
23700	1
11730	2
6930	3
4090	5
2025	10
1000	20
667	30
497	40
331	60

Conditions:

– temperature = 25 °C, V_{DD} = 3.3 V; 5.0 V, I_{SET} = 3 mA; 5 mA; 10 mA; 20 mA; 50 mA; 60 mA.

Figure 12. I_{SET} vs. dropout voltage (V_{drop})

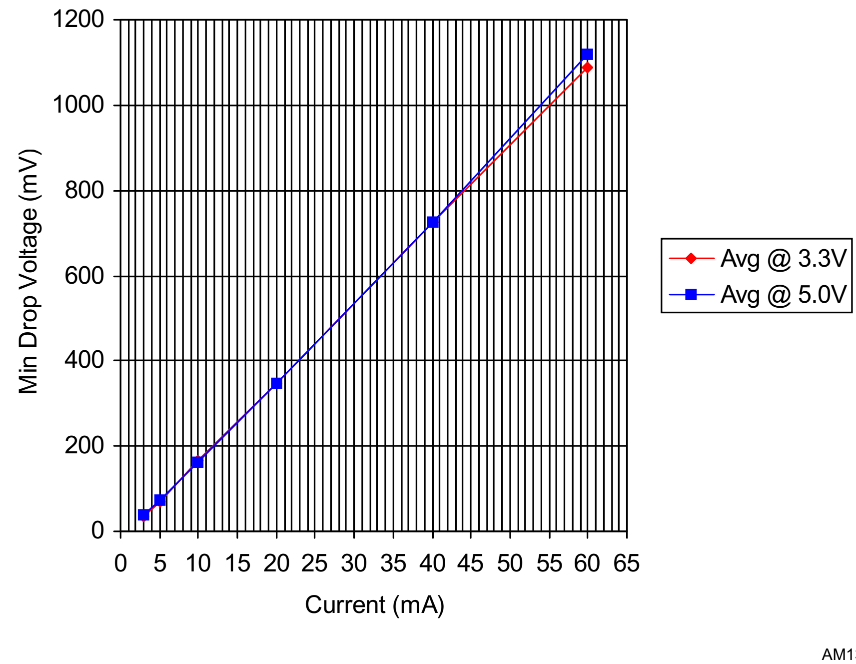


Table 12. I_{SET} vs. dropout voltage (V_{drop})

Iout (mA)	Avg (mV) @ 3.3 V	Avg (mV)@ 5.0 V
3	36	37
5	71	72
10	163	163
20	346	347
40	724	726
60	1080	1110

T_A = 25 °C, V_{DD} = 3.3 V; 5 V

Figure 13. Output current vs. ± ΔI_{OL}(%)

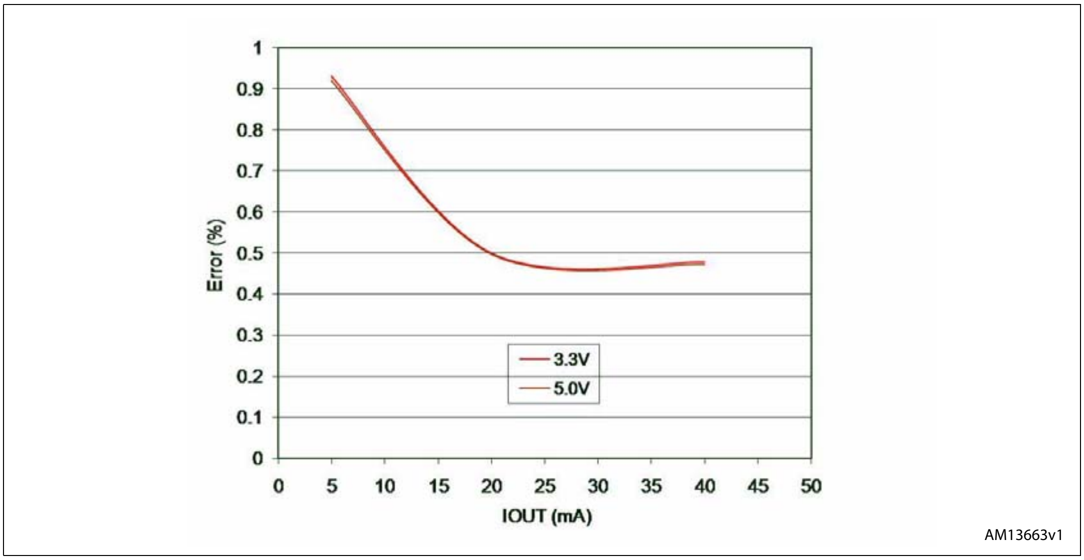


Figure 14. Idd ON/OFF

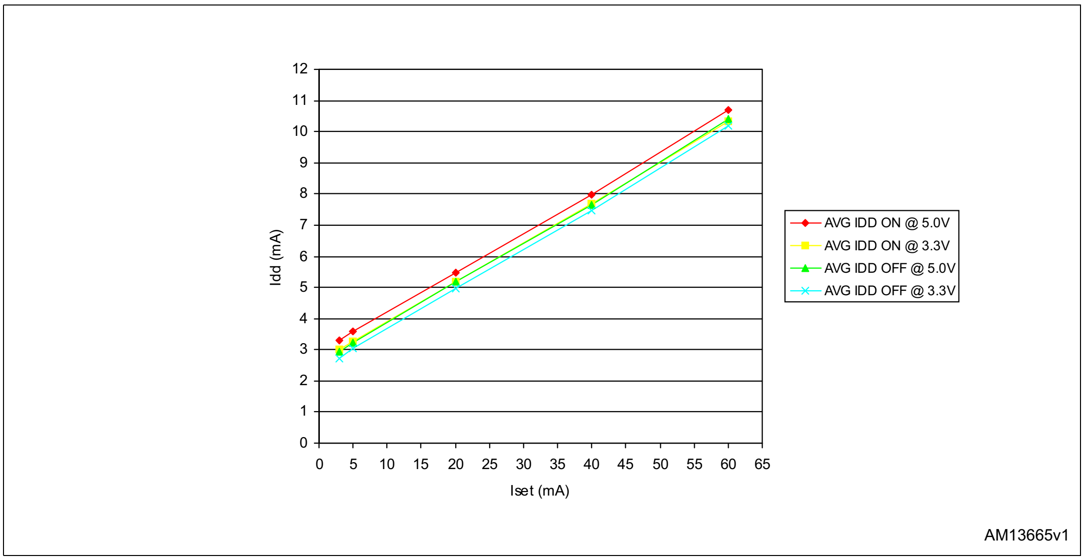
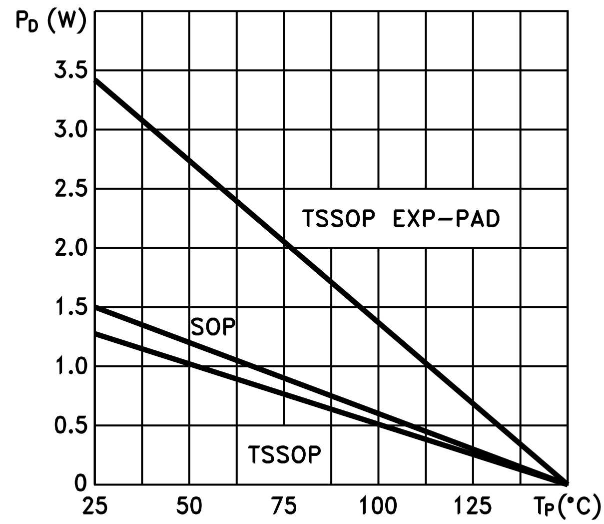


Figure 15. Power dissipation vs. package temperature



Note: The exposed pad should be soldered to the PCB to obtain the thermal benefits.

Figure 16. Turn-ON output current characteristics[1]

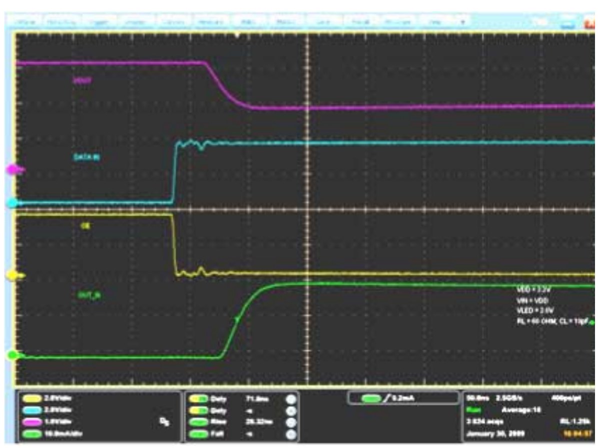
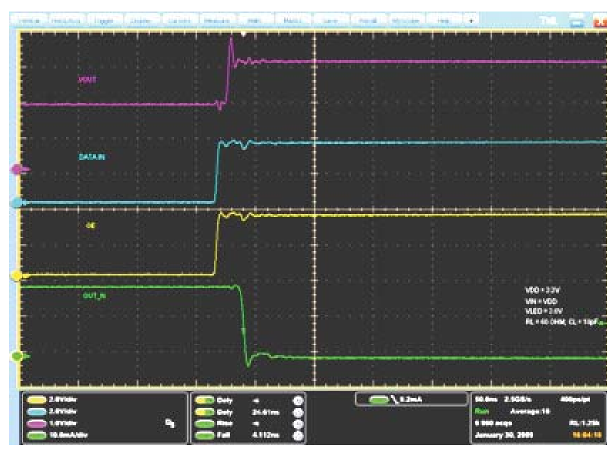


Figure 17. Turn-OFF output current characteristics[2]



1. The reference level for the T_{ON} characteristics is 50% of $\overline{\text{OE/DM2}}$ signal and 90% of output current
2. The reference level for the T_{OFF} characteristics is 50% of $\overline{\text{OE/DM2}}$ signal and 10% of output current

Electrical conditions:

- V_{DD} = 3.3 V, Vin = V_{DD}, Vled = 3.0 V, RL = 60 Ω, CL = 10 pF.
- Ch1 (yellow) = OE/DM2, Ch2 (blue) = SDI, Ch3 (purple) = VOUT, Ch4 (green) = OUT.

7 Error detection mode functionality

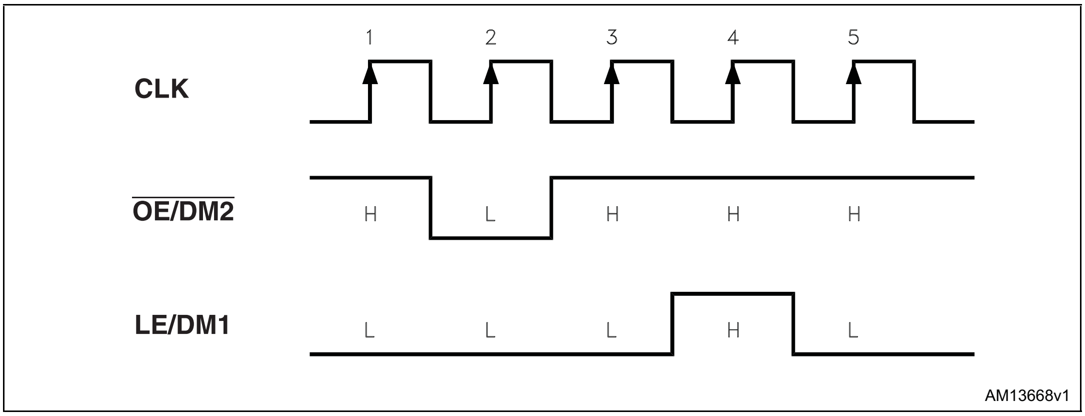
7.1 Phase one: entering error detection mode

From the "normal mode" condition the device can switch to "error mode" by a logic sequence on the $\overline{OE}$/DM2 and LE/DM1 pins, as shown in the following table and diagram:

Table 13. Entering error detection mode - truth table

CLK	1°	2°	3°	4°	5°
$\overline{OE}$/DM2	H	L	H	H	H
LE/DM1	L	L	L	H	L

Figure 18. Entering error detection mode - timing diagram

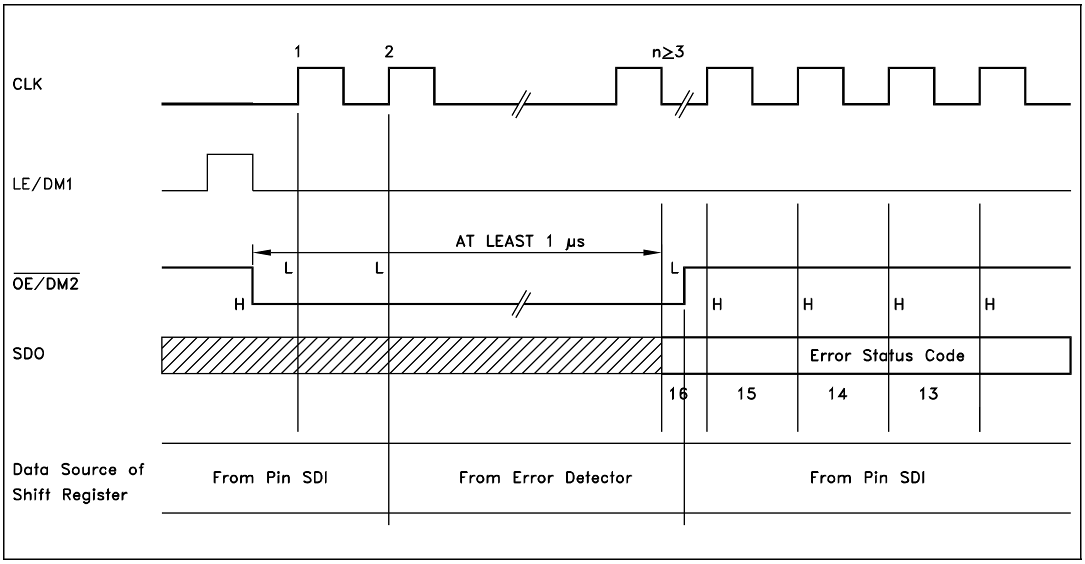


After these five CLK cycles, the device goes into the "error detection mode" and at the 6th rising edge of the CLK, the SDI data are ready for sampling.

7.2 Phase two: error detection

The 16 data bits must be set to “1” in order to set ON all the outputs during detection. The data are latched by LE/DM1 and after that the outputs are ready for the detection process. When the microcontroller switches the $\overline{OE/DM2}$ to LOW, the device drives the LEDs in order to analyze if an OPEN or SHORT condition has occurred.

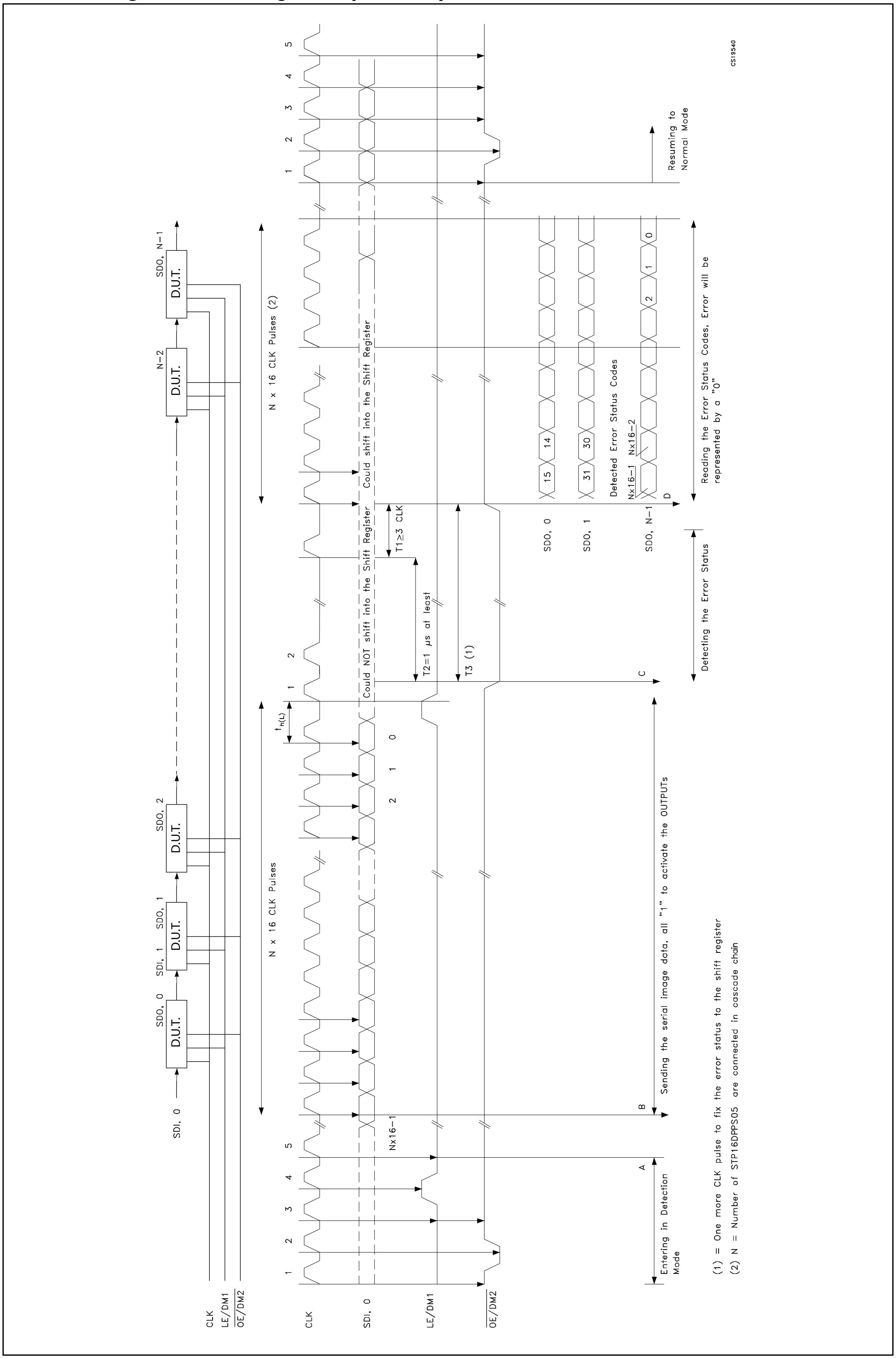
Figure 19. Detection diagram



The LED status is detected in 1 microsecond (minimum) and after this time the microcontroller sets $\overline{OE/DM2}$ in HIGH state and the output data detection results go to the microprocessor via SDO.

Detection mode and normal mode both use the same data format. As soon as all the detection data bits are available on the serial line, the device may go back to normal mode of operation. To re-detect the status, the device must go back in normal mode and re-enter error detection mode.

Figure 20. Timing example for open and/or short-circuit detection



7.3 Phase three: resuming normal mode

The sequence for re-entering normal mode is shown in the following table:

Table 14. Resuming normal mode - timing diagram

CLK	1°	2°	3°	4°	5°
$\overline{OE}$/DM2	H	L	H	H	H
LE/DM1	L	L	L	L	L

Note: For proper device operation, the "entering error detection" sequence must be followed by a "resume mode" sequence, it is not possible to insert consecutive equal sequences.

7.4 Error detection conditions

Table 15. Detection conditions (V_{DD} = 3.3 to 5 V, temperature range -40 to 125 °C)

Configuration	Detect mode	Detection results		
SW-1 or SW-3b	Open line or output short to GND detected	==> $I_{ODEC} \leq 0.5 \times I_O$	No error detected	==> $I_{ODEC} \geq 0.5 \times I_O$
SW-2 or SW-3a	Short on LED or short to V-LED detected	==> $V_O \geq 2.6$ V	No error detected	==> $V_O \leq 2.3$ V

Note: *Where:* I_O = the output current programmed by the R_{EXT}, I_{ODEC} = the detected output current in detection mode.

Figure 21. Detection circuit

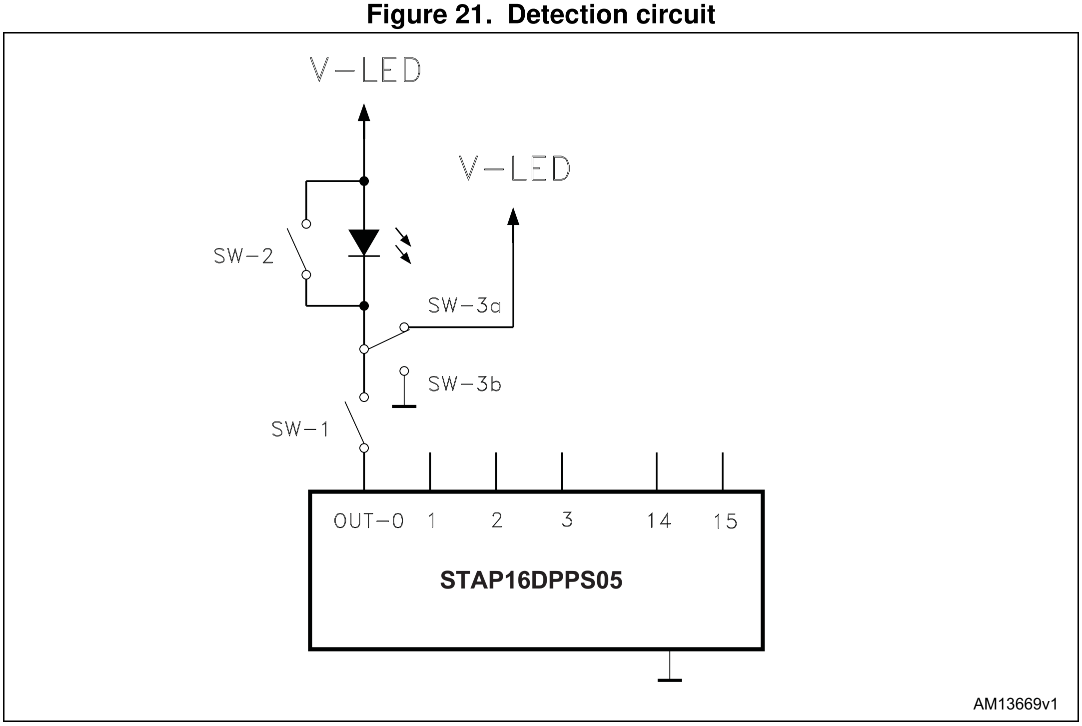
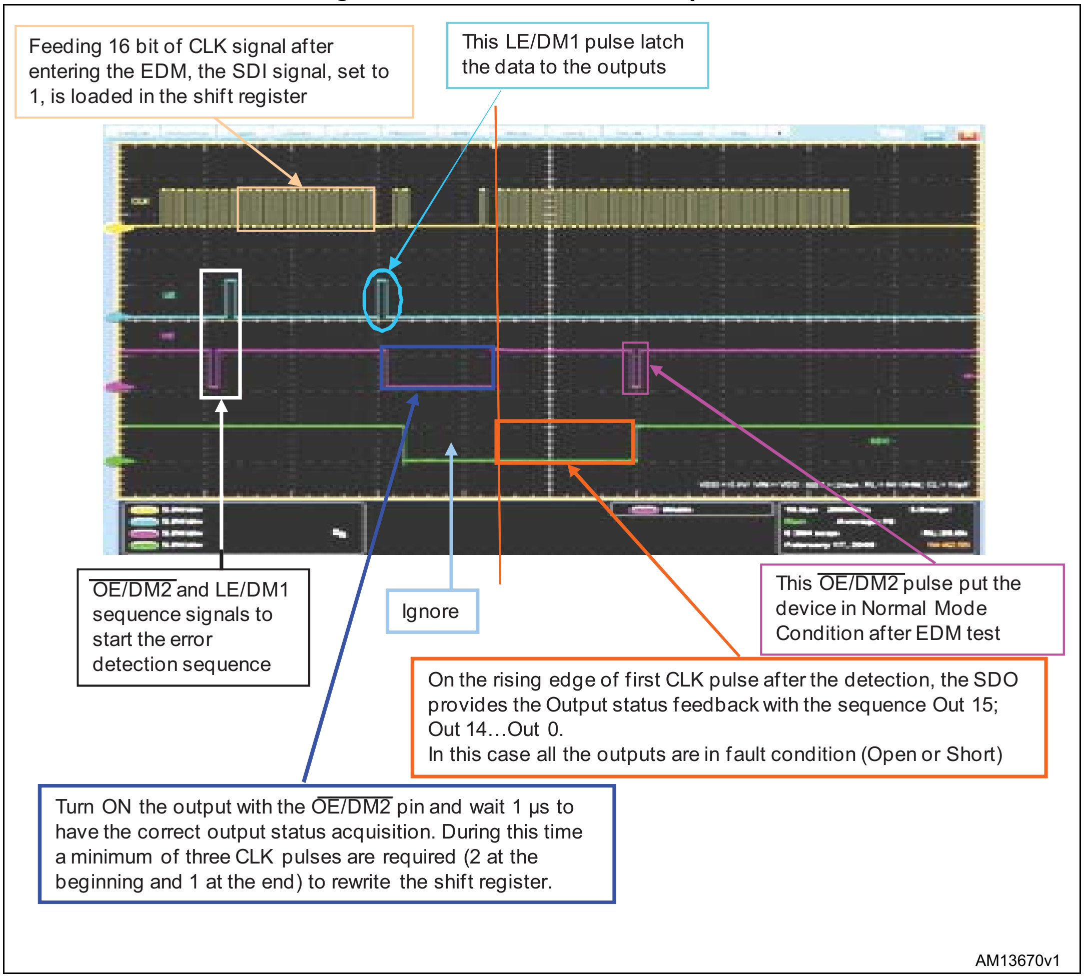


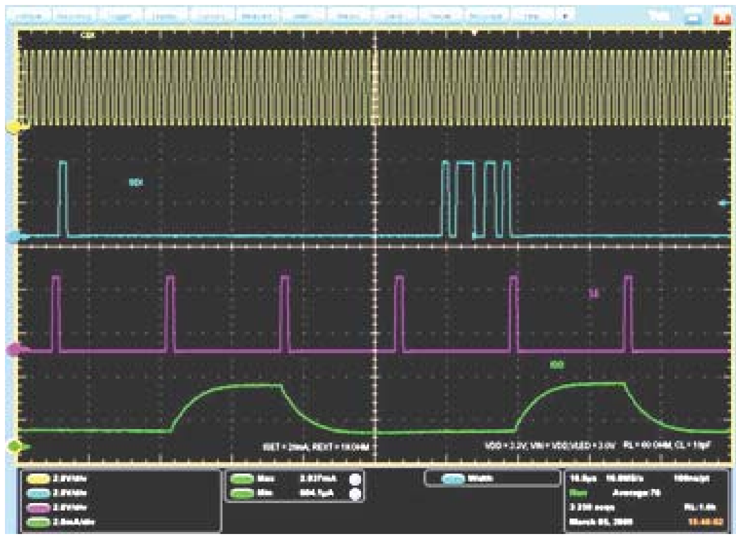
Figure 22. Error detection sequence



7.5 Auto power-saving

The auto power-saving feature minimizes the quiescent current if no active data is detected on the latches and auto powers-up the device as the first active data is latched.

Figure 23. Auto power-saving feature



AM13671v1

Conditions:

- Temp. = 25 °C, V_{DD} = 3.3 V, Vin = V_{DD}, VLed = 3.0 V, Iset = 20 mA.
- Ch1 (yellow) = CLK, Ch2 (blue) = SDI, Ch3 (purple) = LE/DM1, Ch4 (green) = IDD.

Idd consumption:

- Idd (normal operation) = 2.93 mA.
- Idd (shutdown condition) = 170 µA.