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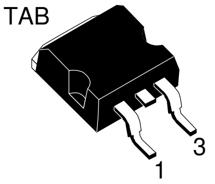
STB18N60DM2

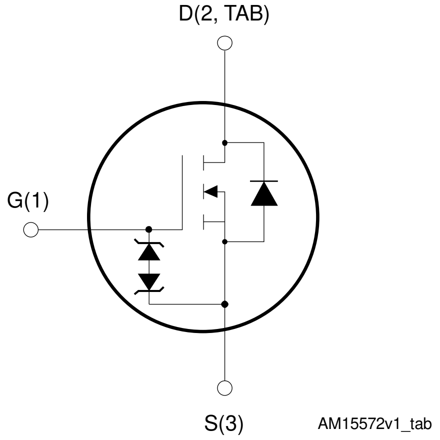
N-channel 600 V, 0.260 Ω typ., 12 A MDMesh™ DM2 Power MOSFET in a D²PAK package

Datasheet - production data



D²PAK

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB18N60DM2	600 V	0.295 Ω	12 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STB18N60DM2	18N60DM2	D²PAK	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	12	A
	Drain current (continuous) at T_{case}= 100 °C	7.6	
I_{DM} (1)	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	90	W
dv/dt (2)	Peak diode recovery voltage slope	40	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature	–55 to 150	°C
T_j	Maximum junction temperature	150	

Notes:

(1) Pulse width is limited by safe operating area.

(2) $I_{SD} \leq 12$ A, di/dt ≤ 400 A/µS, $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 80\% \; V_{(BR)DSS}$.

(3) $V_{DS} \leq 480$ V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.39	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	30	

Notes:

(1) When mounted on 1 a inch² FR-4, 2 Oz copper board

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Avalanche current, repetitive or not repetitive	2.5	A
E_{AR} (2)	Single pulse avalanche energy	380	mJ

Notes:

(1) Pulse width is limited by T_{jmax}.

(2) starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V.

2 Electrical characteristics

(T_{case}= 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1.5	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_{case} = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A		0.260	0.295	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	800	-	pF
C_{oss}	Output capacitance		-	40	-	
C_{rss}	Reverse transfer capacitance		-	1.33	-	
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, f = 1 MHz, V_{GS} = 0 V	-	80	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	5.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 12 A, V_{GS} = 10 V (see *Figure 14: "Gate charge test circuit"*)	-	20	-	nC
Q_{gs}	Gate-source charge		-	5.2	-	
Q_{gd}	Gate-drain charge		-	8.5	-	

Notes:

(1) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 6 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Switching times test circuit for resistive load"* and *Figure 18: "Switching time waveform"*)	-	13.5	-	ns
t_r	Rise time		-	8	-	
$t_{d(off)}$	Turn-off-delay time		-	9.5	-	
t_f	Fall time		-	32.5	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM}(1)	Source-drain current (pulsed)		-		48	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 12 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	125		ns
Q_{rr}	Reverse recovery charge		-	0.675		nC
I_{RRM}	Reverse recovery current		-	11		A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	190		ns
Q_{rr}	Reverse recovery charge		-	1225		nC
I_{RRM}	Reverse recovery current		-	13		A

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

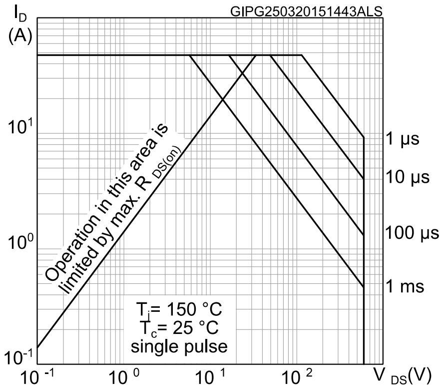


Figure 3: Thermal impedance

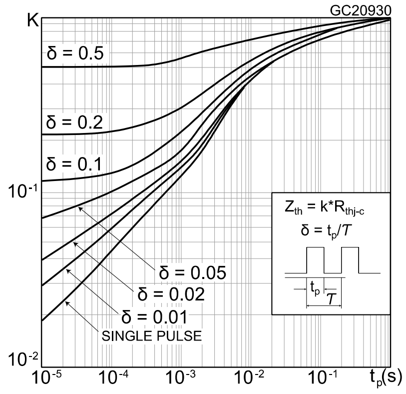


Figure 4: Output characteristics

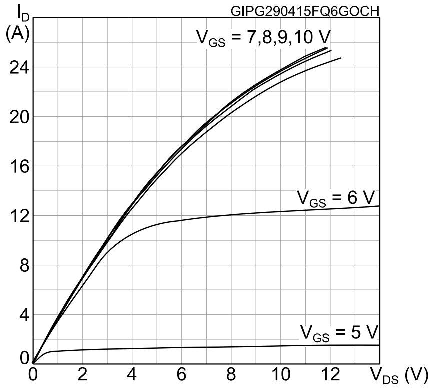


Figure 5: Transfer characteristics

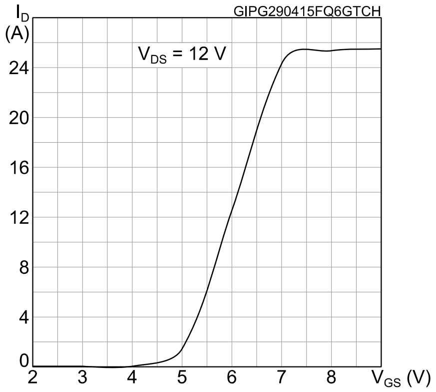


Figure 6: Gate charge vs gate-source voltage

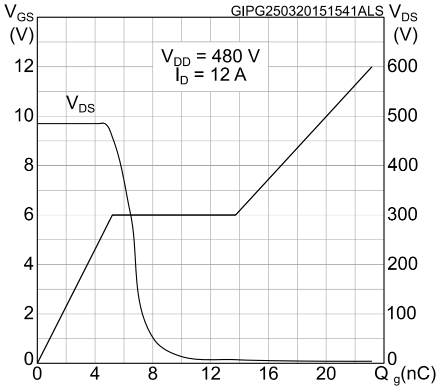


Figure 7: Static drain-source on-resistance

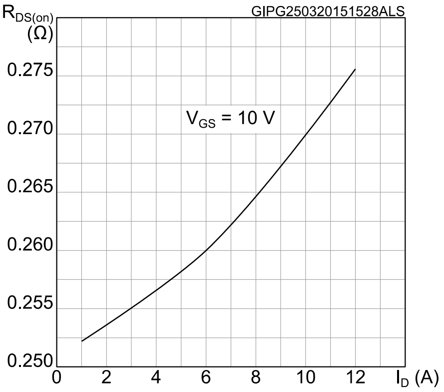


Figure 8: Capacitance variations

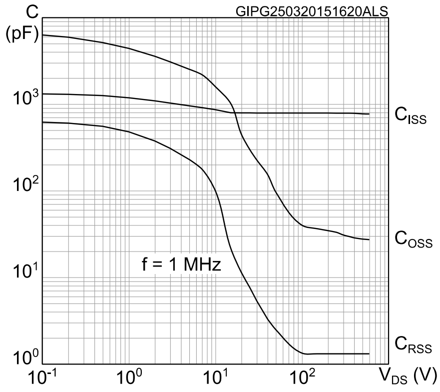


Figure 9: Normalized gate threshold voltage vs temperature

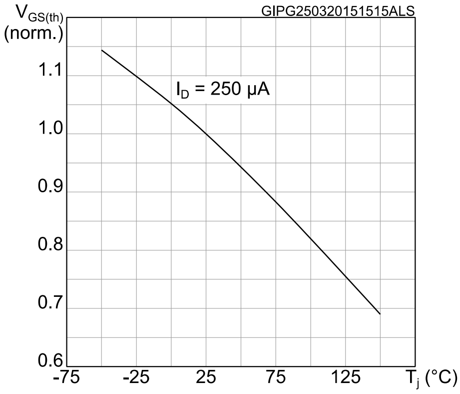


Figure 10: Normalized on-resistance vs temperature

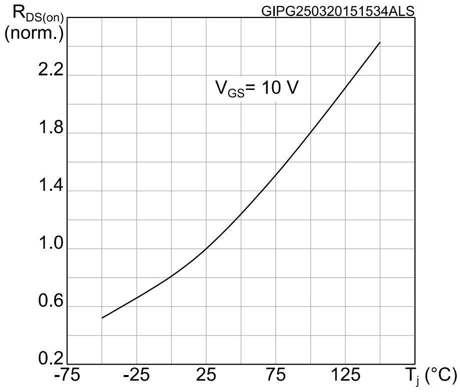


Figure 11: Normalized V(BR)DSS vs temperature

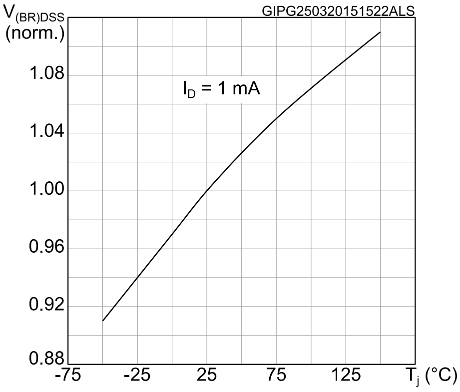
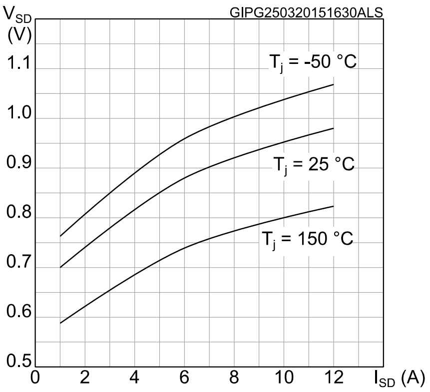


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

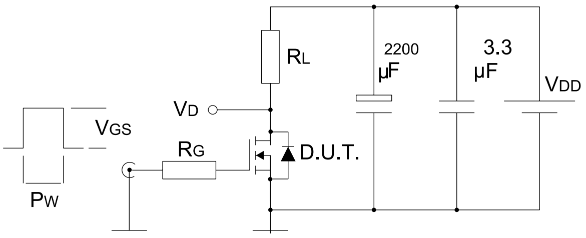


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Figure 14: Gate charge test circuit

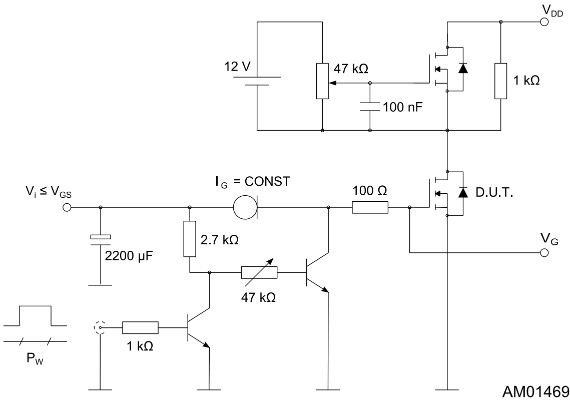

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Figure 15: Test circuit for inductive load switching and diode recovery times

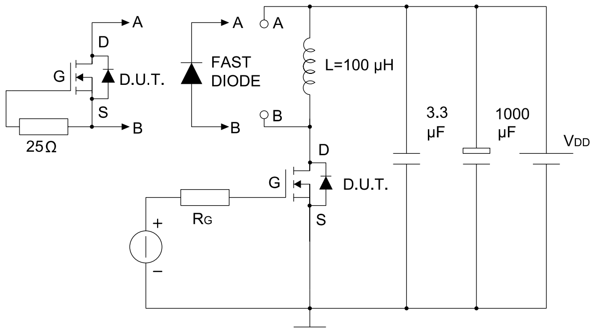

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Figure 16: Unclamped inductive load test circuit

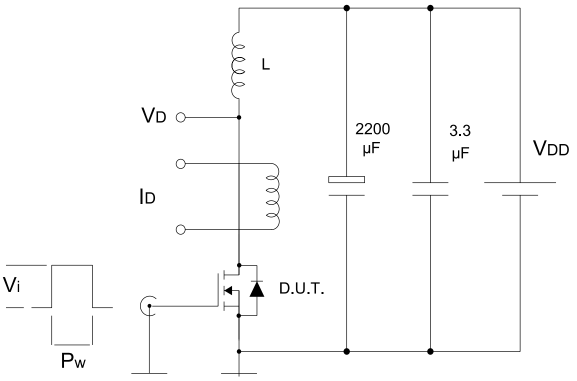

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Figure 17: Unclamped inductive waveform

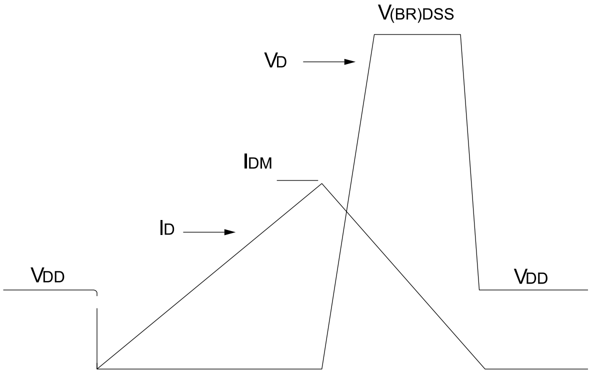

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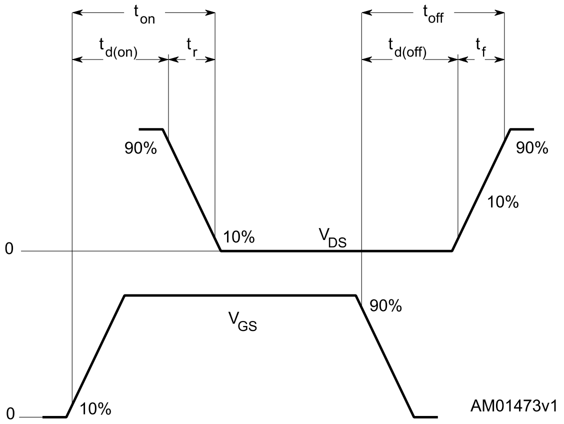
Figure 18: Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 D²PAK_(TO-263)_type_A_package information

Figure 19: D²PAK (TO-263) type A package outline

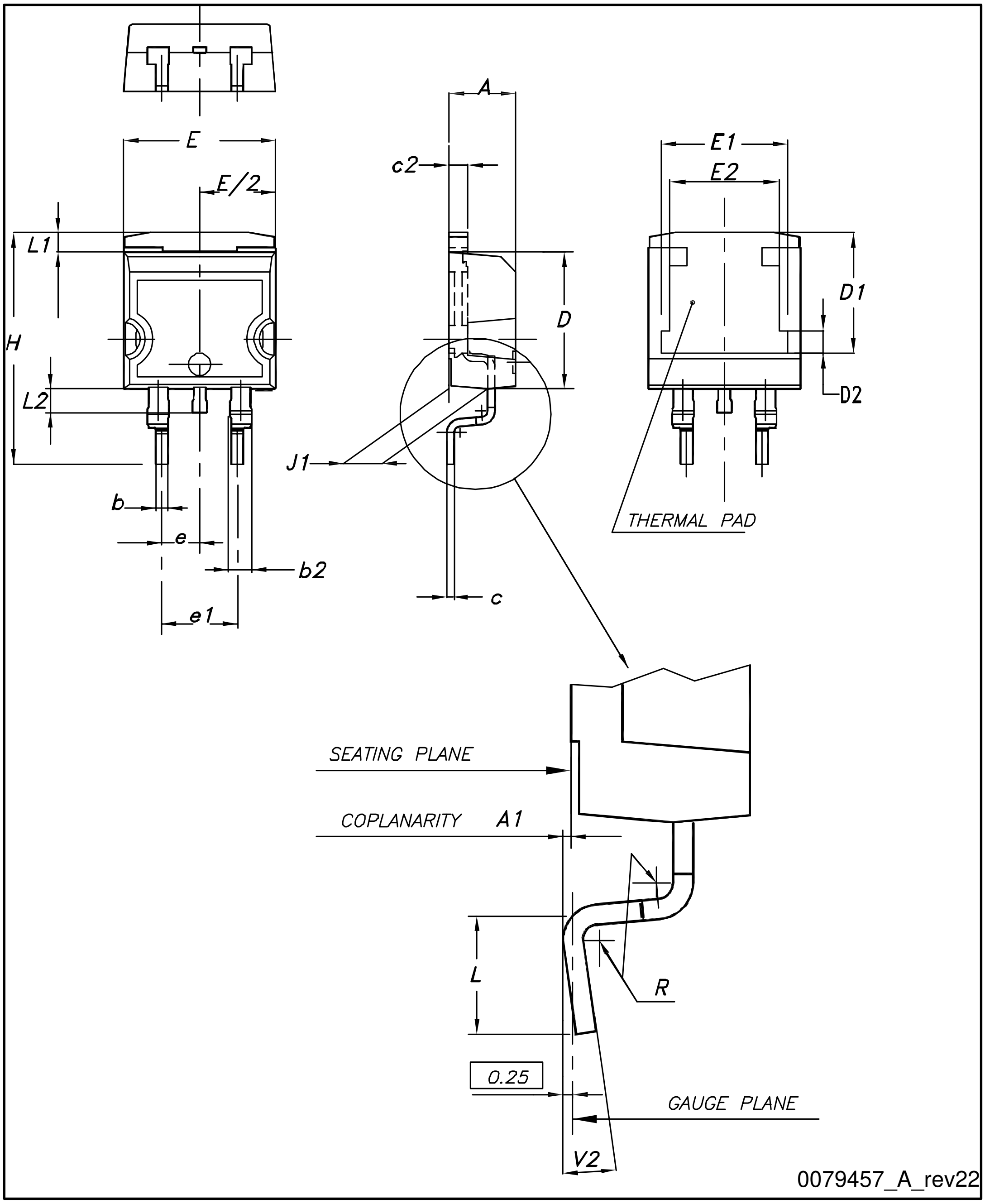
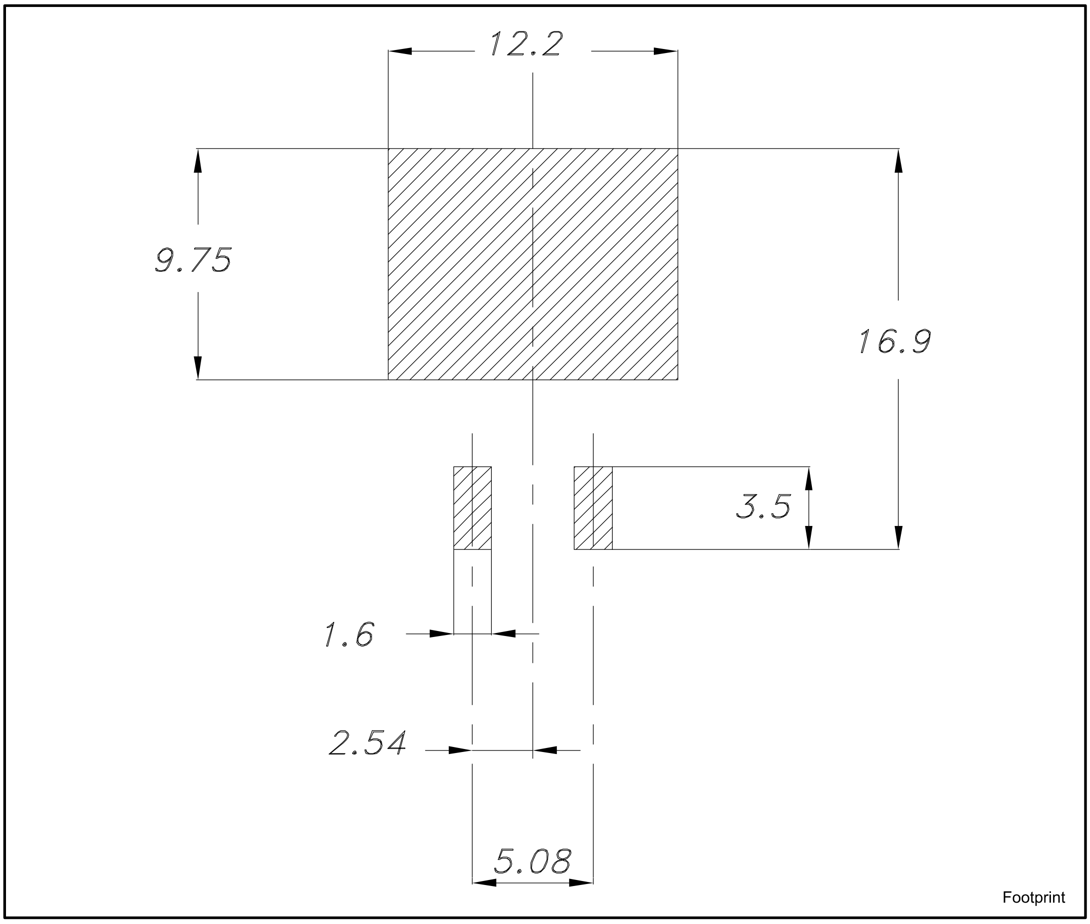


Table 9: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20: D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 D^{2}PAK packing information

Figure 21: Tape oultine

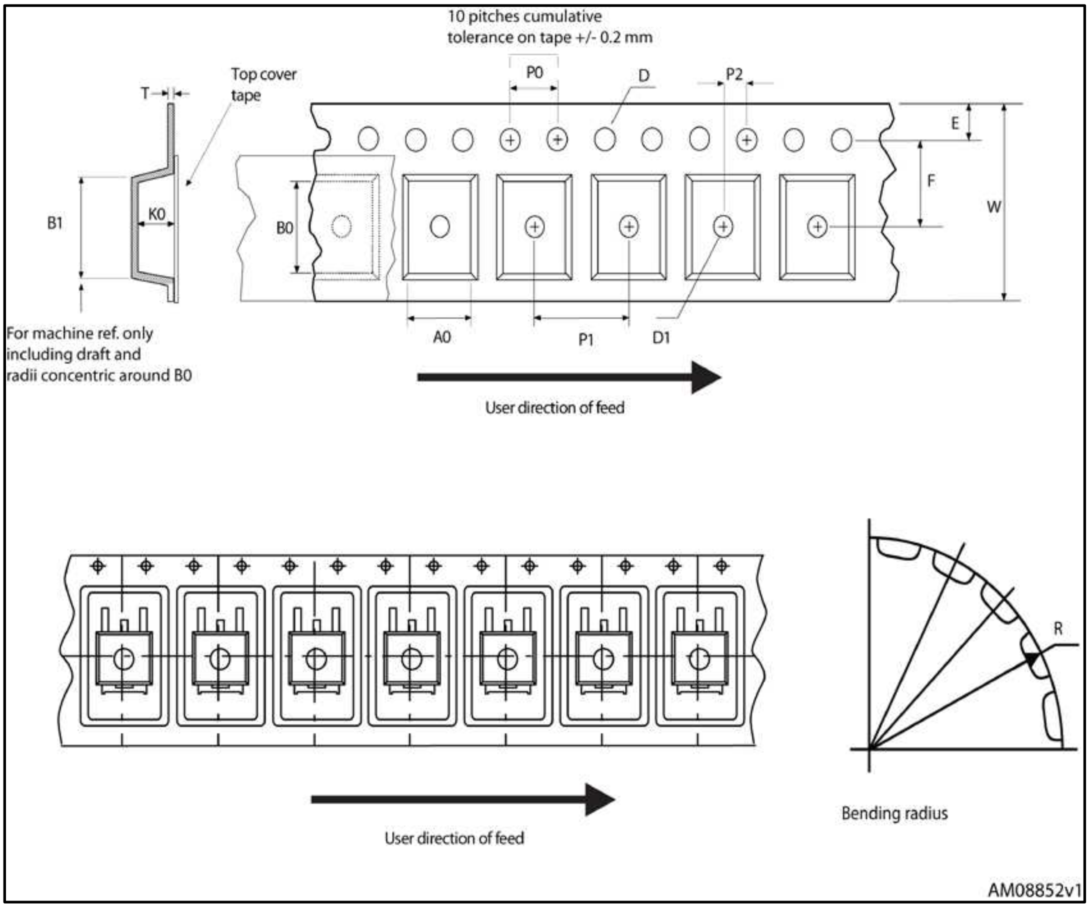


Figure 22: Reel outline

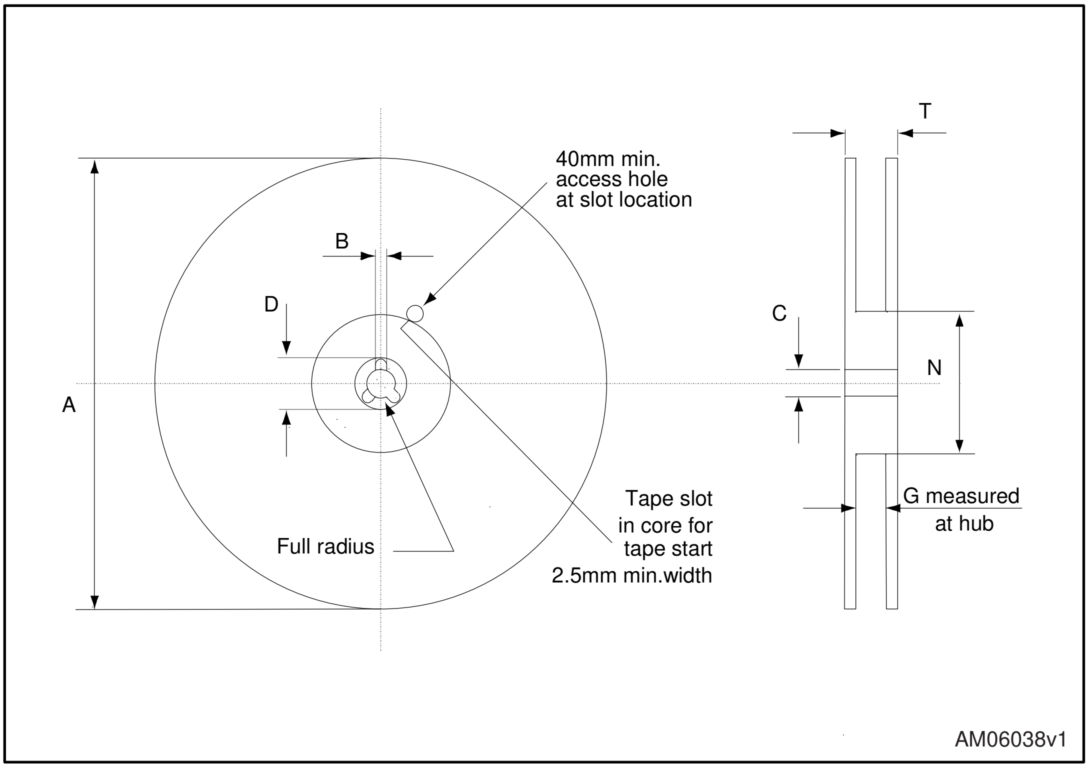


Table 10: D^{2}PAK tape and reel mechanical data

Tape			Reel		
Dim.	**mm**		**Dim.**	**mm**	
	Min.	**Max.**		**Min.**	**Max.**
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
01-Apr-2015	1	First release.
20-May-2015	2	Text edits and formatting changes throughout document In Section 2.1 Electrical characteristics (curves): - updated Figure 4: Output characteristics - updated Figure 5: Transfer characteristics

IMPORTANT NOTICE – PLEASE READ CAREFULLY