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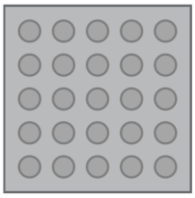
STBCFG01

Switch mode single cell Li+ battery charger with OTG boost, voltage mode fuel gauge and LDO

Datasheet - production data



Flip Chip 25 (2.3 x 2.2 mm)

Features

- High efficiency switching battery charger
  - 2 MHz or 3 MHz switching frequency
  - 1.2 A max. charging current
  - 20 V tolerant input with OVP
  - Programmable input current limitation and dynamic input current limit
  - Battery overvoltage protection
  - Auto-recharge
  - Integrated current sensing resistor
  - USB compatible
- Voltage mode fuel gauge
  - External sensing resistor is not needed
  - Battery swap detection through ID resistor
  - Low battery voltage and low SOC programmable alarms
- 50 mA LDO for system boot in dead battery condition
- USB OTG V_{BUS} generation (500 mA)
  - USB overvoltage protection
  - Programmable battery overcurrent protection
- Automatic 60 mA input pre-bias
- I^2C compatible control interface
- Interrupt output pin
- Flip Chip package, 25 bumps (2.3 x 2.2 mm)

Applications

- Mobile phones
- Smart phones

Description

The STBCFG01 is a switching battery charger integrating the necessary functions to charge single cell Li-Ion batteries, monitor the battery charge and generate 5 V to supply USB OTG bus powered devices.

The IC also integrates the LDO regulator to support system boot in dead battery conditions.

The battery charger features a smart input current limit: the maximum input current can be selected through I^2C and if the input voltage drops below a programmable threshold, the input current is reduced even if the selected maximum current limit has not been reached yet. The dynamic input current limit can be disabled.

An automatic input pre-bias load makes the device suitable for applications using voltage sources with a minimum external load for the right regulation.

The STBCFG01 also integrates a voltage mode fuel gauge to provide the state of charge evaluation without the current sensing resistor.

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1 Application schematic

Figure 1: STBCFG01 application schematic

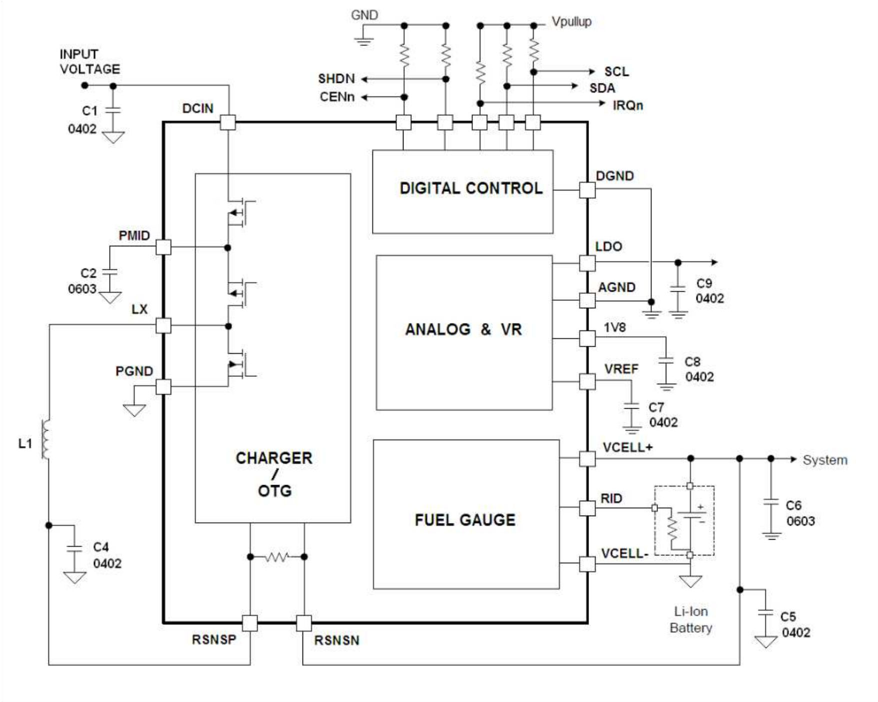


Table 1: Typical bill of material (BOM)

Component name	Size	Value	Supplier	Part number
C1	0603	10 µF, 16 V	MURATA	GRM188R61C106MA73D
C2	0603	4.7 µF, 25 V	TDK	C1608X5R1E475K080AC
C3	0402	1 µF, 16 V	MURATA	GRM155R61C105KA12D
C4	0603	4.7 µF, 25 V	TDK	C1608X5R1E475K080AC
C5	0603	1 µF, 16 V	MURATA	GRM185R61C105KE44
C6	0603	10 µF, 16 V	MURATA	GRM188R61C106MA73D
C7	0603	100 nF, 25 V	MURATA	GRM188R71H104KA93
C8	0603	1 µF, 16 V	MURATA	GRM185R61C105KE44
C9	0603	1 µF, 16 V	MURATA	GRM185R61C105KE44
L1	2.5 x 2.2 mm	1 µH, 2.2 A	TDK	VLS252012ET-1R0N

2 Pin configuration

Figure 2: Pin connections (top view)

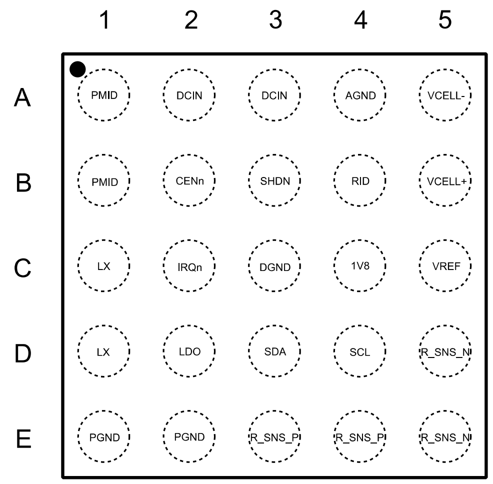


Table 2: Pin description

Symbol	Ball	Pin function	Description
PMID	A1, B1	Power I/O	Reverse blocking MOSFET to high-side connection node
DCIN	A2, A3	Power I/O	Input supply voltage/OTG output
AGND	A4	Analog ground	Analog ground
VCELL-	A5	Analog input	Battery pack negative terminal sense input
CENn	B2	Digital input	Charger enable, active low. Internal 200 kΩ pull-down to GND
SHDN	B3	Digital input	Shutdown input, active high. Internal 200 kΩ pull-down to GND
RID	B4	Analog input	Battery identification resistor connection (for battery detection). An external bias has to be applied
VCELL+	B5	Analog input	Battery pack positive terminal sense input
LX	C1, D1	Power I/O	Switch mode, inductor connection
IRQn	C2	Digital input	Open drain interrupt output, active low
DGND	C3	Digital ground	Digital ground
1V8	C4	Analog out	1.8 V internal regulator bypass pin. Bypass this pin to GND with a capacitor of 220 nF. Do not connect any load
VREF	C5	Analog out	Reference voltage bypass pin. Do not connect any load
LDO	D2	Analog out	4.85 V LDO output
SDA	D3	Digital I/O	I²C data pin to the baseband, I²C master peripheral
SCL	D4	Digital input	I²C clock pin to the baseband, I²C master peripheral
R_SNS_N	D5, E5	Power I/O	Internal sense resistor, negative terminal

Symbol	Ball	Pin function	Description
PGND	E1, E2	Power ground	Power ground
R_SNS_P	E3, E4	Power I/O	Internal sense resistor, positive terminal

3 Maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DCIN}, V_{PMID}	Charger input voltage	-1.5 to +20	V
V_{LX}	Switch mode voltage	-0.3 to +8	V
VCELL+, $R_{\_SNS\_N}$, $R_{\_SNS\_P}$	Battery pin	-0.3 to +6	V
V_{VREF}, V_{V1V8}, V_{CENn}, V_{SHDN}	Low voltage pins	-0.3 to +2.1	V
V_{AMR}	All other input voltage pins	-0.3 to +5.5	V
ESD	Human body model	±2000	V
	Charged device model	±250	V
T_{AMB}	Operating ambient temperature	-30 to +85	°C
T_J	Maximum junction temperature	+125	°C
T_{STG}	Storage temperature	-65 to +150	°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4: Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case	TBD	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	TBD	°C/W

4 Electrical characteristics

T_J = -30 °C to +85 °C, V_{BAT} = 3.6 V, V_{DCIN} = 5 V unless otherwise specified.

Table 5: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General information						
VIN	DCIN input voltage range		3.78		5.95	V
f_{SW}	Switching frequency	FSW bit = 0		2		MHz
		FSW bit = 1		3		
T_{SD}	Thermal shutdown threshold			165		°C
	Hysteresis			20		
t_{TSD}	Thermal shutdown deglitch time			50		µs
Battery charger						
I_{IN}	Current consumption from DCIN	Charger enabled, switching, V_{BUS_CON} = 5 V		14		mA
		Shutdown, LDO disabled		290	400	µA
		Shutdown, LDO enabled		500	800	µA
I_{BAT}	Current consumption from BAT(including fuel gauge)	On battery power VBUS_CON = 0 V GG_RUN = 0		10	25	µA
		On battery power VBUS_CON = 0 V GG_RUN = 1		32	100	µA
V_{INOVP}	DCIN overvoltage protection	V_{DCIN} rising	6.05	6.3	6.62	V
		V_{DCIN} falling	5.95	6.2	6.51	
V_{INOVP_PB}	Pre-bias overvoltage protection	V_{DCIN} rising		7.0		V
		V_{DCIN} falling		6.9		V
	Pre-bias OVP accuracy		-5		+5	%
V_{INUVLO}	DCIN undervoltage lockout	V_{DCIN} rising		3.6		V
		V_{DCIN} falling		3.5		
	DCIN UVLO accuracy		-5		+5	%
I_{PREB}	Pre-bias current			60		mA
t_{PBD}	Pre-bias current enable deglitch time	V_{DCIN} rising over V_{INOVP} but below V_{INOVP_PB}		5		ms
t_{HDO}	Hold-off time	Valid DCIN connection to charging start		200		ms

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ASD}	Automatic shutdown threshold	$V_{ASD} = V_{DCIN}-V_{BAT}$, V_{DCIN} rising		130		mV
		$V_{ASD} = V_{DCIN}-V_{BAT}$, V_{DCIN} falling	0	36		mV
t_{ASD}	Automatic shutdown threshold deglitch time			50		µs
I_{INLIM}	D_{CIN} current limit	I_{LIM} configurable by I^2C		90		mA
				476		
				760		
				1140		
V_{DICL}	Dynamic input current limit threshold	DICL configurable by I^2C (4.0 V, 4.25 V, 4.5 V, 4.75 V)	4.0		4.75	V
	DICL accuracy		-3		+3	%
t_{DICL}	DICL activation deglitch time			100		ms
V_{FLOAT}	CV regulation voltage	$V_{BUS\_CON} = 5$ V	3.52		4.78	V
	CV regulation voltage accuracy	$V_{BUS\_CON} = 5$ V	-1		+1	%
V_{FLD}	CC to CV threshold deglitch time			170		ms
V_{RCHG}	Auto-recharge threshold voltage	ARCHG bit = 1		V_{FLOAT}-0.12		V
	Auto-recharge threshold accuracy	ARCHG bit = 1	-17		+17	%
t_{RCHG}	Auto-recharge threshold deglitch time	ARCHG bit = 1		170		ms
V_{BATOVP}	Battery overvoltage protection	This is got by increasing the battery voltage until BATOVP status register turns on		V_{FLOAT}+0.1		V
	Battery OVP accuracy		-10		+10	%
t_{BOVP}	Battery OVP deglitch time			170		ms
I_{TRK}	Trickle charge current	$V_{BAT}<V_{TRK}$		45		mA
	Trickle charge current accuracy		-20		+20	%
I_{PRE}	Pre-charge current	$V_{TRK}< V_{BAT}<V_{PRE}$		450		mA
	Pre-charge current accuracy		-10		+10	%
I_{FAST}	Fast charge current	$V_{BAT}> V_{PRE}$	550		1250	mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	Fast charge current accuracy		-10		10	%
I_{TERM}	Termination current		50		300	mA
	Termination current accuracy		-30		30	%
t_{TERM}	Charge termination deglitch time			170		ms
V_{TRK}	Trickle charge to pre-charge battery voltage threshold			2		V
	VTRK accuracy		-5		+5	%
t_{TPD}	Trickle charge to pre-charge threshold deglitch time			100		ms
V_{PRE}	Pre-charge to fast charge battery voltage threshold			3		V
	V_{PRE} accuracy		-5		+5	%
t_{PFD}	Pre-charge to fast charge threshold deglitch time			170		ms
V_{DETH}	Battery detection high threshold			3		V
V_{DETL}	Battery detection low threshold			2		V
I_{DETSNK}	Sink detection current			-5		mA
t_{DETSRC}	Current source detection time			340		ms
t_{DETSNK}	Current sink detection time			200		ms
R_{ON_HI}	High-side MOSFET on- resistance (including reverse blocking MOFET)			300		mΩ
R_{ON_LOW}	Low-side MOSFET on- resistance			125		mΩ
R_{SNS}	Internal sensing resistor			35	68	mΩ
t_{MAXPRE}	Maximum pre-charge time	Including trickle charge		45		min.
t_{MAXCHG}	Maximum fast charge time	Including taper charge		360		min.
OTG boost regulator						
I_{BQ}	Boost quiescent current	V_{BAT} = 3.7 V, no load		4		mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BUS}	Output voltage at V_{BUS_CON}		4.75	5	5.25	V
I_{VBUS}	Output current capability	$V_{BUS} \geq 4.75$ V	500			mA
$V_{BATUVLO}$	Battery undervoltage lockout	Falling edge		3		V
	Accuracy		-5		+5	%
V_{BUSOVP}	Output overvoltage protection			6		V
	Accuracy		-5		+5	%
$t_{VBUSOVP}$	V_{BUSOVP} deglitch time			30		ms
I_{BATLIM}	Battery average current limitation		350		950	mA
	Accuracy		-10		+10	%
I_{LMAX}	Cycle-by-cycle limitation			1.2		A
Z_0	Output impedance in OFF mode		100			kΩ
LDO output						
VLDO	LDO output voltage	I_{LDO} = 50 mA, V_{DCIN}- V_{LDO}>300 mV		4.85		V
	Accuracy		-4		+4	%
I_{LDO}	LDO output current	V_{DCIN}- V_{LDO} > 300 mV	50			mA
I_{SC}	LDO short-circuit current	$V_{LDO} \leq 4$ V		75		mA
	Accuracy		-27		+27	%
V_{DO}	LDO dropout voltage	I_{LDO} = 50 mA		150	300	mV
V_{INMIN}	LDO input undervoltage lockout	V_{DCIN} rising		3.6		V
		V_{DCIN} falling		3.5		
	V_{INMIN} accuracy		-5		+5	%
V_{INMAX}	LDO input overvoltage lockout	V_{DCIN} rising		6.3		V
		V_{DCIN} falling		6.2		
	V_{INMAX} accuracy		-5		+5	%
Fuel gauge						
I_{FGQ}	Fuel gauge quiescent current	GG_RUN = 1		25		µA
		GG_RUN = 0		2		
UVLO	Fuel gauge undervoltage lockout	Rising edge	2.0	2.6	2.7	V
	Hysteresis			100		mV
f_{OSC}	Internal time base frequency			512		kHz
	Time base accuracy			1		%

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{STRB}	ADC conversion strobe			4		s
t_{SWAP}	Battery swap deglitch time			1		s
V_{BATERR}	V_{BAT} measurement error		-0.5		+0.5	%
V_{BATRES}	VBAT measurement resolution	OCV reading		2.69		mV
V_{BATRNG}	VBAT measurement range		2.5		5.5	V
V_{RIDTH}	RID threshold		1.2	1.25	1.3	V
	Hysteresis			0.130		V
I²C compatible interface						
V_{IH}	High level input voltage		1.3			V
V_{IL}	Low level input voltage				0.6	V
V_{OL}	Low level output voltage at 10 mA sink current for open drain I/O				0.3	V
C_{IO}	I/O pin capacitance				10	pF
f_{SCL}	SCL clock frequency				400	kHz
t_{LOW}	Minimum clock low period		1.3			µs
t_{HIGH}	Minimum clock high period		600			ns
t_F	SDA and SCL fall time				300	ns
t_{HOLD_STA}	Start condition hold time		600			ns
t_{SU_STA}	Start condition set-up time		600			ns
t_{SU_DAT}	Data set-up time		100			ns
t_{HOLD_DAT}	Data hold time		0			µs
t_{SU_STO}	Stop condition set-up time		600			ns
t_{BUF}	Minimum delay between operations		1.3			µs
Digital interface						
V_{IH}	Input high threshold		1.3			V
V_{IL}	Input low threshold				0.6	V
V_{OL}	Output low threshold				0.3	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{IN_IO}	I/O pin input current		-10		+10	µA

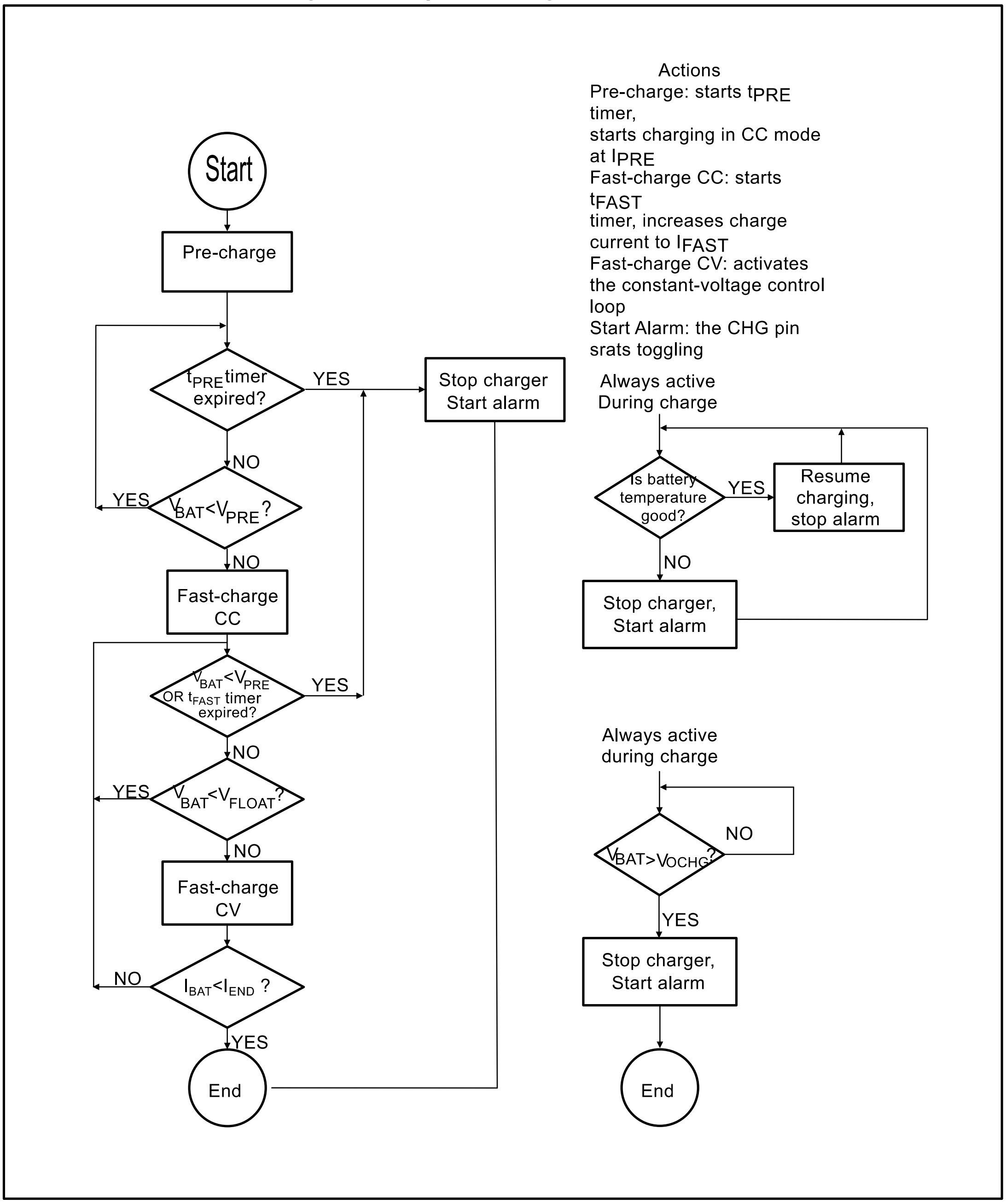
Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.

5 Operation description

5.1 Battery charger

The STBCFG01 integrates a high efficiency battery charger of 1.2 A implementing the CC/CV charging algorithm for single cell Li-Ion battery powered applications. The switching frequency can be either 2 MHz or 3 MHz, according to platform noise requirements, and the inductor value is 1 µH. The charging current sensing resistor is integrated.

Figure 3: Simplified charger architecture



When the battery is deeply discharged (VCELL+ < V_{TRK}, V_{TRK} = 2 V) the device is in trickle charge mode and charges the battery in linear mode with a low current (I_{TRK} = 45 mA) up to the trickle charge threshold.

As soon as the battery voltage enters the pre-charge range (V_{TRK} < V_{CELL+} < V_{PRE}, V_{PRE} = 3 V) the device starts the switch mode charging and increases the charging current up to the pre-charge current level (I_{PRE}) to make the system voltage rise quickly up to a level which allows the system to wake up.

The typical value for the pre-charge current is 450 mA but this value can be decreased to 100 mA through the I²C compatible interface.

A 45 minute (typ.) safety timer is active during both trickle charge and pre-charge.

When the battery voltage is above the pre-charge threshold, the STBCFG01 enters fast charge mode and increases the charging current up to IFAST value. The fast charge current can be programmed through the I²C compatible interface between 550 mA and 1.2 A in 100 mA steps.

A soft-start function makes the battery current increase smoothly when the charging current changes.

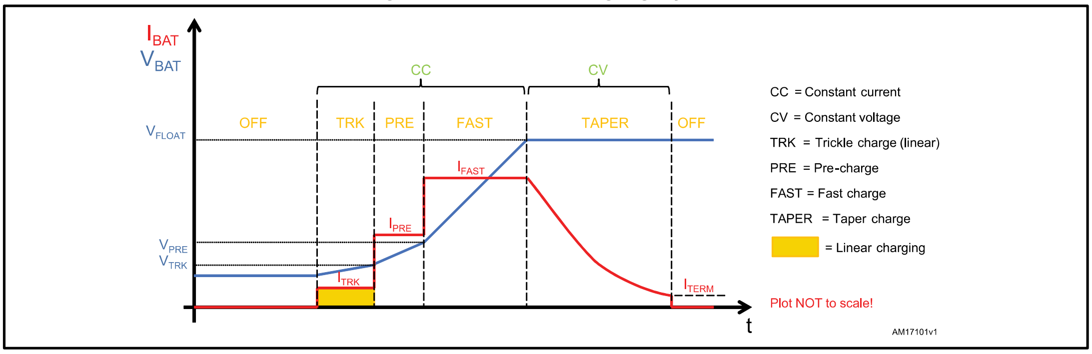
The constant voltage mode enters when the battery voltage reaches the programmable floating voltage threshold (V_{FLOAT}, 3.60 V to 4.70 V in 20 mV steps).

In constant voltage mode, the charging current tapers down the termination current threshold and then the charging process stops. The termination current is programmable from 50 mA to 300 mA in 25 mA steps.

A 360 minute (typ.) safety timer is active when the fast charge starts.

The charger can be disabled pulling high the charger enable input (CENn) and is automatically stopped in automatic shutdown conditions (ASD, V_{DCIN} - V_{BAT} < V_{ASD}).

Figure 4: CC/CV charging cycle



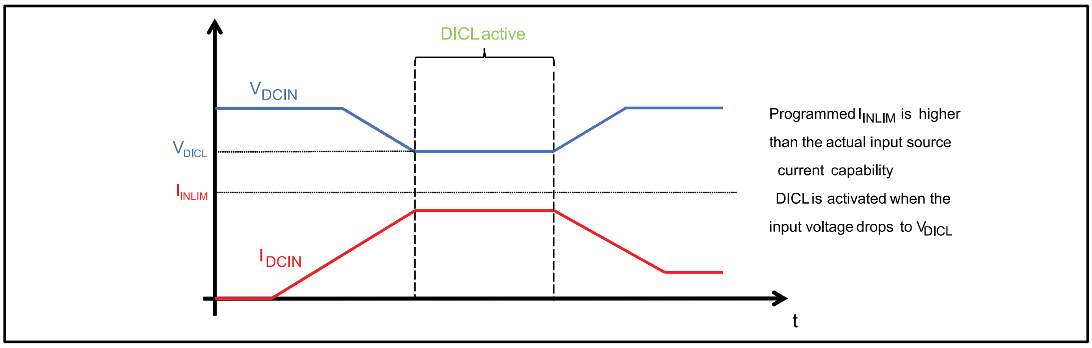
5.1.1 Input current limit

The STBCFG01 implements a programmable input current limitation to prevent the battery charger from exceeding DCIN voltage source current capability. The current limit can be programmed through I²C to the following maximum values: 100 mA, 500 mA, 800 mA, 1.2 A. A “no limit” option is also available.

5.1.2 Dynamic input current limit (DICL)

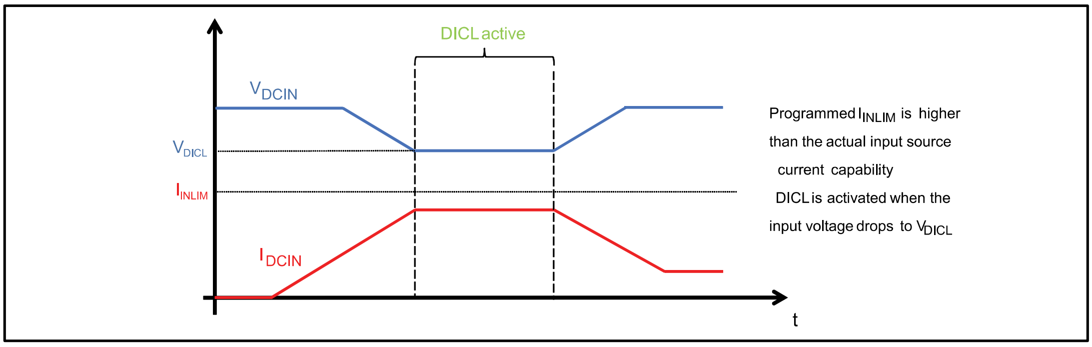
Independently from the chosen input current limit, a dynamic input current limit loop can also be enabled through the I²C compatible interface (DICL_en bit). When DICL is active, an analog loop limits the input current when the input voltage drops to a programmable threshold (V_{DICL} = 4.0 V to 4.75 V in 250 mV steps).

Figure 5: DICL activation



When a valid input source is connected to DCIN, DICL is enabled only if the input voltage is higher than V_{DICL} for a deglitch time (t_{DICL} = 100 ms). The user can check the enabling status of DICL function reading DICL status bit. Once DICL is enabled it can be disabled through DICL_en bit.

Figure 6: DICL enable strategy



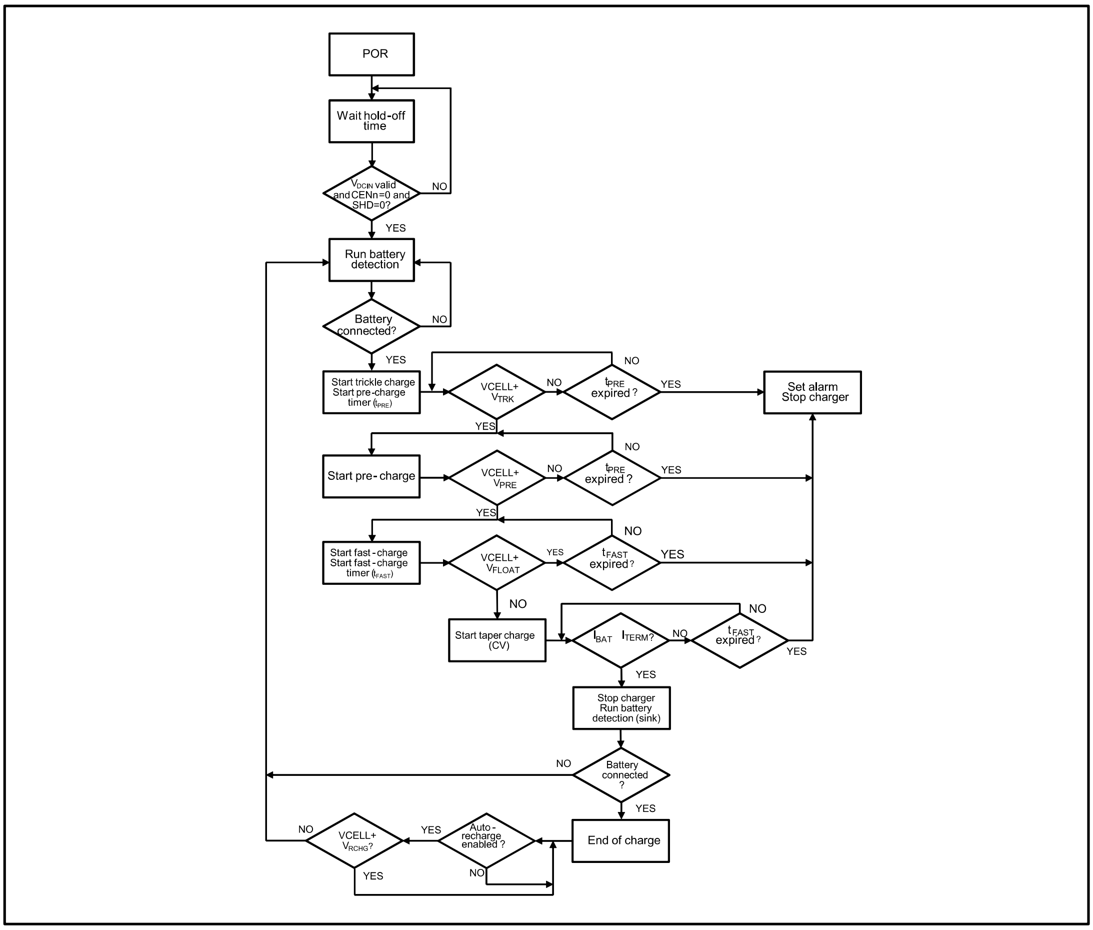
5.1.3 Automatic recharge

When the charging cycle is over, the device keeps monitoring the battery voltage: if the voltage drops below the auto-recharge threshold ($V_{RCHG} = V_{FLOAT}$ - 120 mV), a new charging cycle starts to keep the battery at maximum capacity. The automatic recharge function can be disabled through I²C.

5.1.4 Battery detection

The battery charger IC features a battery detection function to check if a battery is inserted before starting the charging cycle and to make sure that charging termination is not triggered because of a battery disconnection. If the battery is not detected when the input voltage is valid, the device keeps running the detection sequence until a battery is inserted. The battery detection result is reported by DET_ok bit. If the battery detection function or RID comparator detects a battery disconnection, BAT_Fail interrupt is generated. See the battery detection algorithm flowchart for more details.

Figure 7: Battery charger flowchart



5.1.5 Battery overvoltage protection

If the battery voltage exceeds the battery overvoltage protection threshold (V_{BATOVP} = V_{FLOAT} + 100 mV) for more than t_{BOVP}, the charging cycle stops and an alarm is generated. The battery overvoltage protection is active only when the charger is enabled. The charger automatically restarts when the battery voltage falls below the battery overvoltage protection threshold.

5.2 OTG boost

The STBCFG01's internal bridge can be used in boost configuration to generate USB OTG V_{BUS} voltage (5 V, 500 mA).

OTG boost generator can be enabled setting the dedicated I²C enable bit (OTG_en) according to the following conditions:

- $V_{DCIN} < V_{INUVLO}$
- CENn = high
- VCELL+ > $V_{BATUVLO}$

OTG boost operation is automatically stopped if the battery voltage falls below VBATUVLO or if CENn is pulled low during operation.

The device also features an output overvoltage protection which turns off OTG boost if the output voltage rises above V_{BUSOVP}. If the overvoltage lasts for more than $t_{VBUSOVP}$, OTG boost is disabled and an alarm is generated.

Together with the standard cycle-by-cycle current limit for the inductor peak current, the STBCFG01 also implements an average battery current limitation to avoid excessive battery voltage drop during peaks in system current consumption. When the average boost input current reaches the programmed limit (I_{BATLIM} = 350 mA, 450 mA, 550 mA, 950 mA), OTG boost is disabled and an alarm is generated.

5.3 LDO regulator

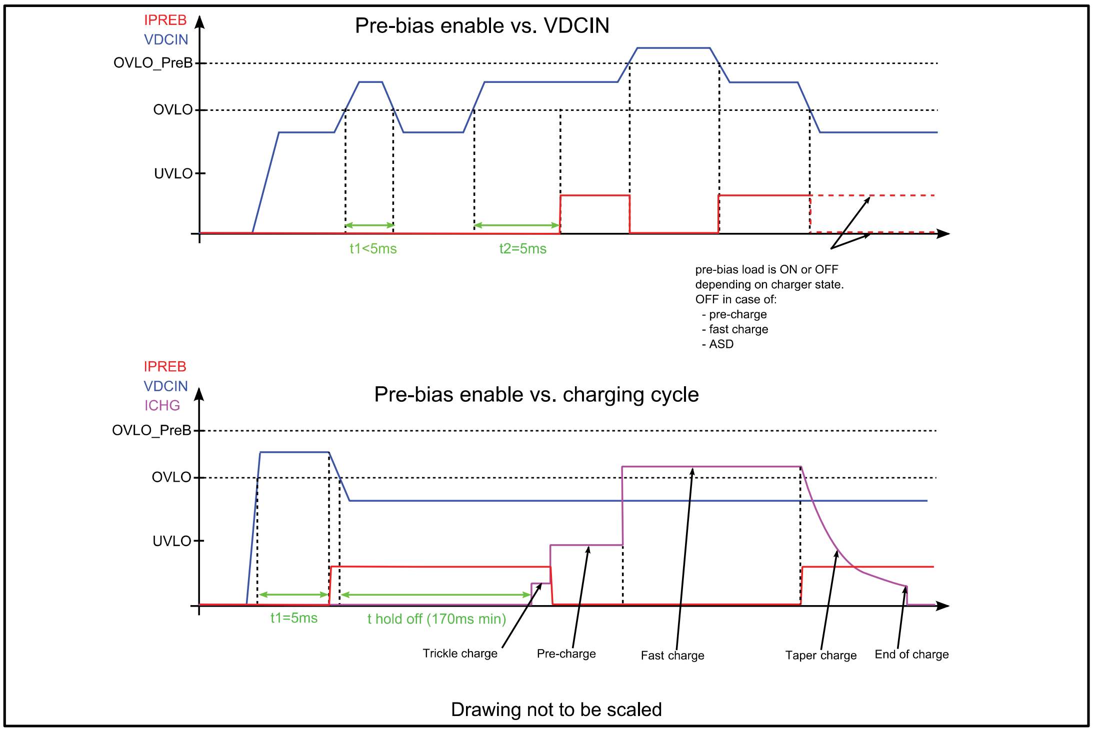
The STBCFG01 integrates a 4.85 V, 50 mA LDO regulator which is active when DCIN voltage is higher than V_{INMIN} and lower then V_{INMAX}. LDO is also active when the battery is not connected and in OTG mode, while it is turned off in automatic shutdown conditions (V_{DCIN} - V_{CELL+} < V_{ASD}). LDO function can be disabled through I²C and its output is protected against short-circuit.

5.4 Pre-bias

In order to allow proper functionality with input sources not integrating the necessary minimum load to provide a valid voltage, the STBCFG01 integrates an automatic pre-bias circuit: if the input voltage (V_{DCIN}) is above the input OVP threshold but lower than the pre-bias OVP threshold (V_{INOVP} < V_{DCIN} < V_{INOVP_PB}) a pre-bias current is applied to DCIN to attempt reducing the input voltage down to a valid level. During the charging cycle, if the pre-bias current has been activated, it is kept on only during trickle charge and taper charge. The pre-bias current is also turned off in automatic shutdown conditions (ASD).

The pre-bias current is active only if the input voltage is in the activation range for at least t_{PBD} (5 ms typ.). The pre-bias function can be disabled through I²C.

Figure 8: Pre-bias enable strategy



5.5 Fuel gauge

The voltage mode fuel gauge provides the accurate information about the state of the Lithium-Ion battery. Battery voltage is constantly monitored to evaluate the state of charge of battery and open circuit voltage.

At power-up, the fuel gauge algorithm uses the voltage reading to provide a first evaluation of SOC based on battery modeling data. The evolution of voltage is then used to track the changes of SOC of battery while cycling. The external software driver performs the temperature compensation.

Initial accuracy depends on the state of the battery. When the fuel gauge is active the battery is supposed to be in fully relaxed state. If the battery is not fully relaxed the initial error in the evaluation of the state of charge is high but converges to lower values while the battery is being used.

The fuel gauge block can be adapted to different batteries. Programmable parameters are used to tailor the algorithm to each battery model.

In order to keep the optimal performance and avoid losing information learned during battery cycling, the user is supposed to save data contained in the device's volatile memory when power is removed. The same data has to be restored at power-up.

The STBCFG01 also provides programmable alarms to notify low battery voltage and low SOC conditions.

5.5.1 Operating mode

At start-up and when the battery voltage is below UVLO threshold, the fuel gauge is in standby mode. This block is active when the battery voltage is above UVLO and GG_RUN bit has been set through I²C. When the fuel gauge is in standby mode, all register values are frozen and the algorithm does not run. In active mode, a voltage reading is acquired every 4 seconds (t_{STRB}).

5.5.2 Battery connection

When a battery is connected, the device wakes up and attempts reading the battery voltage before high current loads can change the open circuit voltage. The charging process is inhibited until the battery voltage reading is completed. If the battery voltage is too low, the charger is not inhibited to allow the battery to be charged up to a stable voltage and avoid oscillations.

5.5.3 Low battery alarm

The voltage mode fuel gauge provides low SOC and low battery voltage alarms, which are notified to the host through the active low open drain interrupt register (IRQn). Both of alarms can be disabled clearing ALRM_en bit in FG_Mode register.

Low battery voltage threshold and low SOC threshold can be changed writing ALARM_Voltage and ALARM_SOC registers. The default thresholds are 3.00 V battery voltage and 1% SOC.

When a low battery voltage condition or a low SOC condition is detected and alarms are enabled, the corresponding bit in FG_CTRL register is set (ALRM_VBAT or ALRM_SOC) and IRQn output is pulled low.

ALRM_VBAT and ALRM_SOC bits have to be cleared by the host to release the interrupt pin (if no other interrupt is active in the device).

If the alarm is cleared while the alarm condition is still true, the device does not generate another interrupt: the alarm condition has to disappear and be detected again in order to generate another interrupt.

At power-up or when the fuel gauge is reset, fuel gauge alarms are enabled and alarms are generated after the first OCV reading and SOC estimation (if the alarm condition is true).

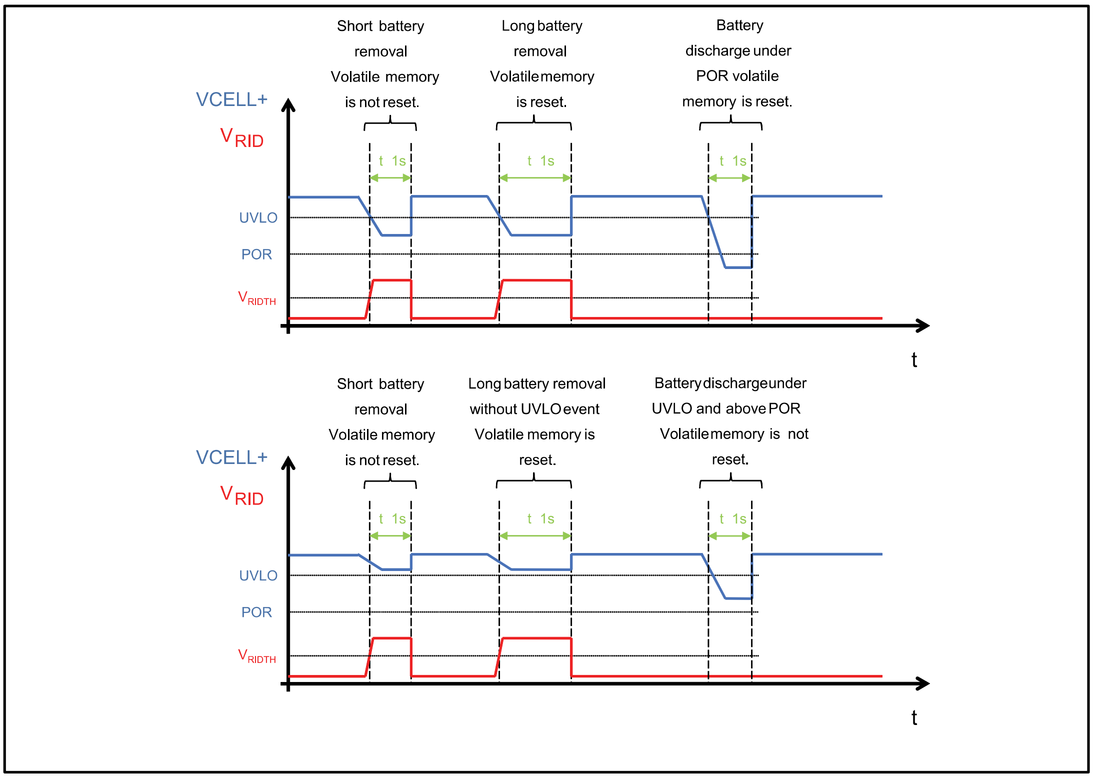
5.5.4 Battery swap

When the battery is removed from the system, the fuel gauge is reset to avoid providing wrong battery information if a different battery is inserted.

In order to detect battery disconnection, the STBCFG01 monitors both the battery voltage (VCELL+) and the voltage on RID pin connected to the battery identification resistor.

All volatile memory information is always lost when the battery voltage falls below POR threshold.

Figure 9: Battery swap detection



5.6 Thermal shutdown

In any working condition, if the die temperature reaches the thermal shutdown threshold (T_{SD} = 165 °C typ.) the device enters shutdown mode: the bridge and LDO output turn off. The fuel gauge keeps working normally. The operation is automatically restored when the temperature falls back into the valid range. Safety timers are reset when a thermal shutdown is triggered.

5.7 Shutdown mode

When SHDN pin is tied high the device enters shutdown mode. In this mode, the switching converter turns off and it cannot be used neither in charging mode nor OTG boost mode. LDO and fuel gauge functionality are not affected by SHDN pin.

5.8 Watchdog

A watchdog timer function can be enabled to reset the programmable register values to power-on reset values if no I²C acknowledgments are generated for more than 45 seconds. This function is normally disabled.

5.9 Alarms

The STBCFG01 provides an open drain active low interrupt output (IRQn) to notify the application processor about abnormal operating conditions or generic events. The following register types check the status of alarms and control the device:

- Interrupt enable
- Interrupt latch

The interrupt enable registers enable the propagation of alarms to the interrupt pin (IRQn). The interrupt is generated (IRQn pulled low) on a rising edge of the interrupt latch bits (assuming that the corresponding enable bit has been set).

The interrupt latch registers show the alarm conditions, which generate the interrupt. Although the alarm condition is no longer active, once each latch register bit is set, it stays high until the register is updated. Interrupt latch registers are updated by writing 0 to their bits: if the alarm condition is still active the bit is kept to 1 (new interrupt is not generated); if the alarm condition is no more active the bit is cleared. This update method assures that no further rising edge on the latch bit is generated for alarms which have already been signaled before the update operation. In order to release IRQn line after an interrupt generated by the charger/OTG, the host processor has to write 0 to IRQ_CLR bit in CHG_Cfg2 register and then back 1. The fuel gauge generated alarms share the same enable bit (ALRM_en).

The following conditions generate an interrupt signal:

- DCIN UVLO
- DCIN OVP
- ASD condition
- Pre-charge timer expiration
- Fast charge timer expiration
- Watchdog timer expiration
- Battery overvoltage protection (charger)
- End of charge
- Battery undervoltage lockout (OTG boost)
- V_{BUS} overvoltage protection (OTG boost)
- Average current limit reached (OTG boost, I_{BATLIM})
- OTG output short-circuit; thermal shutdown
- Low battery voltage (fuel gauge)
- Low SOC (fuel gauge)

6 I²C compatible interface registers

The STBCFG01 can be monitored and controlled using the I²C compatible communication interface. The 7-bit device slave address is 1110001_{BIN}. The table below shows the register map.

Table 6: Register map

Name	Address	POR value	R/W
Fuel gauge			
FG_Mode	00h	19h	R/W
FG_CTRL	01h	15h	R/W
SOC	02h-03h	0000h	R/W
VBAT	08h-09h	0000h	R
OCV	0Dh-0Eh	0000h	R
VM_CNF	11h-12h	0141h	R/W
ALARM_SOC	13h	02h	R/W
ALARM_Voltage	14h	AAh	R/W
REG_ID	18h	14h	R
RAM0…RAM15	20h…2Fh	-	R/W
OCV_ADJ	30h…3Fh	-	R/W
LUT	5Dh…8Ch	-	R/W
Charger/OTG			
CHG_Cfg1	90h	00h	R/W
CHG_Cfg2	91h	62h	R/W
CHG_Cfg3	92h	61h	R/W
CHG_Cfg4	93h	4Fh	R/W
CHG_Cfg5_OTG_Status	94h	06h	R/W
CHG_Status1	95h	00h	R
CHG_Status2	96h	C0h	R
Int_Enable_1	97h	00h	R/W
Int_Enable_2	98h	00h	R/W
Int_Latch_1	99h	00h	R/W
Int_Latch_2	9Ah	00h	R/W

6.1 Fuel gauge registers

Table 7: Fuel gauge mode register (address: 00h)

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
-	OTG_en	LPM_dis	GG_RUN	ALRM_en	-	-	-	19h	R/W

ALRM_en: fuel gauge alarm enable

- 0: disabled
- 1: enabled (default)

GG_RUN: fuel gauge operative mode

- 0: standby (default). Registers are frozen, fuel gauge in standby
- 1: running

LPM_dis: low power mode disable (set this bit to program battery charger/OTG configuration registers and enable OTG function when USB input is not plugged and GG_RUN = 0)

- 0: low power mode enabled (default)
- 1: low power mode disabled

OTG_en: OTG boost enable bit

- 0: disabled (default)
- 1: enabled

Table 8: FG_CTRL register (address: 01h)

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
-	ALRM_VBAT	ALRM_SOC	POR_Det	BAT_Fail	-		IODATA	15h	R/W

IODATA: IRQn pin status

Read:

- 0: IRQn pin is low
- 1: IRQn pin is high
  Write:
- 0: forces IRQn pin low
- 1: IRQn pin is driven by interrupt logic
  BAT_Fail: battery removal or battery UVLO detection bit. Write 0 to clear
- 0: battery connected
- 1: battery removed or UVLO

POR_Det: power-on reset detection bit. Write 1 to force a soft reset (self-clearing)

- 0: no POR event occurred
- 1: POR event occurred

ALRM_SOC: low SOC alarm

- 0: SOC OK
- 1: low SOC

Write this bit to 0 to clear the alarm. If the alarm condition is still active a new alarm is triggered only on the following rising edge of the alarm condition (the alarm condition has to disappear and then appear again).

ALRM_VBAT: low battery voltage alarm

- 0: battery voltage above threshold
- 1: low battery voltage

Write this bit to 0 to clear the alarm. If the alarm condition is still active a new alarm is triggered only on the following rising edge of the alarm condition (the alarm condition has to disappear and then appear again).

Table 9: SOC register LSB (register address: 02h)

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
SOC[7:0]								00h	R/W

Table 10: SOC register MSB (register address: 03h)

b15	B14	b13	b12	b11	b10	b9	b8	POR	R/W
SOC[15:8]								00h	R/W

SOC register LSb: 1/512% SOC

Table 11: VBAT register LSB (register address: 08h)

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
VBAT[7:0]								00h	R

Table 12: VBAT register MSB (register address: 09h)

b15	B14	b13	b12	b11	b10	b9	b8	POR	R/W
Reserved					VBAT[10:8]			00h	R

VBAT register LSb: 2.69 mV

Table 13: OCV register LSB (register address: 0Dh)

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
OCV[7:0]								00h	R

Table 14: OCV register MSB (register address: 0Eh)

b15	B14	b13	b12	b11	b10	b9	b8	POR	R/W
Reserved			OCV[12:8]					00h	R

OCV register LSb: 0.67 mV

Table 15: VM_CNF register LSB (register address: 11h)

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
VM_CNF[7:0]								41h	R/W