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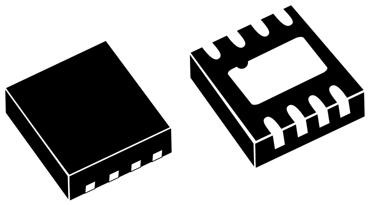
STBP112

Overvoltage protection device

Datasheet - production data

Features

- Input overvoltage protection up to 28 V
- Integrated high voltage N-channel MOSFET switch - low $R_{DS(on)}$ of 165 mΩ
- Integrated charge pump
- Maximum continuous current of 2 A
- Thermal shutdown
- Soft-start feature to control the inrush current
- Enable input ($\overline{EN}$)
- Fault indication output ($\overline{FLT}$)
- IN input ESD protection: ±15 kV air discharge, ±8 kV contact discharge (with 1 µF input capacitor), ±2 kV HBM (standalone device)
- Certain overvoltage options compliant with the China Communications Standard YD/T 1591-2006 (overvoltage protection only)
- Small, RoHS compliant 2 x 2 x 0.75 mm TDFN 8-lead package with thermal pad.



TDFN 8-lead (2 x 2 x 0.75 mm)

Applications

- Smart phones
- Digital cameras
- PDA and palmtop devices
- MP3 players
- Low power handheld devices.

Contents

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1 Description

The STBP112 device provides overvoltage protection for input voltage up to +28 V. Its low $R_{DS(on)}$ N-channel MOSFET switch protects the systems connected to the OUT pin against failures of the DC power supplies in accordance with the China MII Communications Standard YD/T 1591-2006.

In the event of an input overvoltage condition, the device immediately disconnects the DC power supply by turning off an internal low $R_{DS(on)}$ N-channel MOSFET to prevent damage to protected components.

In addition, the device also monitors its own junction temperature and switches off the internal MOSFET if the junction temperature exceeds the specified limit.

The device can be controlled by the microcontroller and can also provide status information about fault conditions.

The STBP112 is offered in a small, RoHS-compliant 8-lead TDFN (2 mm x 2 mm) package.

Figure 1. Logic diagram

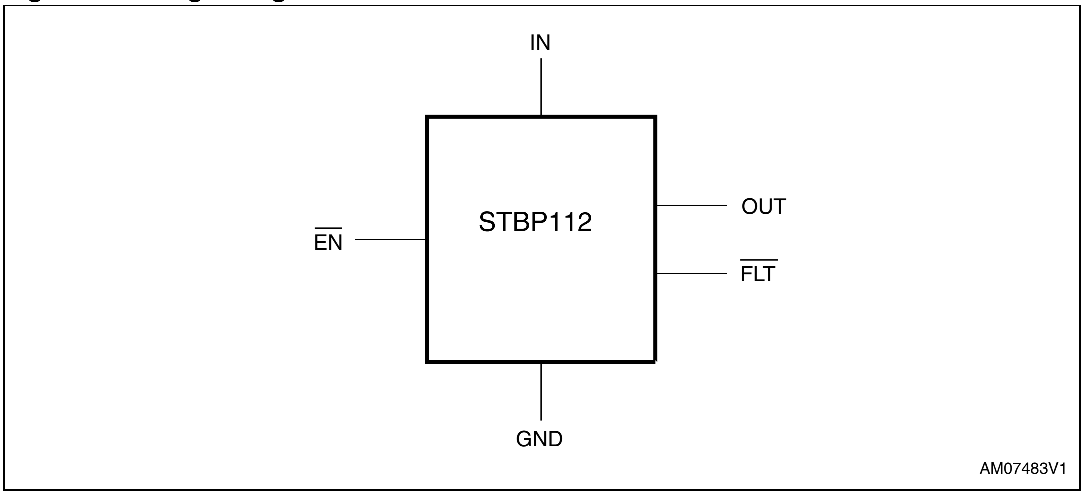
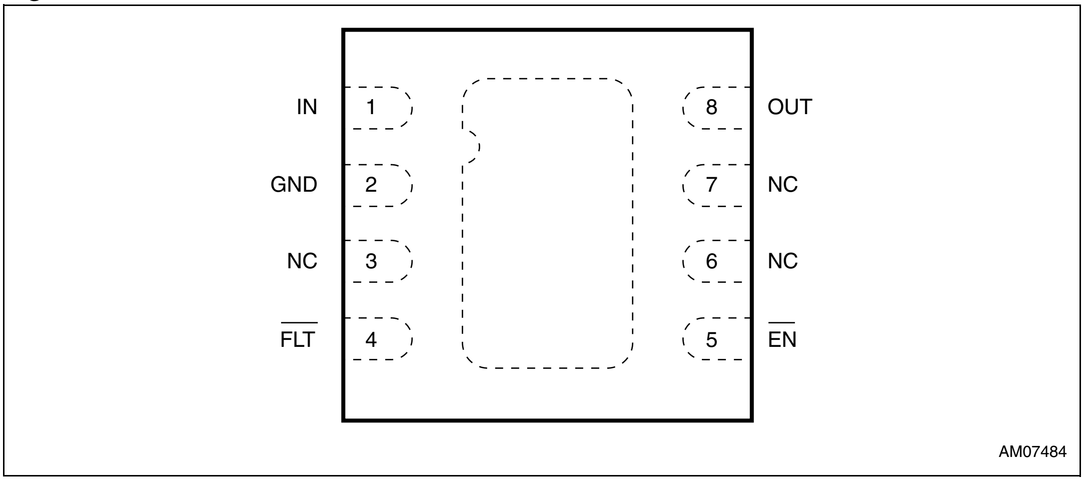


Figure 2. Pinout



1. Exposed thermal pad may be tied to GND.

2 Pin description

2.1 Input (IN)

Input voltage (IN) pin. The IN pin is connected to the DC power supply. An external low ESR ceramic capacitor of minimum value 1 µF must be connected between IN and GND. This capacitor is needed for decoupling and also protects the IC against fast voltage spikes and ESD events. This capacitor should be located as close to the IN pin as possible.

2.2 Output (OUT)

Output voltage (OUT) pin. The OUT pin is connected to the input through a low $R_{DS(on)}$ N-channel MOSFET switch.

If no fault is detected and the STBP112 is enabled by the $\overline{EN}$ input, this switch is turned on and the output voltage follows the input voltage.

The output is disconnected from the input when the input voltage is under the UVLO threshold or above the OVLO threshold, when the junction temperature is above the thermal shutdown threshold or when the device is disabled by the $\overline{EN}$ input.

After the input voltage or junction temperature returns to the specified range, there is a recovery delay, t_{rec}, and the power output is then connected to the input (see *Figure 8 on page 13*).

The switch turn-on time is intentionally prolonged to limit the inrush current and voltage drop caused, for example, by charging output capacitors (soft-start feature).

2.3 Fault indication output ($\overline{FLT}$)

The active low, open-drain fault indication output provides information on the STBP112 state to the application controller. The $\overline{FLT}$ is asserted (i.e. driven low), if the STBP112 is in the overvoltage condition or thermal shutdown mode is active.

As the $\overline{FLT}$ output is of the open-drain type, it may be pulled up by an external resistor R_{PU} to the controller supply voltage (see *Figure 4*). If there is no need to use this output, it may be left disconnected. The suitable R_{PU} resistor value is in the range of 10 kΩ to 1 MΩ.

To improve safety and to prevent damage to application circuits in the event of extreme voltage or current conditions, an optional protective resistor R_{FLT} can be connected between the $\overline{FLT}$ output and the controller input (see *Figure 4*). The suitable R_{FLT} resistor value is in the range of 10 kΩ to 100 kΩ.

The $\overline{FLT}$ output is in Hi-Z (high impedance) state when the device is disabled by $\overline{EN}$ input or when the input voltage is lower than the UVLO threshold.

2.4 Enable input ($\overline{EN}$)

This active low logical input can be used to enable or disable the device. When the $\overline{EN}$ input is driven high, the STBP112 is in shutdown mode and the power output is disconnected from the input (see *Figure 8 on page 13*). When the $\overline{EN}$ input is driven low and all operating conditions are within specified limits, the power output is connected to the input.

The $\overline{EN}$ input is equipped with an internal pull-down resistor of 250 kΩ (typical value). If there is no need to use this input, it may be left floating or, preferably, connected to GND.

For V_{IN} lower than 2.5 V (max.), the pull-down resistor is internally disconnected to lower the $\overline{EN}$ pin input current in case the external AC adapter is not connected, the application is running from an internal battery and the STBP112 device is disabled.

To improve safety and to prevent damage to application circuits in the event of extreme voltage or current conditions, an optional protective resistor R_{EN} can be connected between the $\overline{EN}$ input and the controller output (see *Figure 4*). The protective resistor forms a voltage divider with the internal pull-down resistor, which limits the maximum possible R_{EN} value with respect to the $V_{IH(\overline{EN})}$ threshold of $\overline{EN}$ input and the controller's output voltage for logic high, V_{OH}. For the worst case, the highest protective resistor value is

$$R_{ENmax} = R_{PD(\overline{EN})min} \times (V_{OH} / V_{IH(\overline{EN})} - 1),$$

where $R_{PD(\overline{EN})min}$ is 100 kΩ and $V_{IH(\overline{EN})}$ is 1.2 V.

For most cases, an R_{EN} value of 10 kΩ to 100 kΩ is adequate.

The $\overline{FLT}$ output is in Hi-Z state when the device is disabled by $\overline{EN}$ input.

2.5 No connect (NC)

Pin 3, 6, and 7 are no connect (NC). They may be left floating or connected to GND.

2.6 Ground (GND)

Ground terminal. All voltages are referenced to GND. The exposed thermal pad is internally connected to GND.

Table 1. Pin description and signal names

Pin	Name	Type	Function
1	IN	Input/supply	Input voltage
2	GND	Supply	Ground
3, 6, 7	NC	-	Not connected
4	$\overline{FLT}$	Output	Fault indication output (open-drain)
5	$\overline{EN}$	Input	Enable input (pull-down resistor to GND)
8	OUT	Output	Output voltage

Figure 3. Block diagram

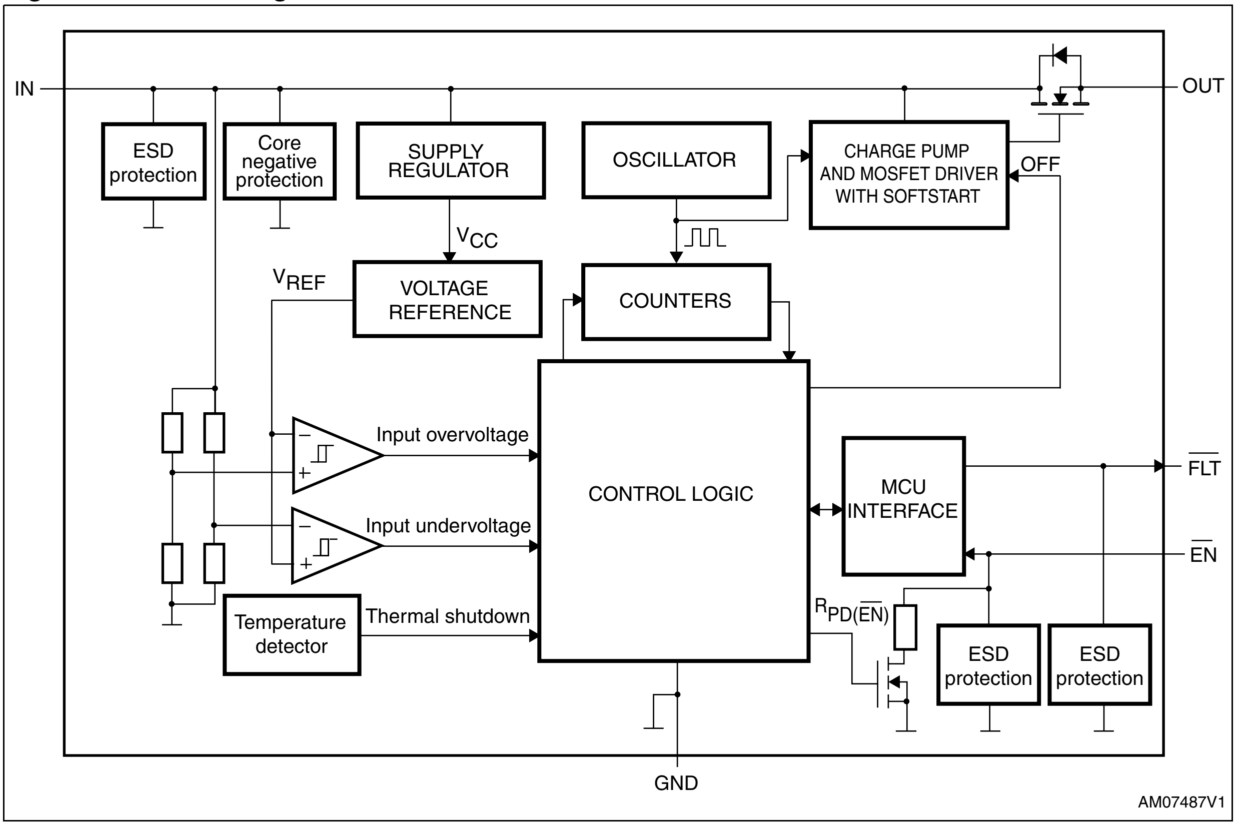
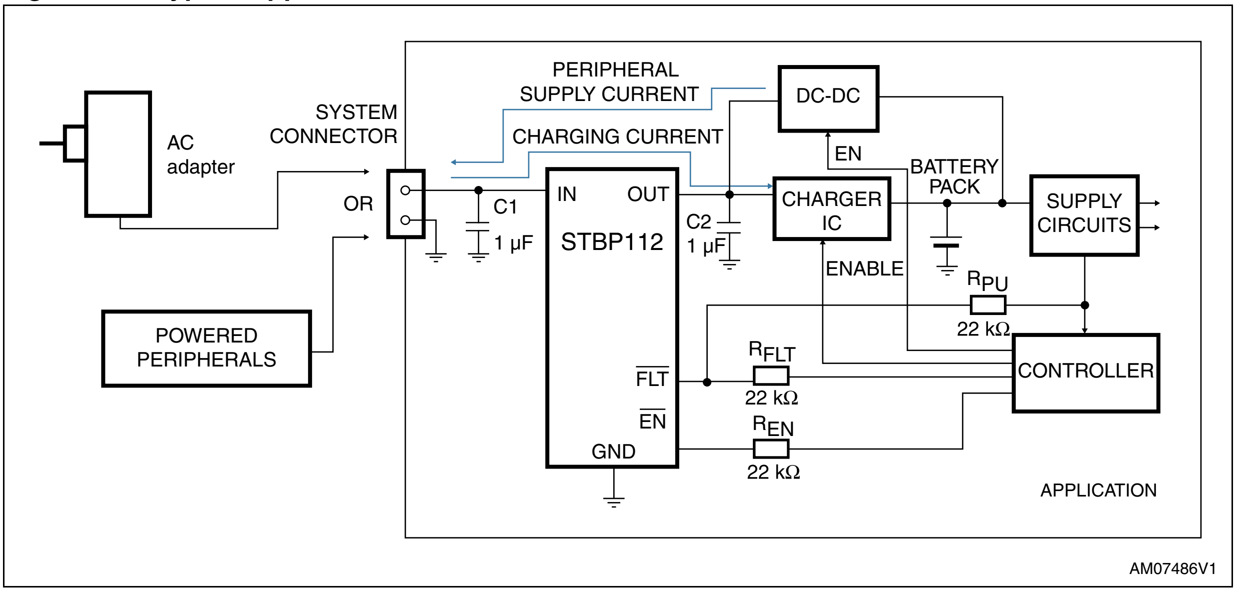


Figure 4. Typical application circuit



1. Optional resistors R_{EN} and R_{FLT} prevent damage to the controller under extreme voltage or current conditions and are not required. Low ESR ceramic capacitor C1 is necessary to ensure proper function of the STBP112. Capacitor C2 is not necessary for STBP112 but may be required by the charger IC.
2. The STBP112 MOSFET switch topology allows the current to flow also in a reverse direction, i.e. from OUT to IN, which can be useful for powering external peripherals from the system connector. If the reverse current (supply current) is undesirable, it may be prevented by connecting an external Schottky diode in series with the OUT pin. The voltage drop between IN and the charger is then increased by the voltage drop across the diode.

3 Operation

The STBP112 provides overvoltage protection for positive input voltage up to 28 V using a built-in low $R_{DS(on)}$ N-channel MOSFET switch.

3.1 Power-up

At power-up, with $\overline{EN}$ = low, the MOSFET switch is turned on after the startup delay, t_{on}, after the input voltage exceeds the UVLO threshold to ensure the input voltage is stabilized (see *Figure 5*).

3.2 Normal operation

The device continuously monitors the input voltage and its own internal temperature so the output voltage is kept within the specified range. The internal MOSFET switch is turned on and the $\overline{FLT}$ output is deasserted.

The STBP112 enters normal operation state if the input voltage returns to the interval between V_{UVLO} and V_{OVLO} - $V_{HYS(OVLO)}$ and the junction temperature falls below T_{off} - $T_{HYS(off)}$. The internal MOSFET is turned on after the t_{rec} delay to ensure that the conditions have stabilized and the $\overline{FLT}$ output is deasserted.

Note: *The STBP112 MOSFET switch topology allows the current to flow also in a reverse direction, i.e. from OUT to IN, which can be useful for powering external peripherals from the system connector (see the supply current in Figure 4). At first, the current flows through the MOSFET body diode. If the voltage that appears on the IN terminal is above the UVLO threshold, the MOSFET is (after the startup delay) turned on so the voltage drop across STBP112 is significantly reduced.*
If the reverse current is undesirable, it may be prevented by connecting an external, properly rated low drop Schottky diode in series with the OUT pin. The voltage drop between IN and charger is increased by the voltage drop across the diode.

3.3 Undervoltage lockout (UVLO)

To ensure proper operation under any condition, the STBP112 has an undervoltage lockout (UVLO) threshold. When the input voltage is rising, the output remains disconnected from input until the V_{IN} voltage exceeds the V_{UVLO} threshold. This circuit is equipped with hysteresis, $V_{HYS(UVLO)}$, to improve noise immunity under transient conditions.

3.4 Overvoltage lockout (OVLO)

If the input voltage V_{IN} rises above the threshold level V_{OVLO}, the MOSFET switch is immediately turned off. At the same time, the fault indication output $\overline{FLT}$ is activated (i.e. driven low), see *Figure 6*. This device is equipped with hysteresis, $V_{HYS(OVLO)}$, to improve noise immunity under transient conditions.

3.5 Thermal shutdown

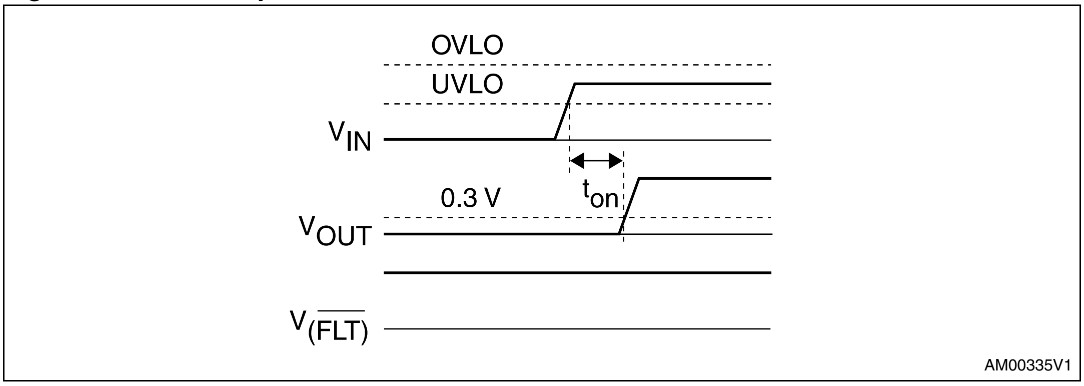
If the STBP112 internal junction temperature exceeds the T_{off} threshold, the internal MOSFET switch is turned off and the fault indication output $\overline{FLT}$ is driven low.

To improve thermal robustness, this circuit has a 20 °C hysteresis, $T_{HYS(off)}$.

Due to the internal reverse diode, the thermal shutdown is not functional for the reverse current.

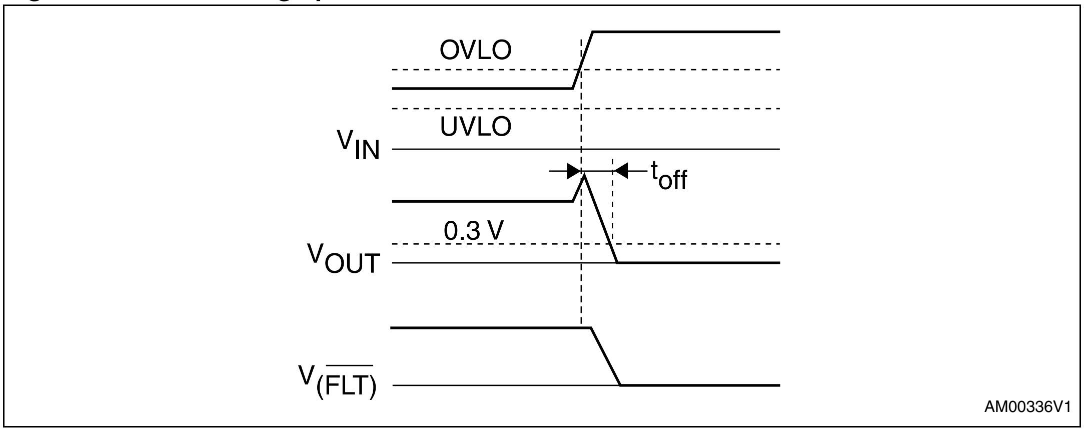
4 Timing diagrams

Figure 5. Power-up



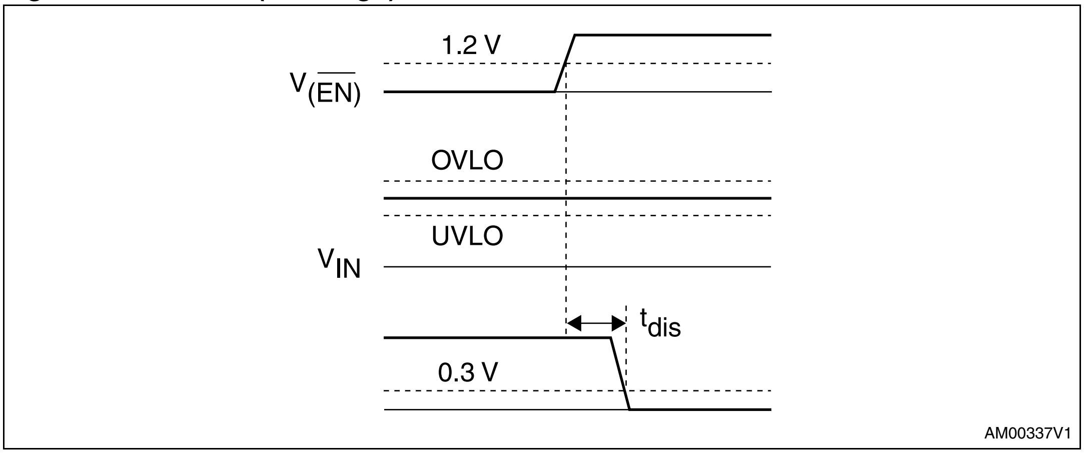
1. EN input is low.

Figure 6. Overvoltage protection



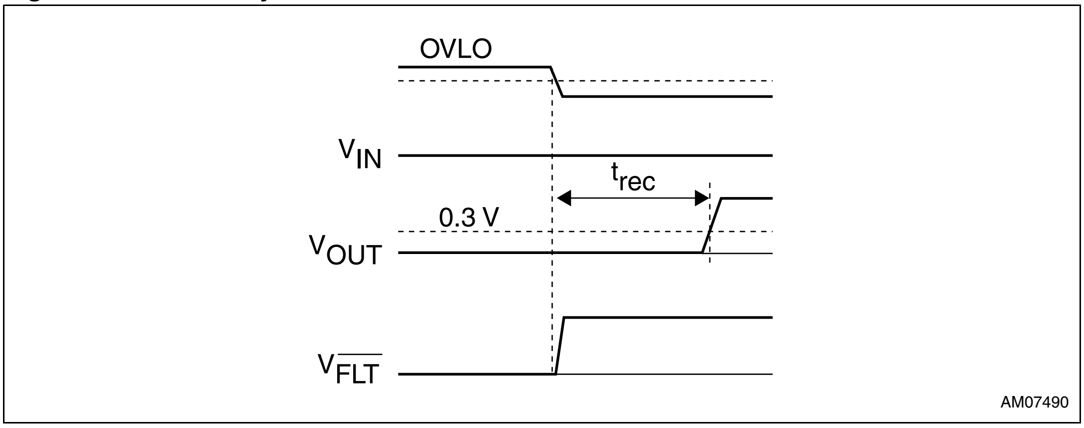
1. EN input is low.

Figure 7. Disable (EN = high)



1. FLT output is in Hi-Z state when EN driven high.

Figure 8. Recovery from OVP



1. $\overline{EN}$ input is low.

5 Typical operating characteristics

Figure 9. Maximum load current at T_A = 50 °C and 85 °C for various PCB thermal performance and $T_J \leq 125$ °C

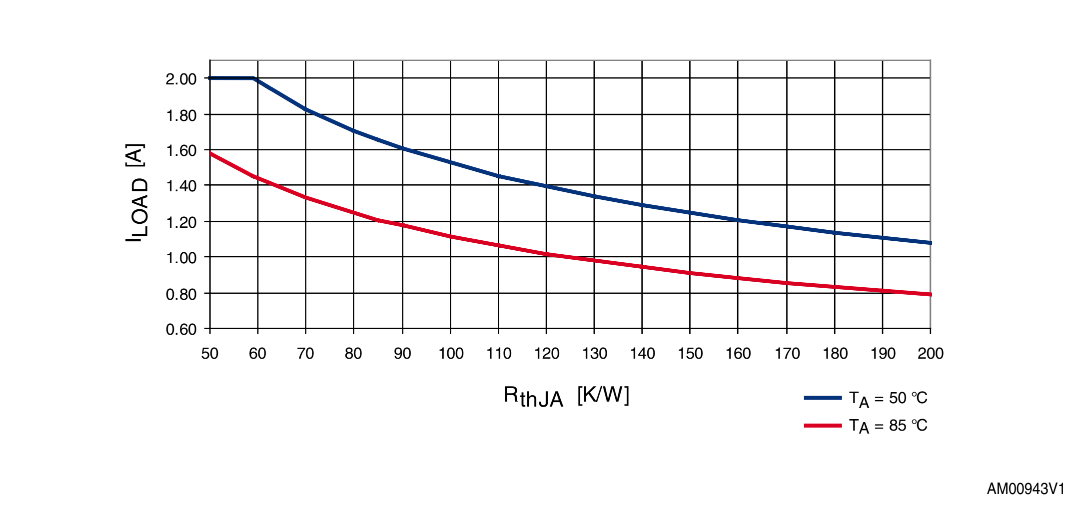
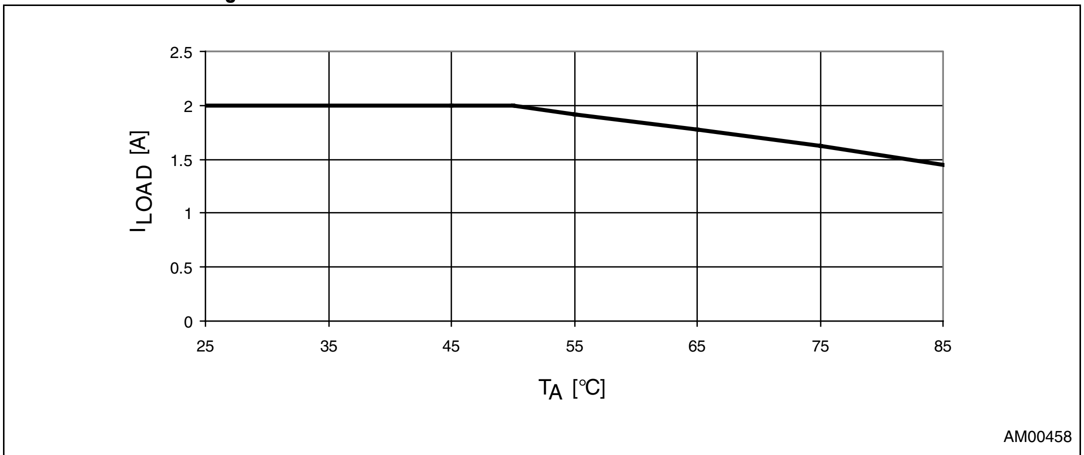
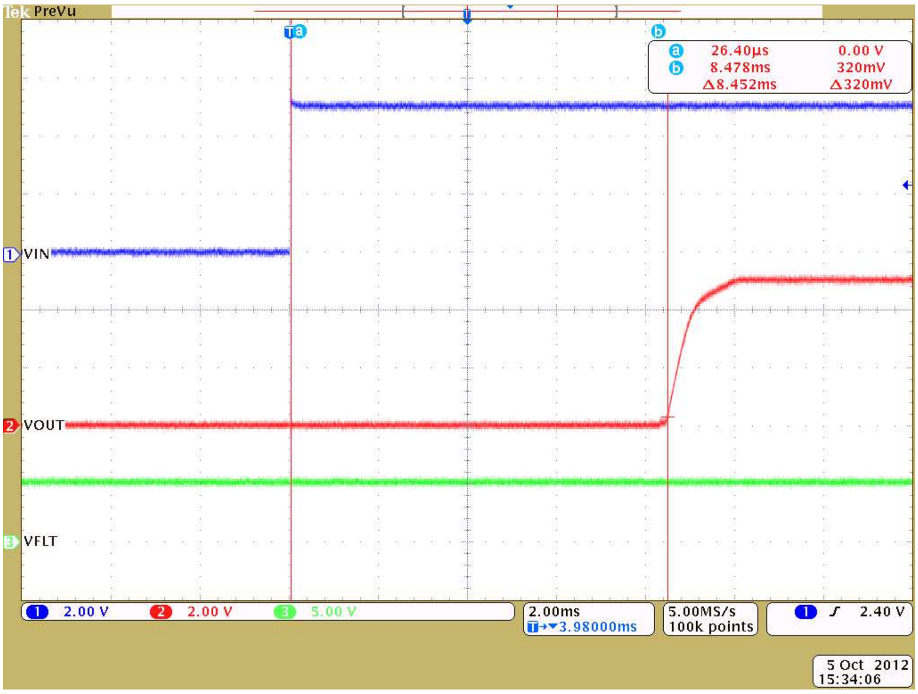


Figure 10. Maximum load current vs. ambient temperature for R_{thJA} = 59 K/W and $T_J \leq 125$ °C



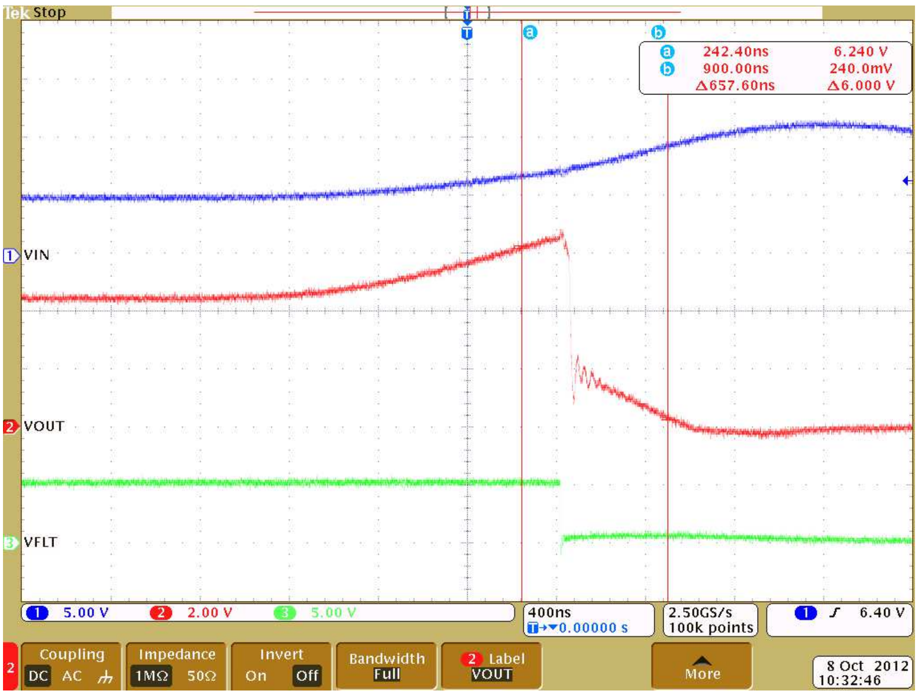
Typical operating characteristics (STBP112CV)

Figure 11. Startup, t_{on}



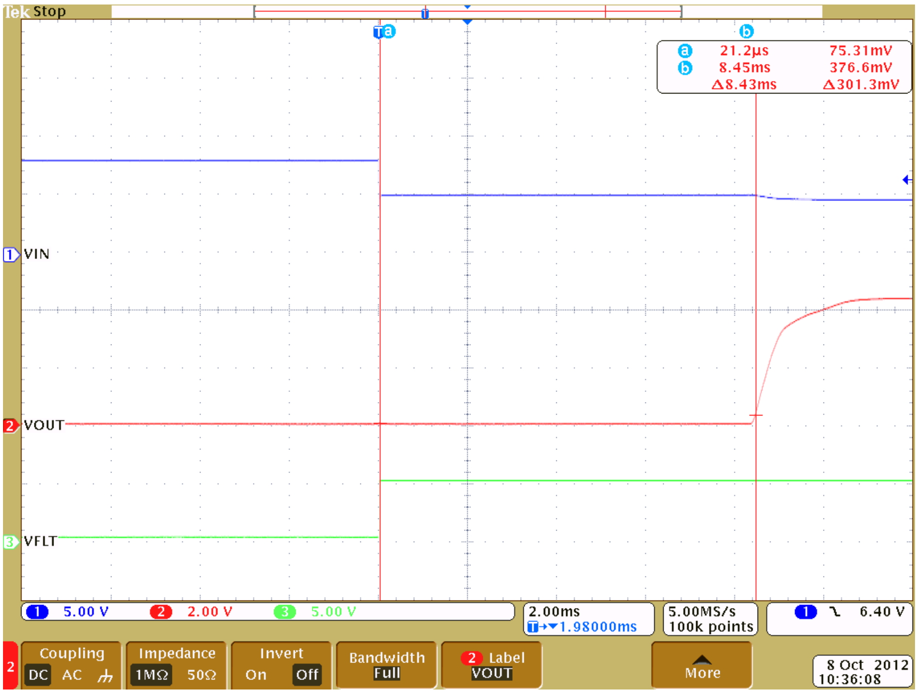
1. Output load is 100 kΩ.

Figure 12. Overvoltage, t_{off}



1. Output load is 5 Ω.

Figure 13. Recovery from overvoltage, t_{rec}

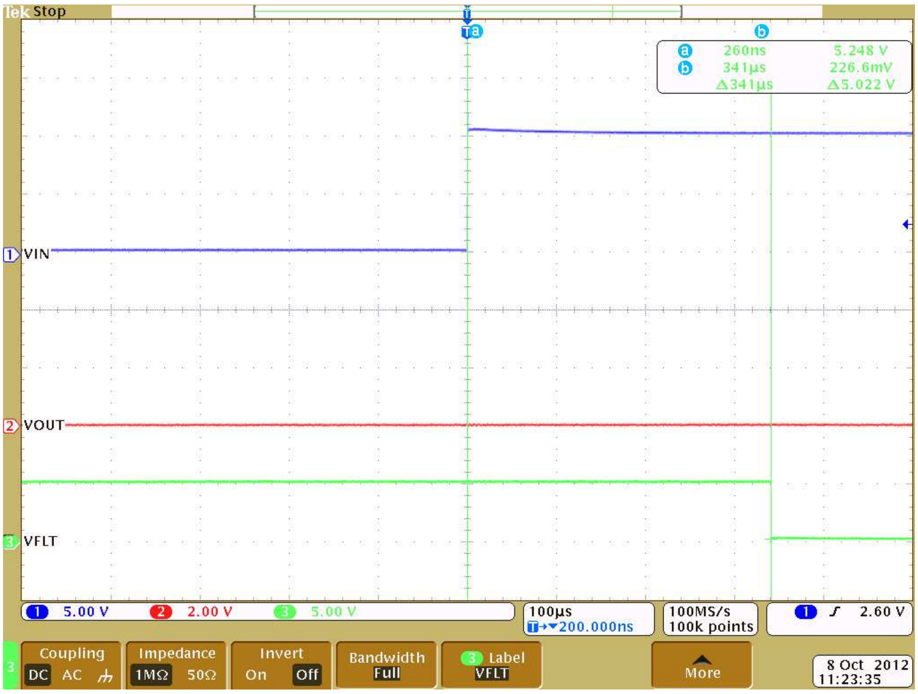


1. Output load is 5 Ω.

Figure 14. Disable, t_{dis}

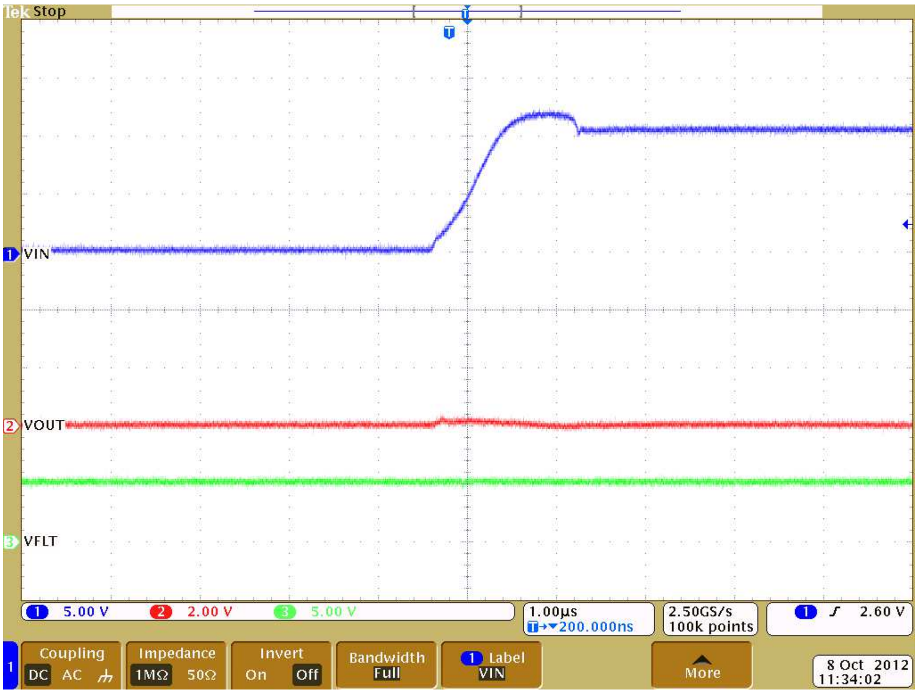
1. Output load is 5 Ω.

Figure 15. Startup to overvoltage



1. Output load is 5 Ω.

Figure 16. Startup to overvoltage (detail)



1. Output load is 5 Ω. Almost no glitch on the output.

Figure 17. Soft-start performance for 10 µF capacitive load

1. Output load is 10 µF in parallel with 5 Ω.

Figure 18. Soft-start performance for 100 µF capacitive load

1. Output load is 100 µF in parallel with 5 Ω.

Figure 19. I_{CC} vs. temperature at V_{IN} = 5 V

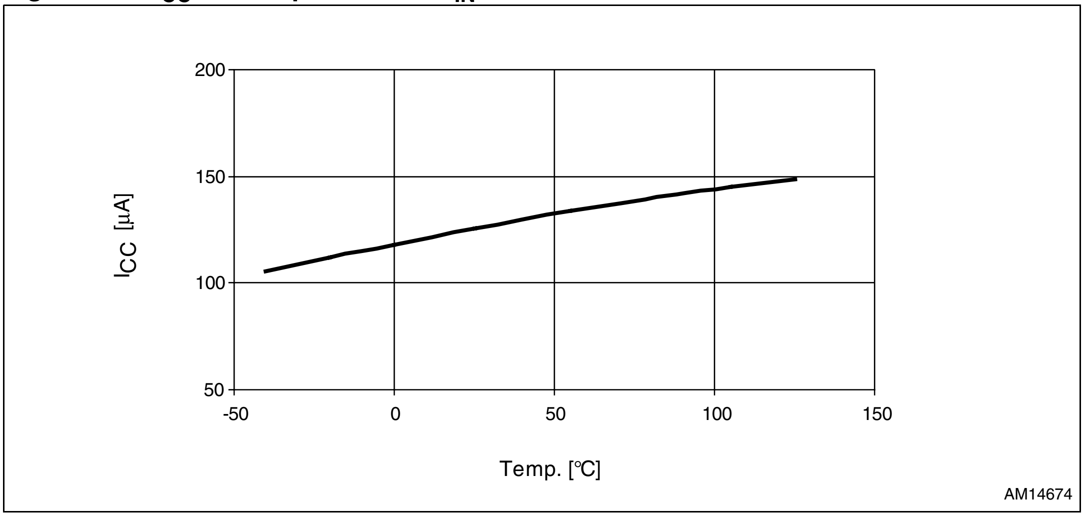


Figure 20. I_{CC} vs. V_{IN}

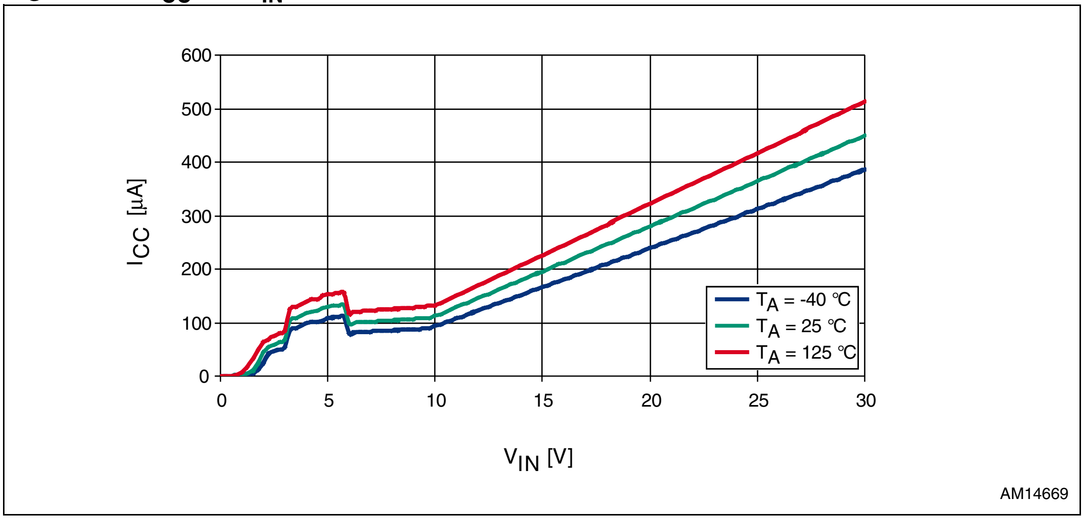


Figure 21. I_{CC} vs. V_{IN} (detail)

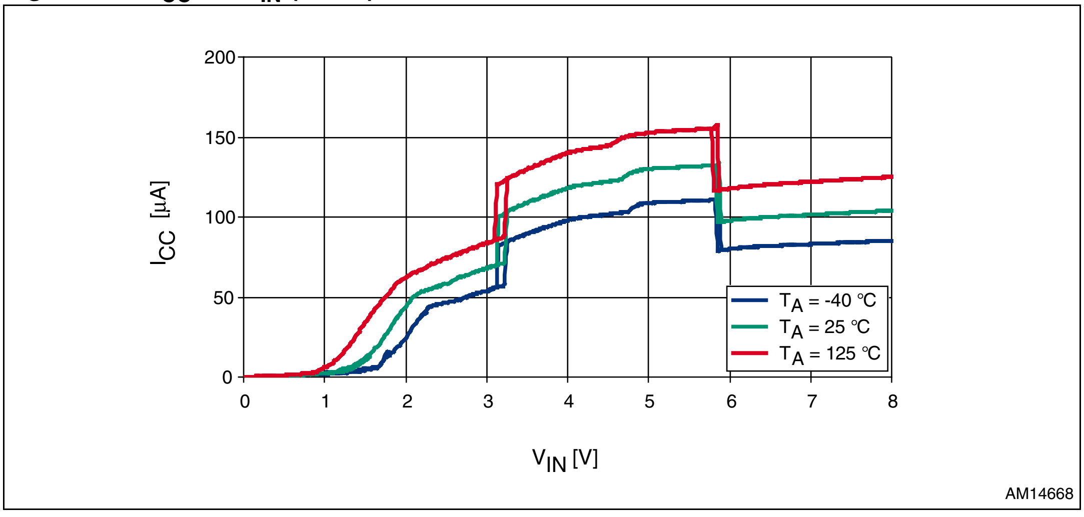


Figure 22. $I_{CC(STDBY)}$ vs. temperature at V_{IN} = 5 V

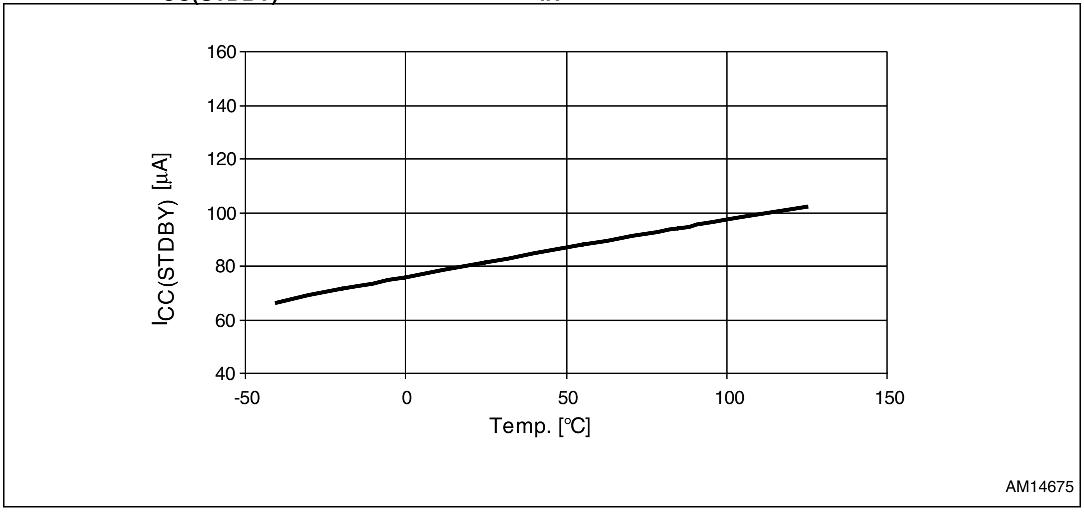


Figure 23. $I_{CC(STDBY)}$ vs. V_{IN}

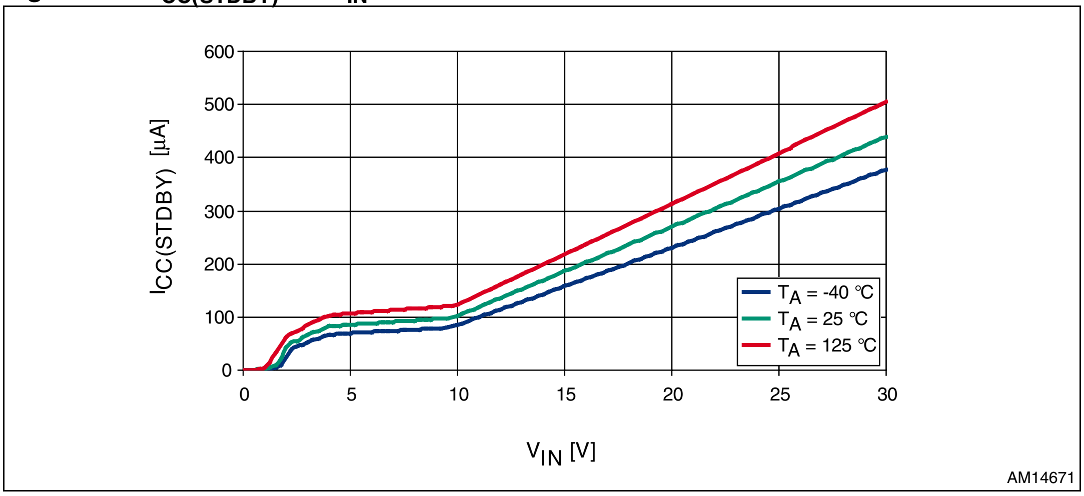


Figure 24. $I_{CC(STDBY)}$ vs. V_{IN} (detail)

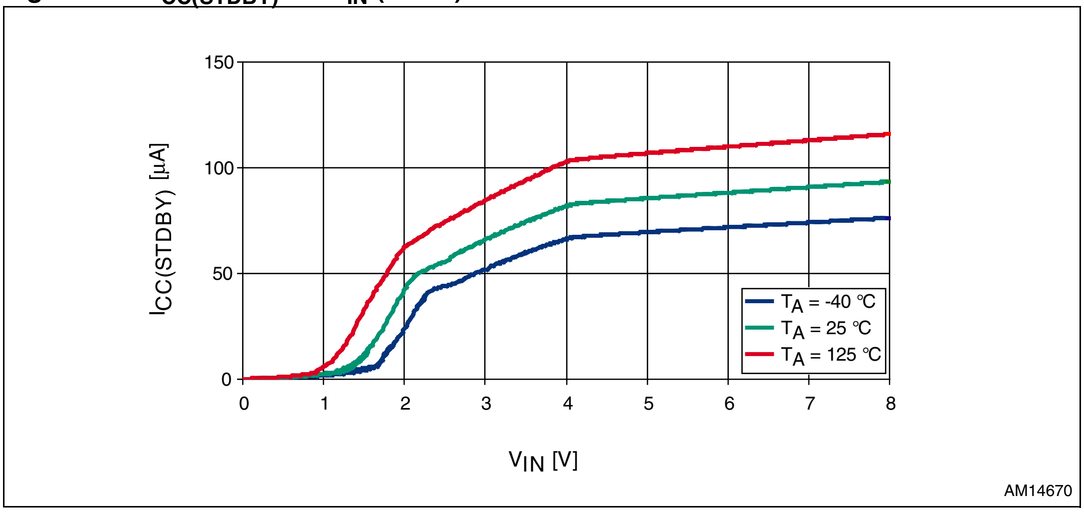


Figure 25. V_{OVLO} vs. temperature

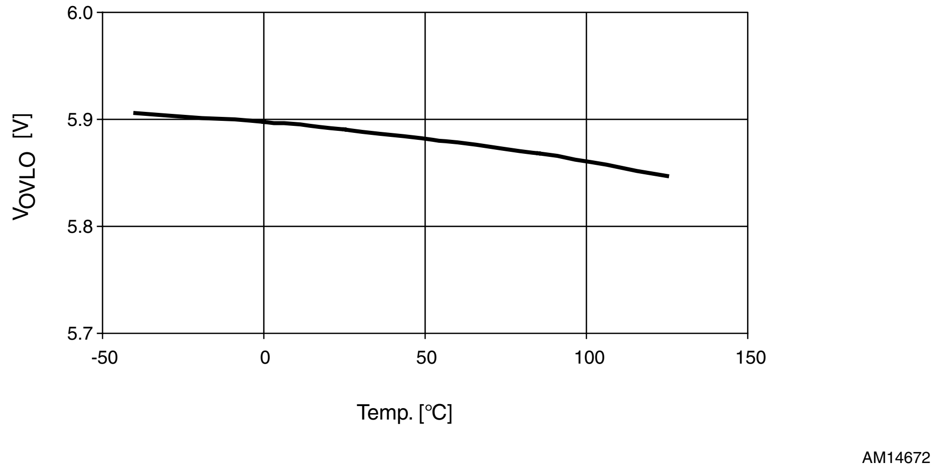


Figure 26. V_{UVLO} vs. temperature

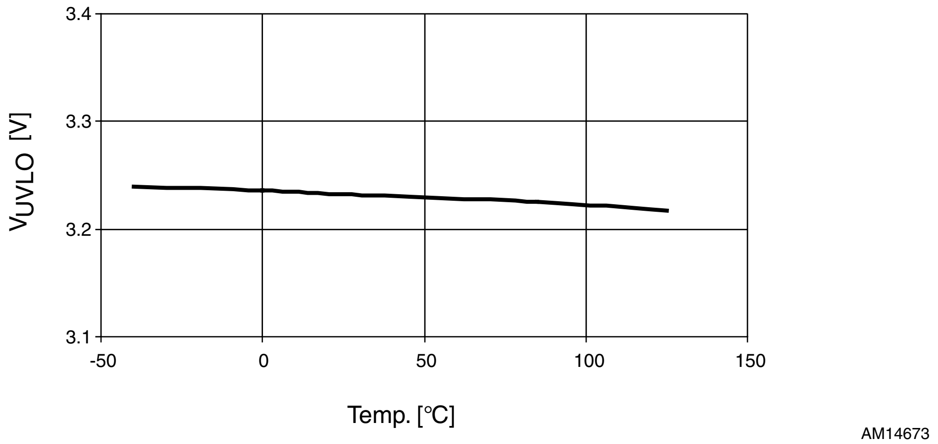


Figure 27. $V_{OL(\overline{FLT})}$ vs. temperature at $I_{SINK(\overline{FLT})}$ = 5 mA, V_{IN} = 5 V

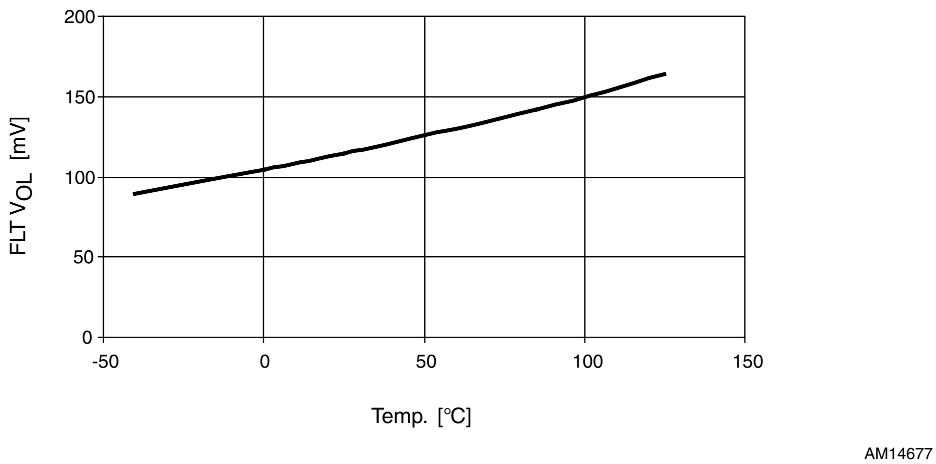


Figure 28. $R_{DS(on)}$ vs. temperature at 5 V, 1 A

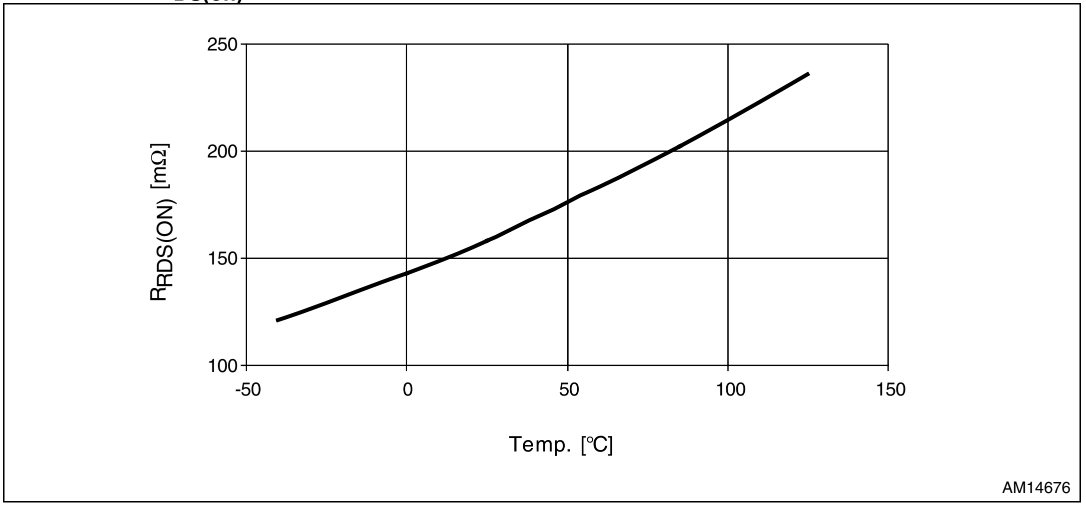


Figure 29. $V_{IL(\overline{EN})}$ vs. temperature

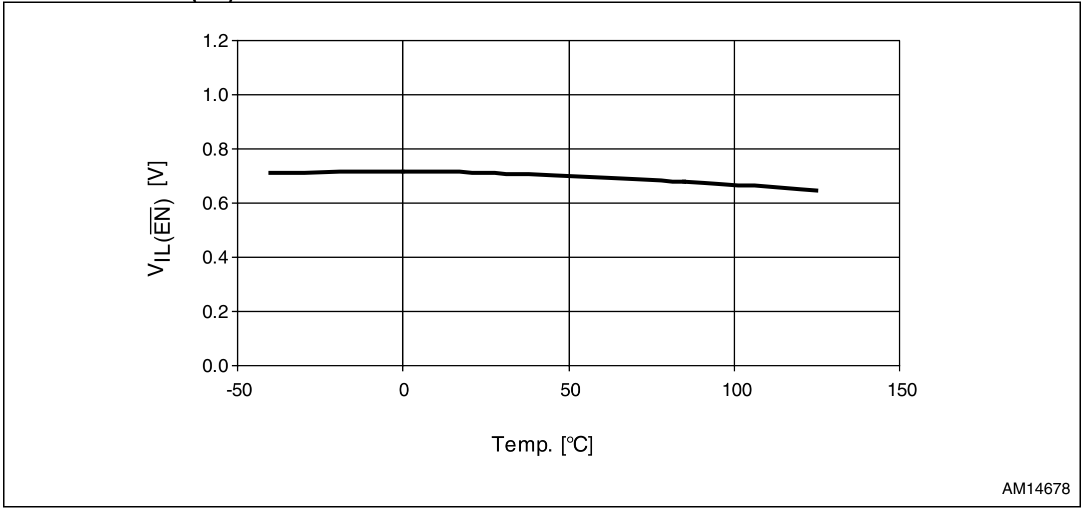


Figure 30. $V_{IH(\overline{EN})}$ vs. temperature

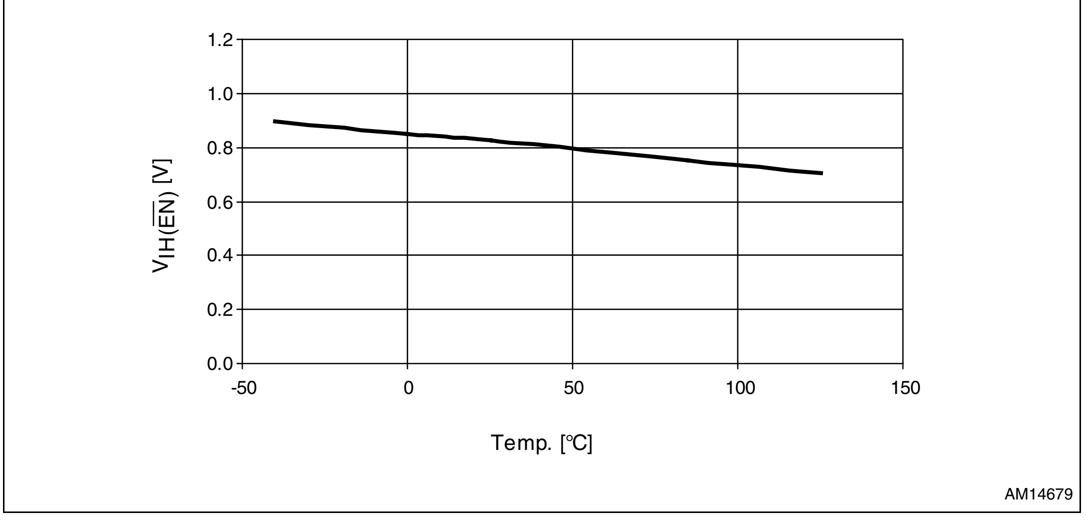


Figure 31. $I_{(\overline{EN})}$ vs. V_{IN} at $V_{(\overline{EN})}$ = 5 V

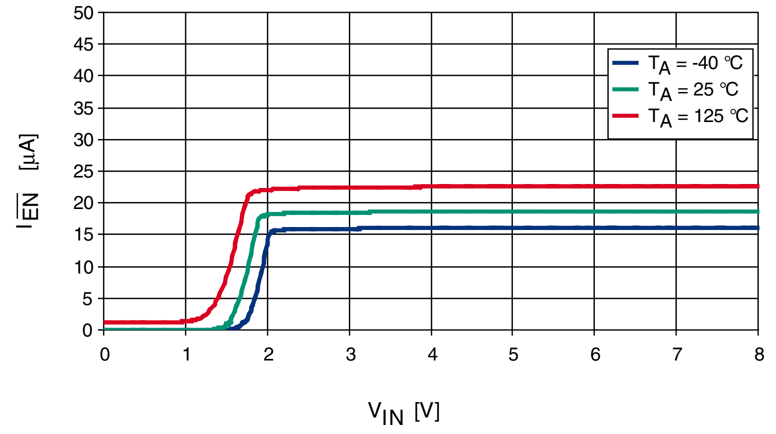


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Figure 32. $R_{PD(\overline{EN})}$ vs. temperature at $V_{(\overline{EN})}$ = V_{IN} = 5 V

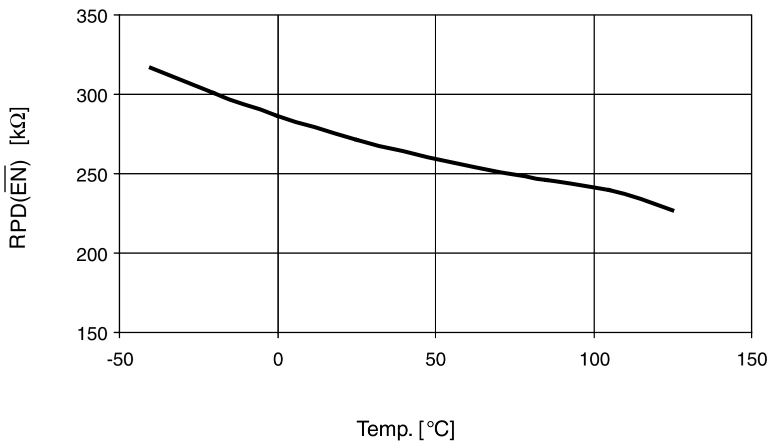

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Figure 33. t_{on} vs. temperature

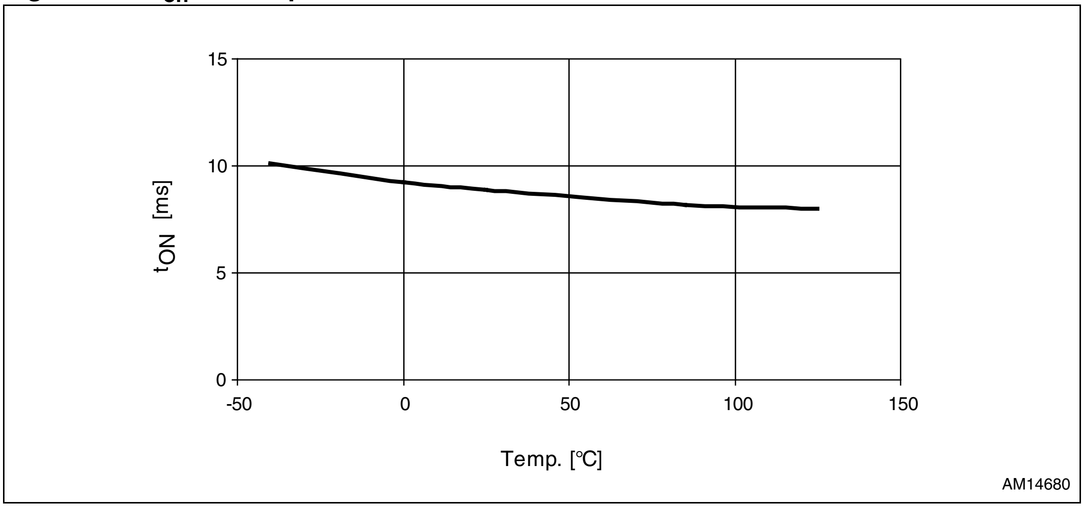
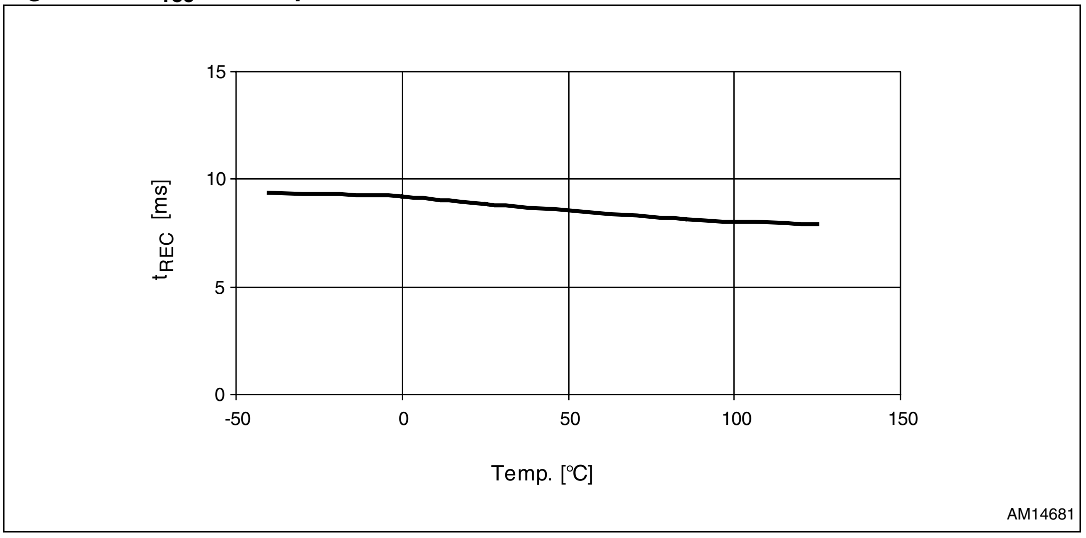


Figure 34. t_{rec} vs. temperature



6 Maximum rating

Stressing the device above the rating listed in *Table 2* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Section 3 on page 10* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics™ SURE program and other relevant documentation.

Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_{STG}	Storage temperature (V_{IN} off)		-55 to 150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds		260	°C
T_J	Operating junction temperature range (internally limited to T_{off})		-40 to 150	°C
V_{IN}	IN pin input voltage		-0.3 to 30	V
V_{OUT}	OUT pin input/output voltage		-0.3 to 12	V
V_{IO}	Input/output voltage (other pins)		-0.3 to 7	V
I_{LOAD}	Load current (IN to OUT)	$T_A \leq 50$ °C	2000	mA
		$T_A = 85$ °C	1500	mA
$I_{REVERSE}$	Reverse diode current (OUT to IN)		500	mA
$I_{SINK(\overline{FLT})}$	$\overline{FLT}$ pin sink current		15	mA
V_{ESD}	ESD withstand voltage (IEC 61000-4-2, IN pin only)(2)		±15 (air), ±8 (contact)	kV
	Human body model (HBM), model = 2(3)		2000	V
	Machine model (MM), model = B(4)		200	V

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.
2. System-level value (see typical application circuit, C1 ≥ 1 µF low ESR ceramic capacitor).
3. Human body model, 100 pF discharged through a 1.5 kΩ resistor according to the JESD22/A114 specification.
4. Machine model, 200 pF discharged through all pins according to the JESD22/A115 specification.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance (junction-to-ambient)	59(1)	°C/W
R_{thJC}	Thermal resistance (junction-to-case)	5.9	°C/W

1. The package was mounted on a 4-layer JEDEC test board with 2 thermal vias connecting from the thermal land to the first buried plane. The 4-layer PCB (2S2P) was constructed based on JESD 51-7 specifications and vias based on JESD 51-5.