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STCCP27A

1.8V/2.8V High speed dual differential line receivers, Compact camera port decoder, I^2C control line

Feature summary

- SUB-Low voltage differential signaling inputs:
  V_{ID} = 100mV with R_T = 100Ω, C_L =10pF
- High signaling rate:
  f_{IN} = 416MHz max (D+,D-, CLK+, CLK-)
  f_{OUT} = 52MHz max (D1-D8, CLK)
- Very high speed:
  t_{pLH}~t_{pHL}=3.5ns (typ) at V_{DD}=2.8V; V_L=1.8V
- Operating voltage range:
  V_{DD}(OPR) = 2.65V to 3.6V
  V_L(OPR) =1.65V to 1.95V
- Symmetrical output impedance
  (D1-D8, H-SYNC, V-SYNC, CLK):
  $|I_{OH}|=I_{OL}$=8mA (min) at V_{DD}=2.65V;V_L=1.8V
- Low power dissipation
  (Disabled: EN=Gnd):
  $I_{SOFF} = I_{DD} + I_L$ = 10µA (max)
- CMOS logic input threshold
  (EN, SYNC_SEL):
  V_{IL} = 0.3xV_{DD}; V_{DD} =2.65V to 3.6V
  V_{IH} = 0.7xV_{DD}; V_{DD} =2.65V to 3.6V
- Bidirectional level translator line
  (I/OV_{DD} - I/OV_L) for I^2C communications:
  400kHz max frequency
  $|I_{OH}|$= 20µA (min.) at V_{DD}=2.8V;V_L=1.8V
  I_{OL} = 1 mA (min.) at V_{DD}=2.8V;V_L=1.8V
- 3.6V Tolerant on inputs (EN, SYNC_SEL)
- Leadfree µTFBGA package
  (RoHS restriction of hazardous substances)

µTFBGA25

.

Description

The STCCP27A receiver converts the subLVDS clock/datastream (up to 416 Mbps throughput bandwidth) back into parallel 8 bits of CMOS/LVTTL. The device recognizes the CCP 32bit start of frame (SOF), end of frame (EOF), start of line (SOL) and end of line (EOL) sequences to generate the H-SYNC and V-SYNC signals. Output LVTTL clock (up to 52 MHz) is transmitted in parallel with data. Input and Output data are rising edge strobe. This chipset is an ideal means to link mobile camera modules to baseband processors. In order to minimize static current consumption, it is possible to shut down the device when the interface is not being used by a power-down (EN) pin that reduces to 10µA the Maximum Current Consumption making this device ideal for portable applications like Mobile Phone, Portable Battery Equipment. Two dedicated I^2C lines are provided to translate bidirectional controls from camera and µC devices. The STCCP27A is offered in a µTFBGA package to optimize PCB space. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity from transient excess voltage. The STCCP27A is characterized for operation over the commercial temperature range -40°C to 85°C.

Order code

Part number	Temperature Range	Package	Comments
STCCP27ATBR	-40 to 85 °C	µTFBGA25 3x3mm (Tape & Reel)	3000 parts per reel

Contents

1 Schematic diagram

Figure 1. Simplified application block diagram

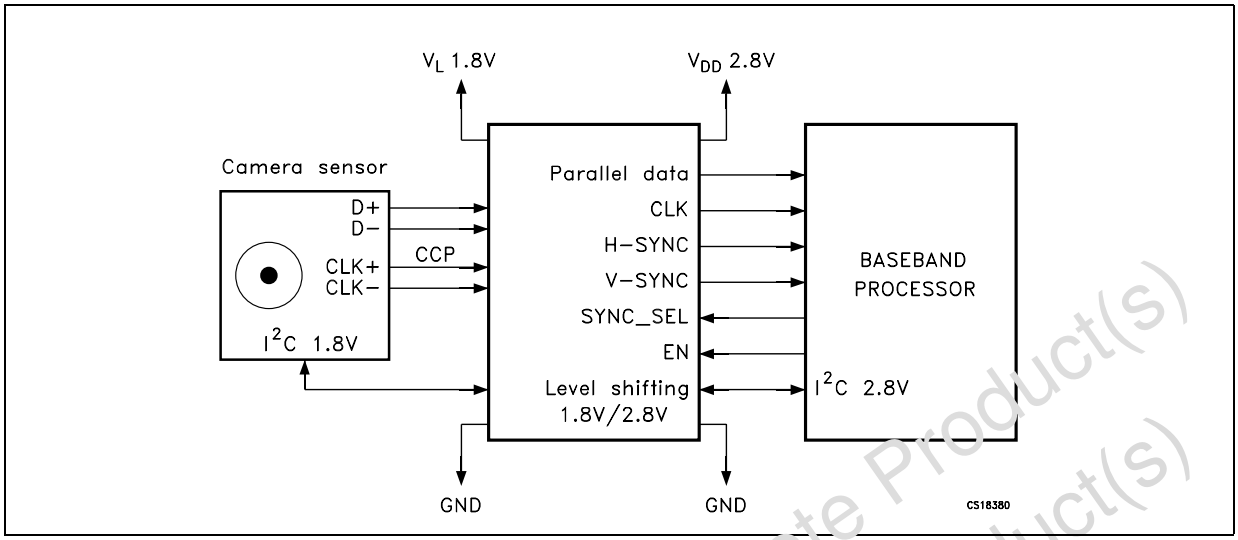


Figure 2. Block diagram

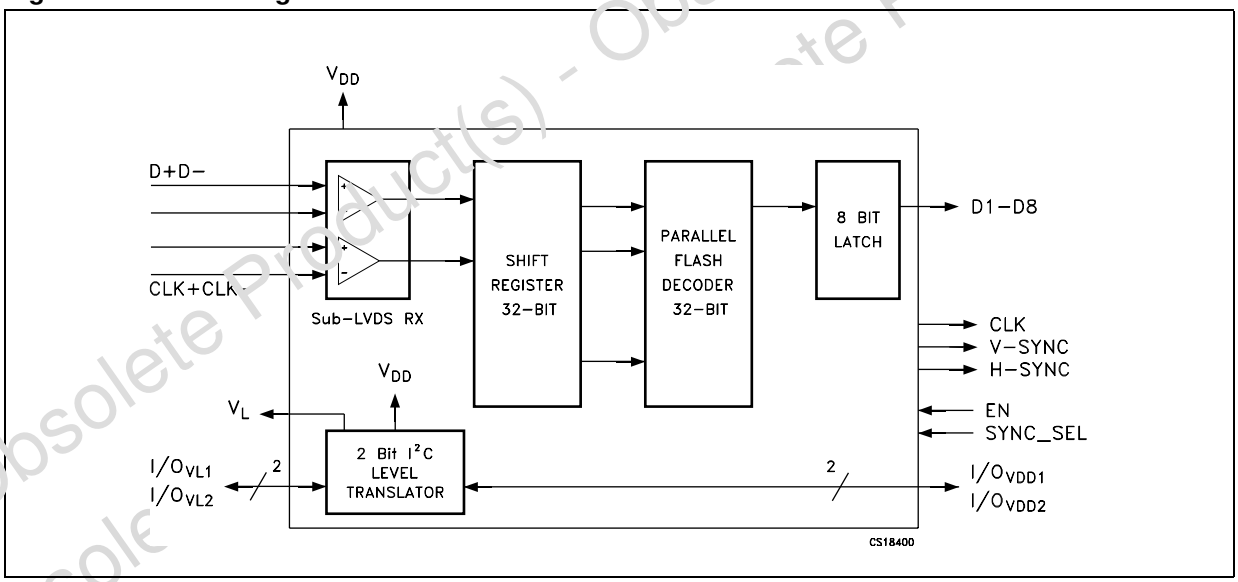
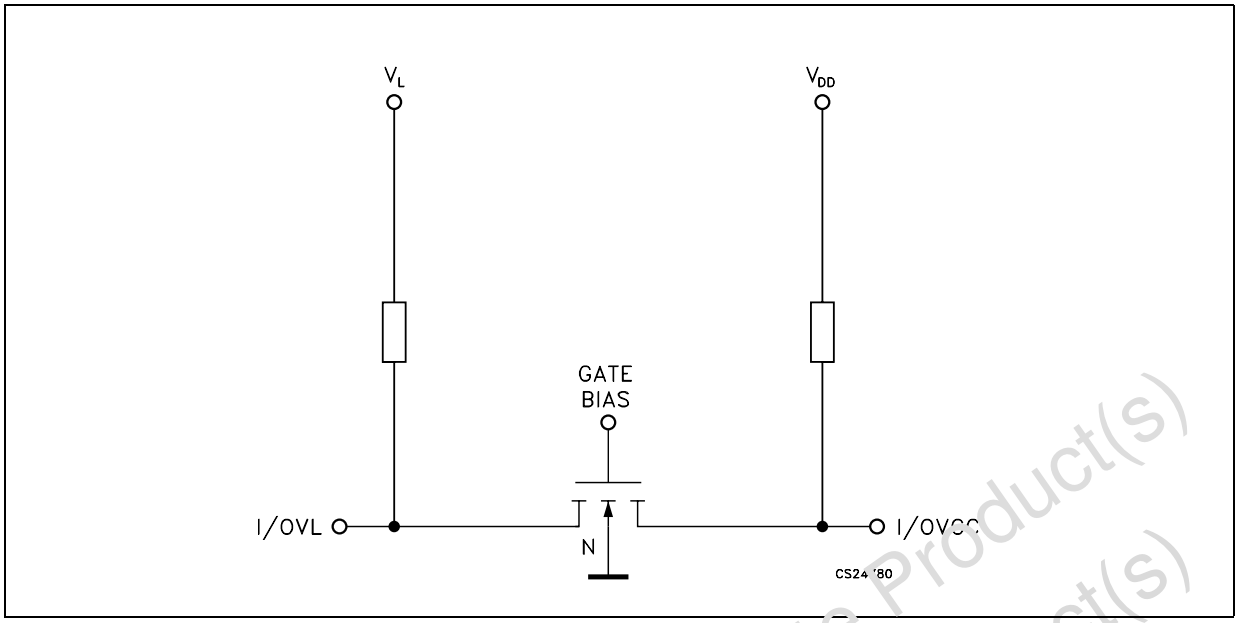


Figure 3. Simplified I^2C line block diagram



2 Pin configuration

Figure 4. Pin configuration (top through view - bumps are on the other side)

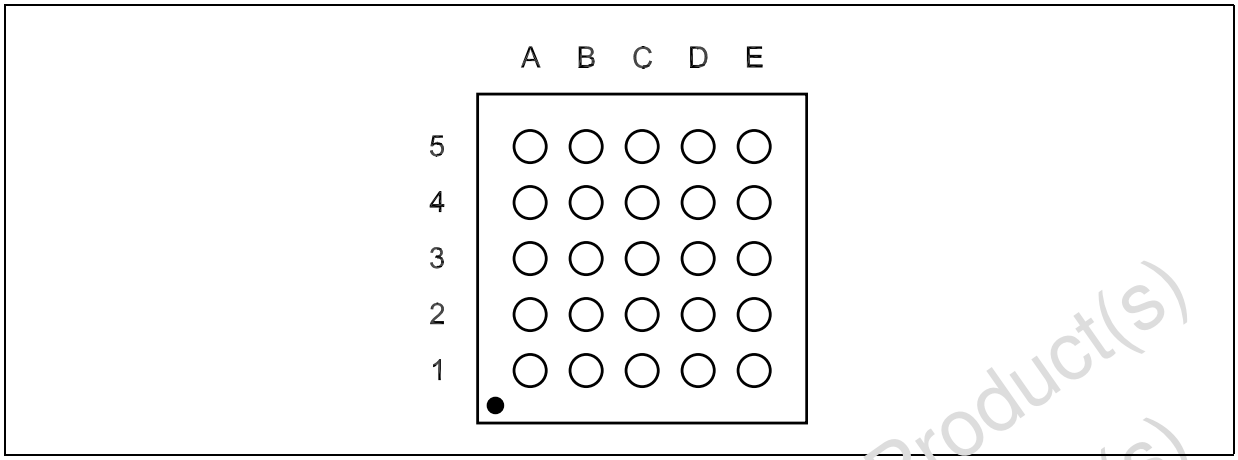


Table 1. Pin description

Pin n°	Symbol	Name and function
D5	D1	Decoder Output (LSB)
E5	D2	Decoder Output
D4	D3	Decoder Output
E4	D4	Decoder Output
D2	D5	Decoder Output
E2	D6	Decoder Output
D1	D7	Decoder Output
E1	D8	Decoder Output (MSB)
A2, A1	D+, D-	Differential Data Receiver Inputs
A5, A4	CLK+, CLK-	Differential CLK Receiver Inputs
B3	EN	Receivers Enable Input
D3	CLK	Clock Output
C3	H-SYNC	Horizontal Sync Output
B2	V-SYNC	Vertical Sync Output
A3, E3	GND	Ground
C5	V_{DD}	Main Supply Voltage
B4	SYNC SEL	Select Sync Input
C1	V_L	Secondary Supply Voltage
B1, C2	I/O_{VL1}, I/O_{VL2}	I^2C Line (V_L Referred)
B5, C4	I/O_{VDD1}, I/O_{VDD2}	I^2C Line (V_{DD} Referred)

Table 2. Main function table

Input						Output				Function
Enable	SYNC_SEL	D+	D-	CLK+	CLK-	V-SYNC	H-SYNC	D1-D8	CLK	
L	X	X	X	X	X	L	L	L	L	CCP disabled
H	H	SOF (FF_H 00_H 00_H 02_H)				H	H	See detailed timing diagram		Start of frame
H	H	EOF(FF_H 00_H 00_H 03_H)				L	L			End of frame
H	H	SOL(FF_H 00_H 00_H 00_H)				No change	H			Start of line
H	H	EOL(FF_H 00_H 00_H 01_H)				No change	L			End of line
H	L	X	X	X	X	L	L	D+, D-	See detailed timing diagram	Disabledsync (D1-D8 will get out data, including sync code)

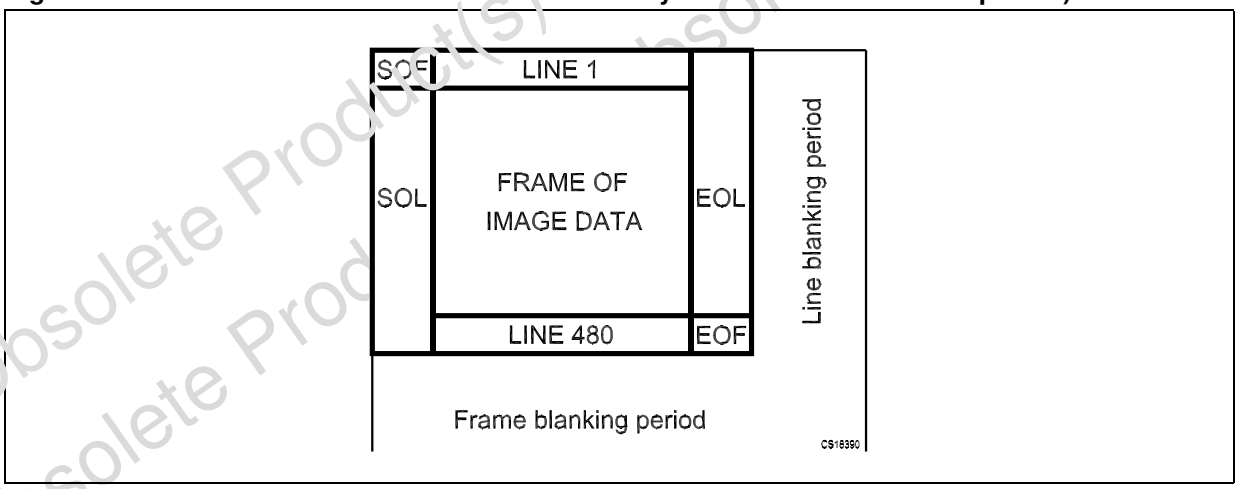
Z = High Impedance, L = Low Voltage Level, H = High Voltage Level, X = Don't care

Table 3. I^2C Bus function table

Enable	I/O Input		Function
	I/O_{VDD}	I/O_{VL}	
X	L	L	I^2C Comm.
X	V_{DD}	V_L	I^2C Comm.
X	Open	V_L	I^2C Comm.
X	V_{DD}	Open	I^2C Comm.

Open: If I/O_{VDD} is not driven then the I/O_{VL} will go in high level V_L by embedded 10kΩ pull-up resistor; If I/O_{VL} is not driven then the I/O_{VCC} will go in high level V_{DD} by embedded 10KΩ pull-up resistor

Figure 5. Frame structure In VGA case (allowed synchronization codes sequence)



3 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Main supply voltage	-0.5 to 4.6	V
V_L	Secondary supply voltage	-0.5 to 4.6	V
V_D	SubLVDS data bus input voltage (D+, D-)	-0.5 to 4.6	V
V_{CLK}	SubLVDS clock bus input voltage (CLK+, CLK-)	-0.5 to 4.6	V
V_I	DC input voltage (SYNC_SEL, EN)	-0.5 to 4.6	V
V_O	DC output voltage (D1-D8, H-SYNC, V-SYNC, CLK, I/O_{VDD})	-0.5 to (V_{DD} + 0.5)	V
$V_{I/OVL}$	DC output voltage (I/O_{VL})	-0.5 to (V_L + 0.5)	V
T_{STG}	Storage temperature range	-65 to +150	°C
ESD	Electrostatic discharge protection HBM Human body model (all pins)	±2	kV

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Main supply voltage	2.65	2.8	3.6	V
V_L	Secondary supply voltage	1.65	1.8	1.95	V
V_{ID}	Differential level input voltage (D+, D-, CLK1+, CLK1-)	0.1		0.4	V
V_{CM}	Common level input voltage (D+, D-, CLK1+, CLK1-)	0.5	0.9	1.3	V
V_{IC}	Level input voltage (SYNC_SEL, EN)			3.6	V
$V_{I/OVDD}$	Level input voltage (I/O_{VDD})			V_{DD}	V
$V_{I/OVL}$	Level input voltage (I/O_{VL})			V_L	V
R_T	Termination resistance (per pair differential input line)	80	100	120	Ω
C_L	Termination capacitance (per line vs gnd pin)		10		pF
T_A	Operating ambient temperature range	-40		85	°C
T_J	Operating junction temperature range	-40		125	°C
t_R, t_F	Rise and fall time (I/O_{VDD}, I/O_{VL}; 10% to 90%; 90% to 10%)			600	ns

4 Electrical characteristics

Table 6. Electrical characteristics (Over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25°C, and V_{DD} = 2.8V, V_L = 1.8V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CM}	Common mode input voltage (see fig.1)	R_T = 100Ω ± 1%	0.5	0.9	1.3	V
I_I	Input leakage current (D+, D-, CLK1+, CLK1-)	V_I = 0.4V			±10	µA
		V_I = 1.4V			±10	µA
I_S	Supply current (I_L + I_{DD})	EN=V_{DD}, I/O_{VL} = V_L, I/O_{VDD} = V_{DD}, D+, CLK+ = Gnd or V_{DD}, D+, CLK+ = V_{DD} or Gnd		3.6	7.0	mA
I_{SOFF}	Shutdown supply current (I_L+ I_{DD})	EN=Gnd, V_{DD}=2.65V to 3.6V V_L=1.65V to 1.95V			10	µA
V_{IH}	HIGH Level input voltage (SYNC_SEL, EN)	V_{DD} = 2.65V to 3.6V V_L = 1.65V to 1.95V	0.7xV_{DD}		3.6	V
V_{IL}	LOW Level input voltage (SYNC_SEL, EN)	V_{DD} = 2.65V to 3.6V V_L = 1.65V to 1.95V	0		0.3xV_{DD}	V
I_{IH}	HIGH Level input current (SYNC_SEL, EN)	V_{IH} = 0.7xV_{DD}			±10	µA
I_{IL}	LOW Level input current (SYNC_SEL, EN)	V_{IL}= 0.3xV_{DD}			±10	µA
V_{OH}	HIGH Level output voltage (D1-D8, H-SYNC, V-SYNC, CLK)	I_{OH} = -8mA	2.0			V
		I_{OH} = -4mA	2.4			V
V_{OL}	LOW Level output voltage (D1-D8, H-SYNC, V-SYNC, CLK)	I_{OL} = +8mA			0.60	V
V_{IH2}	HIGH Level input voltage (I/O_{VL1}, I/O_{VL2})	V_{DD} = 2.65V to 3.6V V_L = 1.65V to 1.95V	0.7xV_L			V
	HIGH Level input voltage (I/O_{VDD1}, I/O_{VDD2})	V_{DD} = 2.65V to 3.6V V_L = 1.65V to 1.95V	0.7xV_{DD}			V
V_{IL2}	LOW Level input voltage (I/O_{VL1}, I/O_{VL2})	V_{DD} = 2.65V to 3.6V V_L = 1.65V to 1.95V	0		0.25	V
	LOW Level input voltage (I/O_{VDD1}, I/O_{VDD2})	V_{DD} = 2.65V to 3.6V V_L = 1.65V to 1.95V	0		0.25	V
V_{OH2}	HIGH Level output voltage (I/O_{VL1}, I/O_{VL2})	I_{OH} = -20µA $V_{I/OVDD}$ = V_{DD}	V_L-0.4			V
	HIGH Level output voltage (I/O_{VDD1}, I/O_{VDD2})	I_{OH} = -20µA $V_{I/OVL}$ = V_L	V_{DD}-0.4			V
V_{OL2}	LOW Level output voltage (I/O_{VL1}, I/O_{VL2}, I/O_{VDD1}, I/O_{VDD2})	I_{OL}= +1mA, $V_{I/OVL}$or $V_{I/OVDD}$ = Gnd			0.35	V

Table 7. Switching characteristics (R_T = 100Ω ± 1%, C_L = 10pF, over recommended operating conditions unless otherwise noted. Typical values are referred to T_A = 25°C and V_{DD} = 2.8V, V_L = 1.8V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_r	Rise time LVTTL Output voltage (10% to 90%)			3.1	4.0	ns
t_f	Fall time LVTTL output voltage (90% to 10%)			2.0	4.0	ns
$t_{r\ I/O}$	Rise time I^2C input/output voltage (20% to 80%)				320	ns
$t_{f\ I/O}$	Fall time I^2C input/output voltage (80% to 20%)				20	ns
t_{pLH}	Propagation delay time (CLK to V-SYNC, H-SYNC) (low to high)			6.5	8.5	ns
t_{pHL}	Propagation delay time (CLK to V-SYNC, H-SYNC) (high to low)			6.5	8.5	ns
t_{pLH}	Propagation delay time (CLK to D1-D8) (low to high)			6.5	8.5	ns
t_{pHL}	Propagation delay time (CLK to D1-D8) (high to low)			6.5	8.5	ns
t_{pLH}	Propagation delay time I^2C input/output voltage (50% to 50%) (Low to High)				100	ns
t_{pHL}	Propagation delay time I^2C input/output voltage (50% to 50%) (High to Low)				10	ns
t_{EN}	Enable delay time (EN to V-SYNC, H-SYNC: t_{PZL}, t_{PZH})	t_{rEN} = 2.0ns (10% to 90%) t_{fEN} = 2.0ns (90% to 10%)			20	µs
t_{DIS}	Disable delay time (EN to V-SYNC, H-SYNC: t_{PLZ}, t_{PHZ})	t_{rEN} = 2.0ns (10% to 90%) t_{fEN} = 2.0ns (90% to 10%)			1000	ns
f_{OPR}	Operating frequency	$t_{rD,CLK}$ = 400ps (10% to 90%) $t_{fD,CLK}$ = 400ps (90% to 10%) $V_{CM\ D,CLK}$ = 0.9V, $V_{DD,CLK}$ = 150mV	1		416	MHz
T_{CLK}	Clock Period		2.4		1000	ns
$t_{SUD-CLK}$	Setup time (D to CLK) (low to high or high to low vs positive CLK edge) (note 1) (see fig. 6)		0.6			ns
t_{HCLK-D}	Hold time (CLK to D) (positive CLK edge to D) (note 1) (see fig. 6)		1.0			ns

Note: 1 50% V_{DIN} to 50% V_{DOUT}

Table 8. Capacitive characteristics

Symbol	Parameter	Test condition		Value			Unit
		V_{DD} (V)		T_A = 25°C			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance (SYNC_SEL, EN)	2.65 to 3.6	V_L = 1.65V to 1.95V, V_I = GND or V_{DD}		3.5		pF

5 Timing diagram

(unless otherwise specified T_A = 25°C)

Figure 6. $t_{SUD-CLK}$, t_{HCLK-D} (Differential input signals D+,D- and CLK+,CLK-)

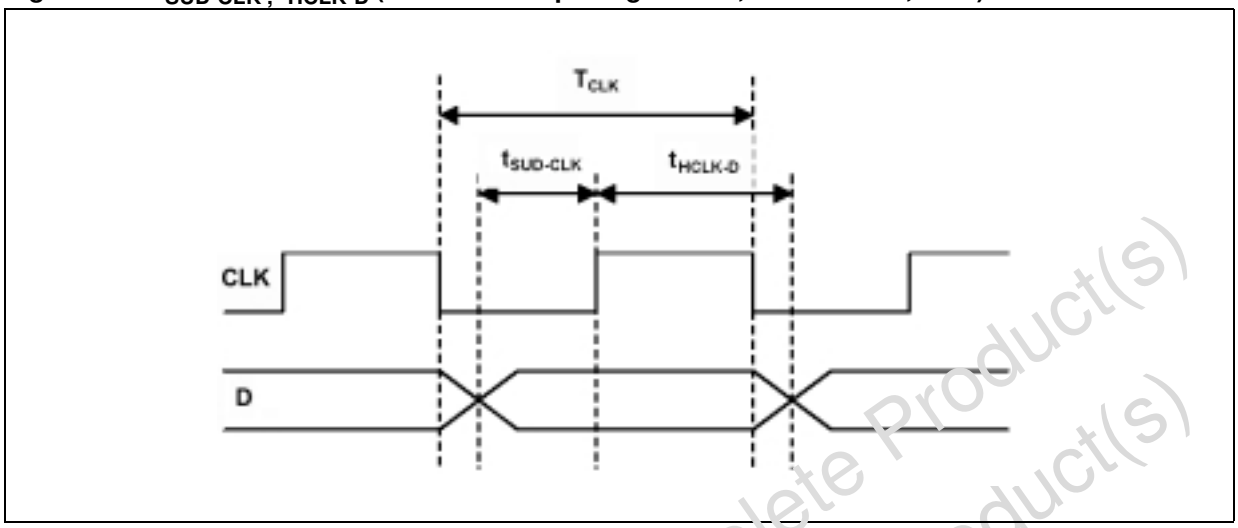
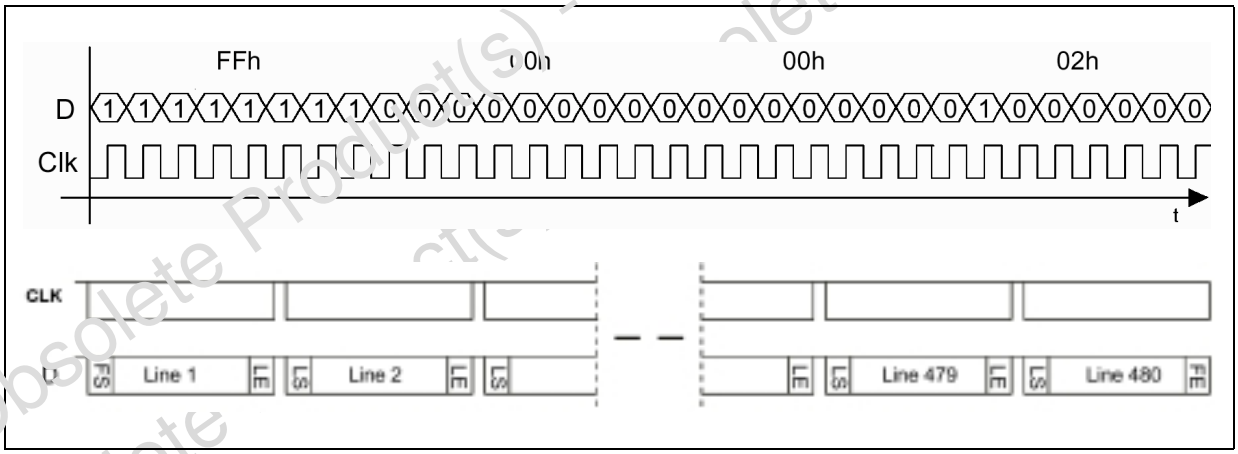


Figure 7. Bit order in synchronization codes and data, LSB first (example start of frame), image frame structure



Note: LSB (bytewise Least Significant Bit first)

Figure 8. Disabled sync mode free running clock IN (SYNC_SEL=GND) (D1-D8 will get out input data DIN, including sync code)

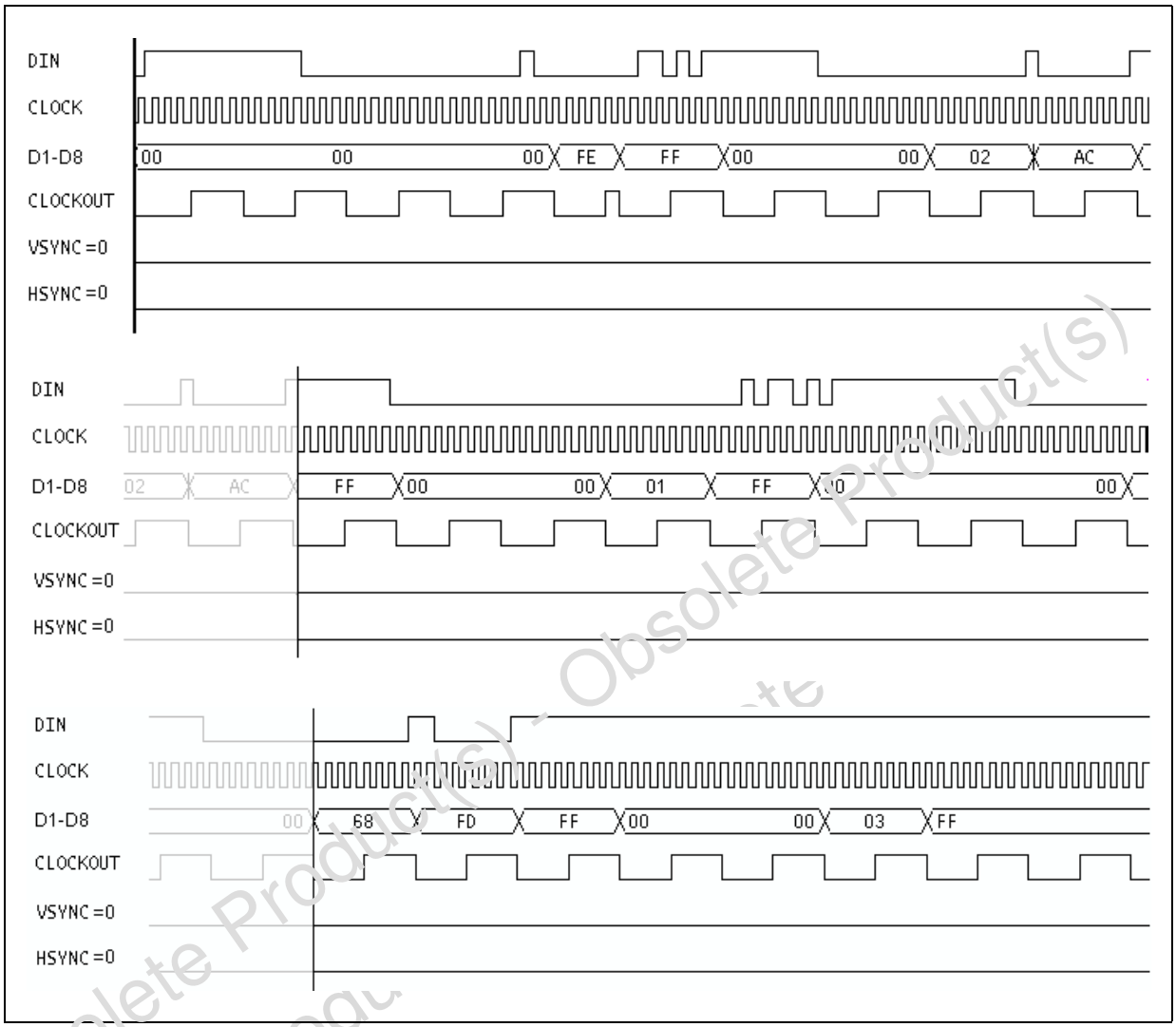


Figure 9. Enabled sync mode free running clock IN (SYNC_SEL=V_{DD}) (D1-D8 will get out input data DIN only, excluding sync code)

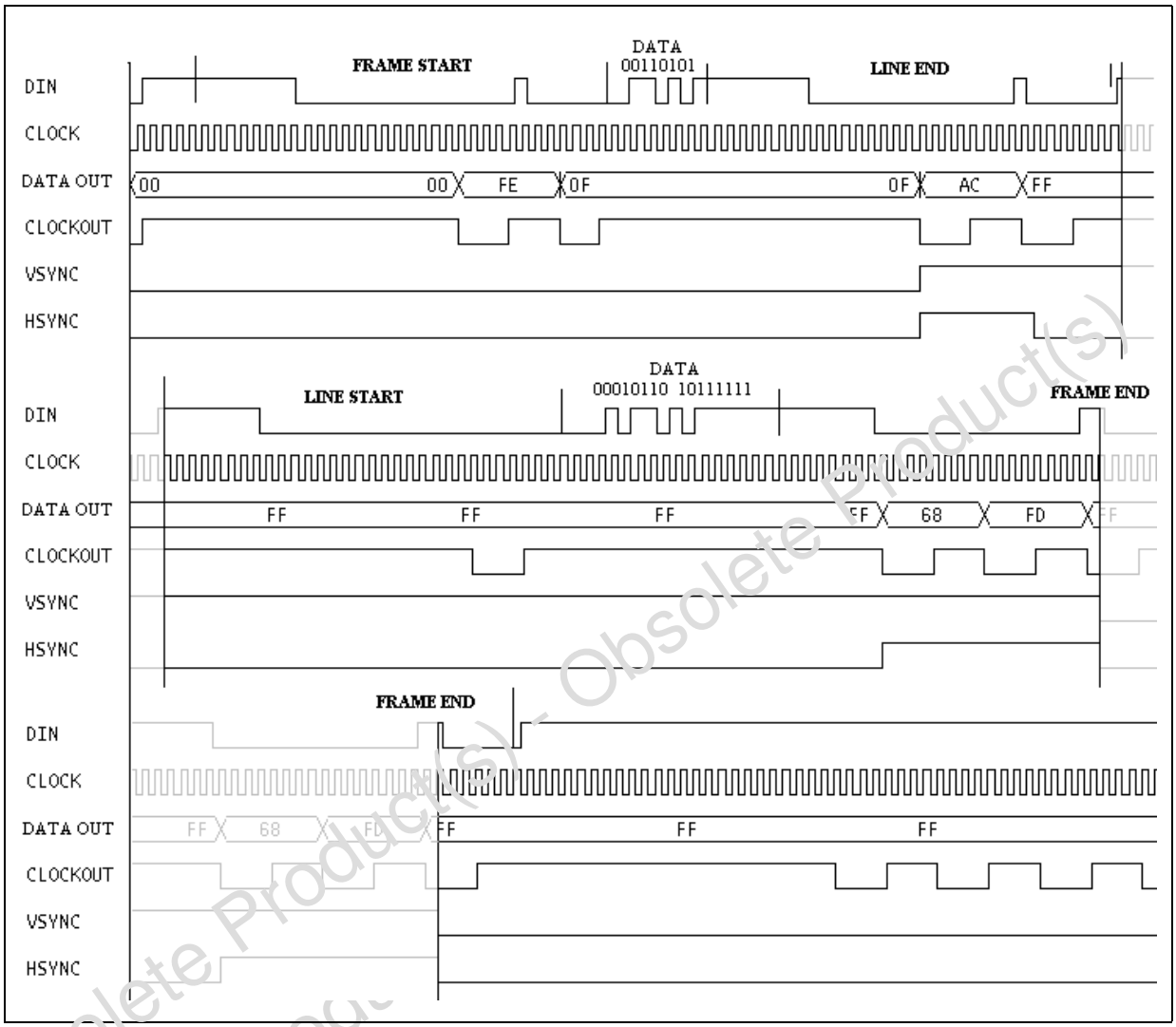


Figure 10. Enabled sync mode gated clock IN (SYNC_SEL=VDD) (D1-D8 will get out input data DIN only, excluding sync code)

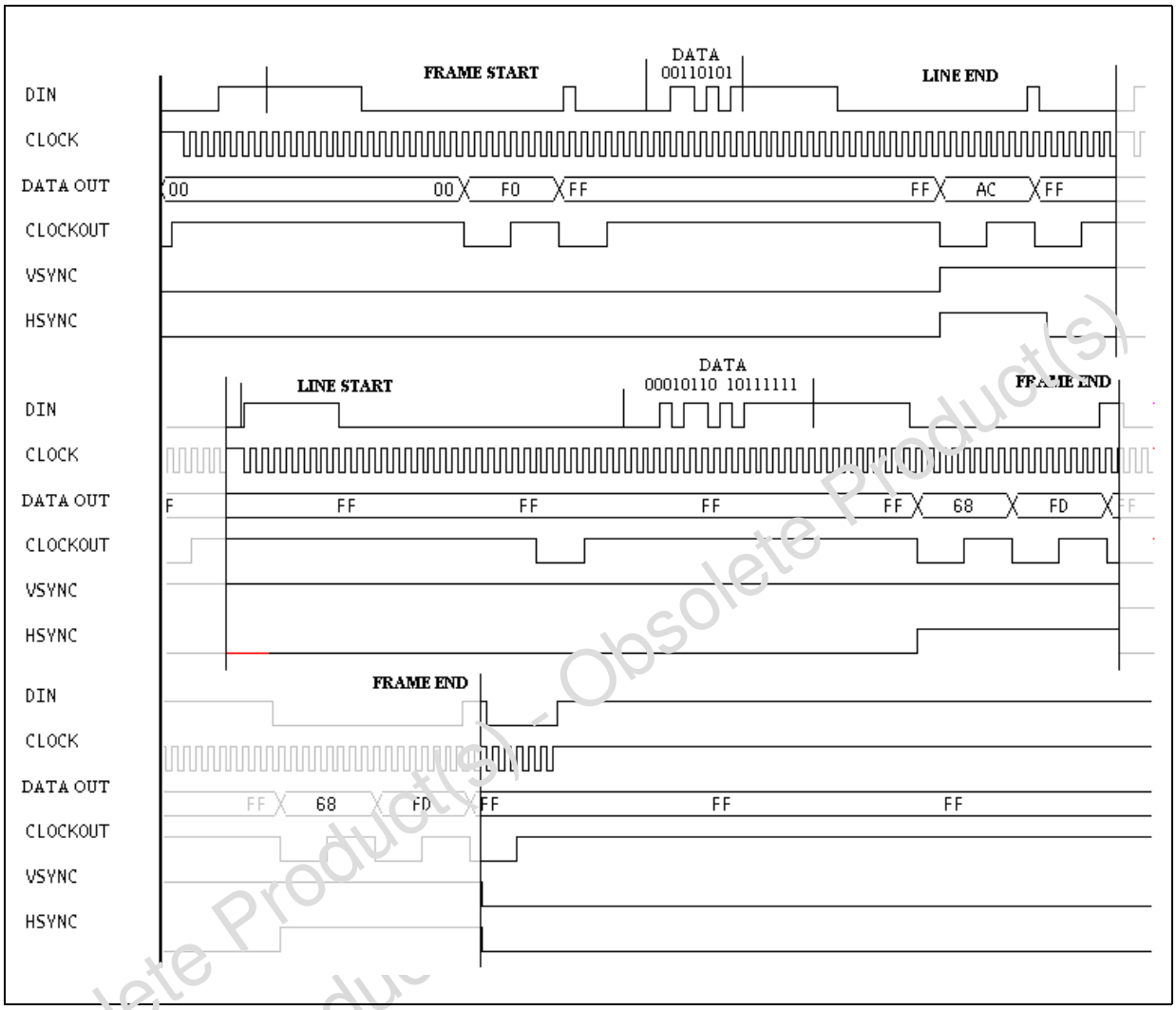


Figure 11. Enabled sync mode free running clock IN (SYNC_SEL=V_{DD}) (D1-D8 will get out input data DIN only, excluding sync code

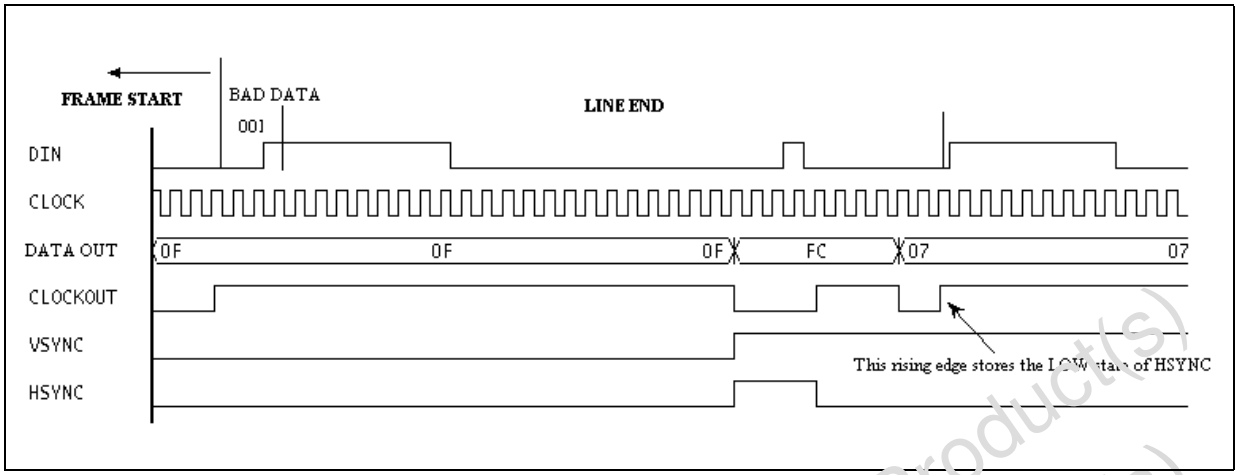
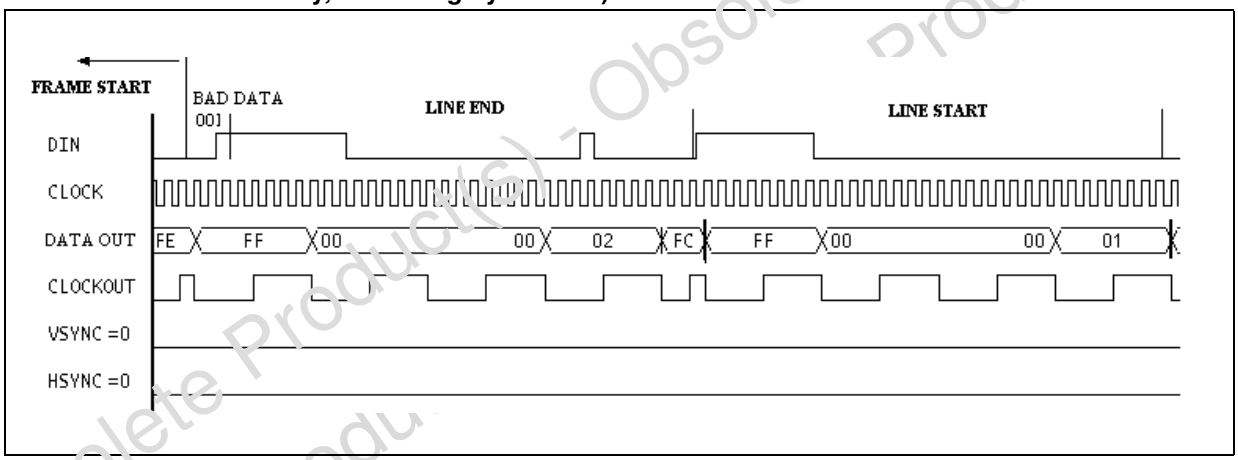


Figure 12. Disabled sync mode free running clock IN (SYNC_SEL=Gnd) (D1-D8 will get out input data DIN only, excluding sync code)

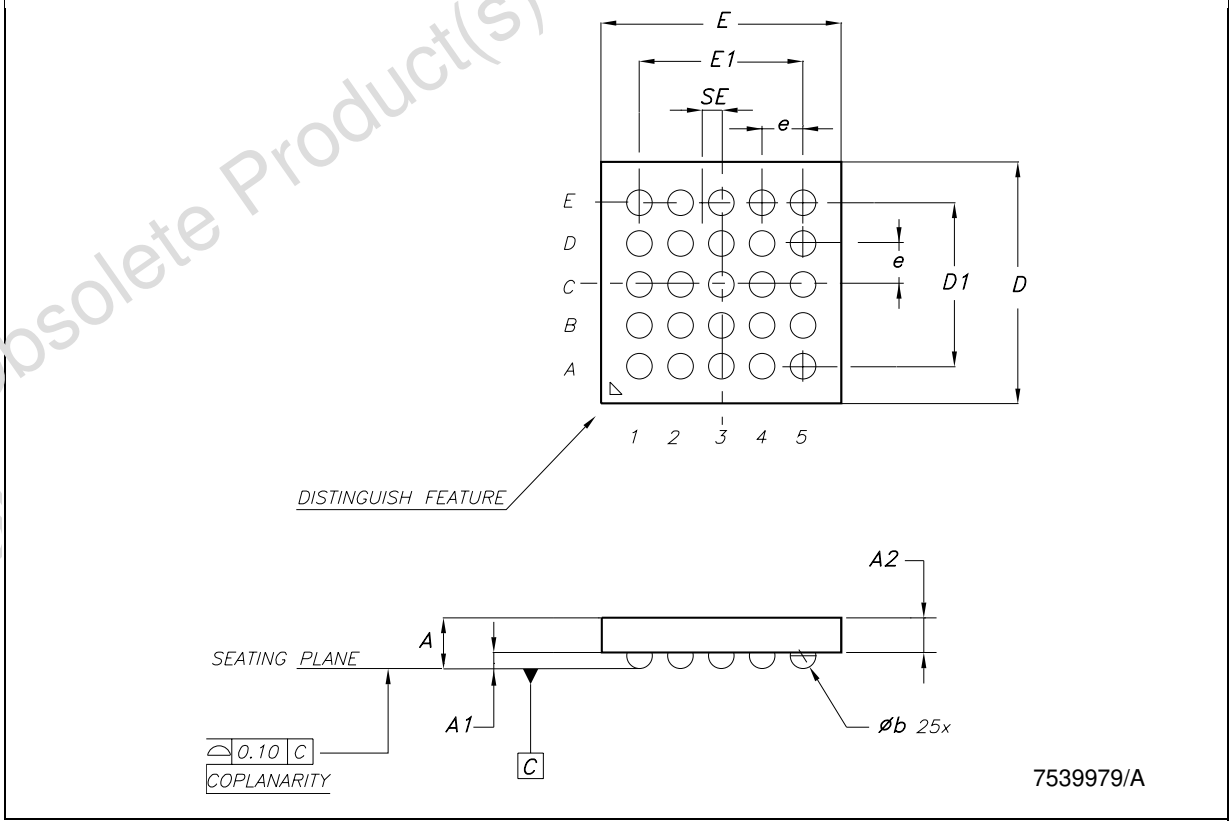


6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

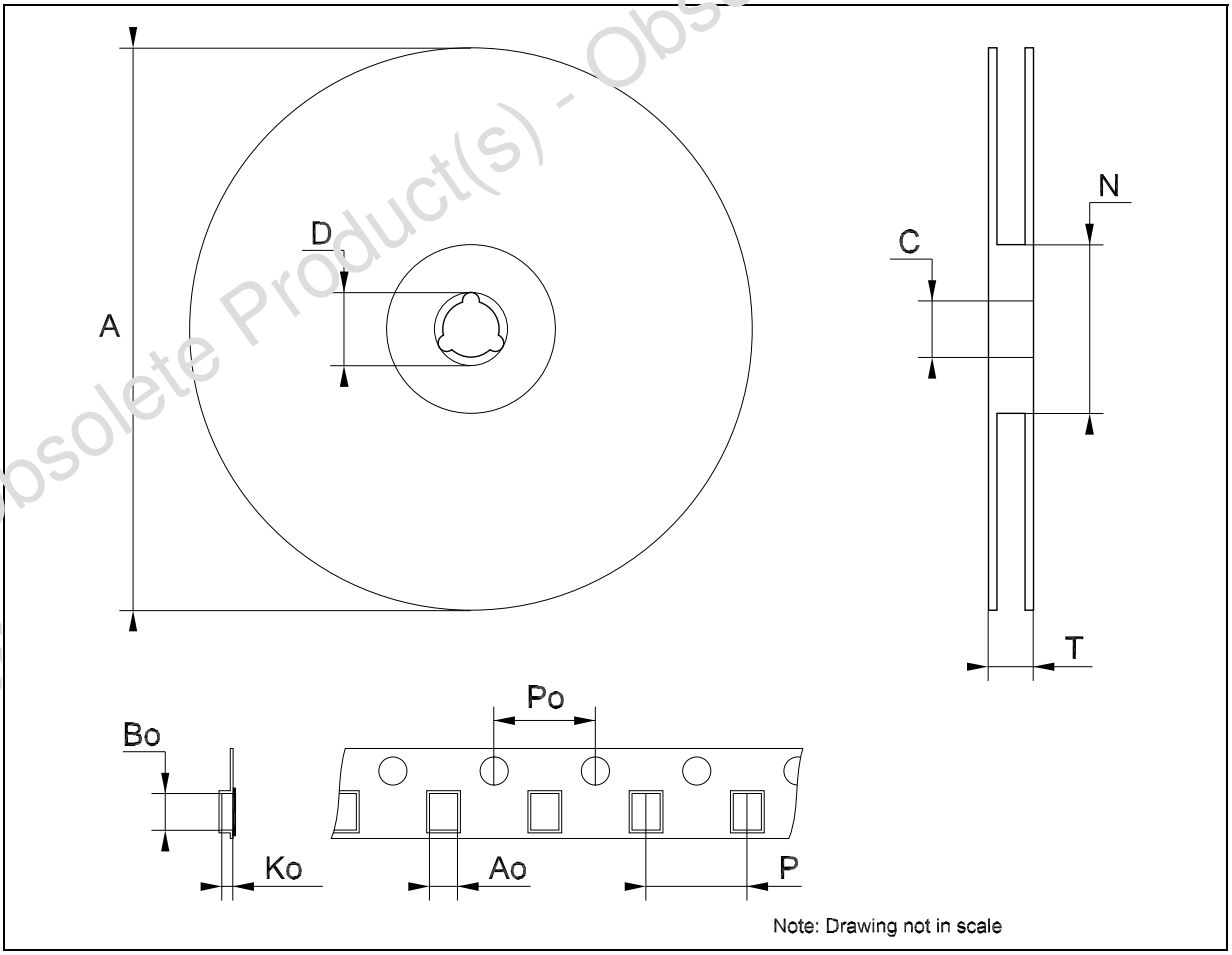
µTFBGA25 MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.0	1.1	1.16	39.4	43.3	45.7
A1			0.25			9.8
A2	0.78		0.86	30.7		33.9
b	0.25	0.30	0.35	9.8	11.8	13.8
D	2.9	3.0	3.1	114.2	118.1	122.0
D1		2			78.8	
E	2.9	3.0	3.1	114.2	118.1	122.0
E1		2			78.8	
e		0.5			19.7	
SE		0.25			9.8	



Tape & Reel TFBGA25 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.60			0.063	
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

7 Revision history

Table 9. Revision history

Date	Revision	Changes
12-Apr-2006	1	Initial release.

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