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STCD1020, STCD1030, STCD1040

Multichannel clock distribution circuit

Features

- 2, 3 or 4 outputs buffered clock distribution
- Single-ended sine wave or square wave clock input and output
- Individual clock enable for each output
- Lower fan-out on clock source
- No AC coupling capacitor needed at the input
- Ultra-low phase noise and standby current
- 2.5 V to 3.6 V supply voltage[a]
- 10 pF typical load driving capability
- Available in TDFN packages
  - STCD1020 - 8-lead (2 mm x 2 mm)
  - STCD1030 - 10-lead (2 mm x 2.5 mm)
  - STCD1040 - 12-lead (2 mm x 3 mm)
- Operating temperature : –40 °C to 85 °C

TDFN (8-, 10- or 12- lead)

Applications

- Multimode RF clock reference
- Baseband peripheral devices clock reference

a. For the 1.65 to 2.75 V version, please contact local ST sales office.

Table 1. Device summary

Order code	Operating temperature range	Channel	Supply	Package
STCD1020RDG6E	–40 °C to 85 °C	2	2.8 V	TDFN8
STCD1030RDH6E[1]	–40 °C to 85 °C	3	2.8 V	TDFN10
STCD1040RDM6F	–40 °C to 85 °C	4	2.8 V	TDFN12

1. Contact local ST sales office for availability.

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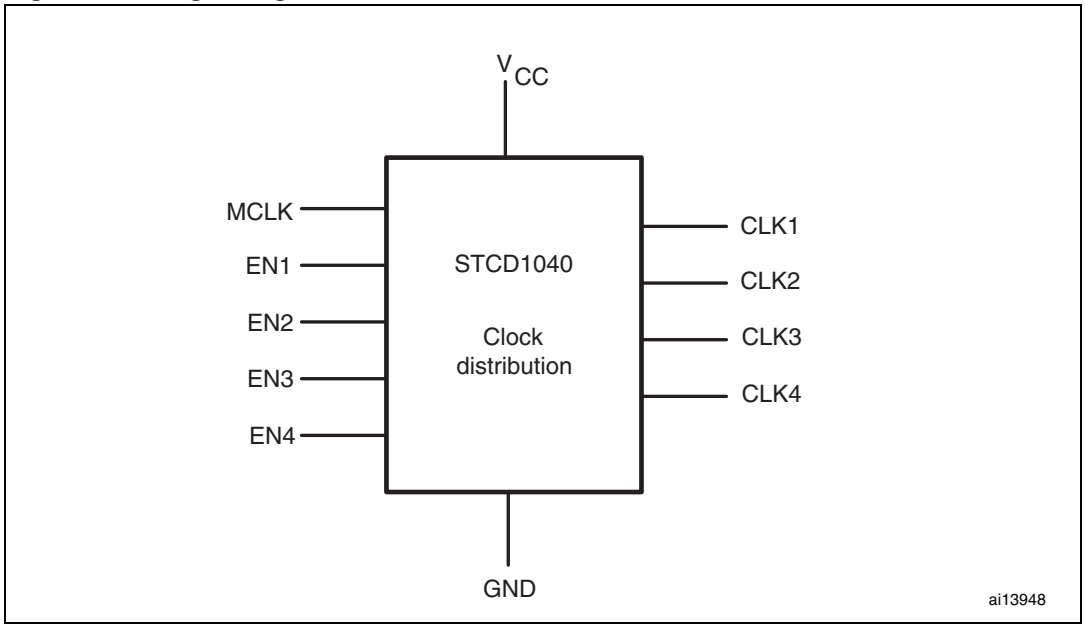
1 Description

The STCD1020, STCD1030 and STCD1040 are 2, 3 or 4 outputs unity gain clock distribution circuits, which are used to provide a common frequency clock to multimode mobile RF applications. It can also be used for those baseband peripheral applications in a mobile phone such as WLAN, Bluetooth, GPS and DVB-H as a clock reference. The STCD1020, STCD1030 and STCD1040 isolate each device driven by their clock outputs and minimize interference between the devices. Each of the clock buffers can be disabled to lower the power consumption if the connected device does not need the clock. The STCD1020, STCD1030 and STCD1040 accept commonly used mobile master clock frequencies ranging from 10 MHz to 52 MHz.

The STCD1020, STCD1030 and STCD1040 are available in 2 mm x 2 mm 8-lead, 2 mm x 2.5 mm 10-lead and 2 mm x 3 mm 12-lead TDFN packages and can be operated with a single 2.8 V (or 1.8 V) supply. The operating temperature is –40 °C to +85 °C.

2 Device overview

Figure 1. Logic diagram



Note: No EN3, EN4, CLK3 nor CLK4 for STCD1020 and no EN4 nor CLK4 for STCD1030.

Figure 2. Connections diagram (STCD1020, 2-channel)

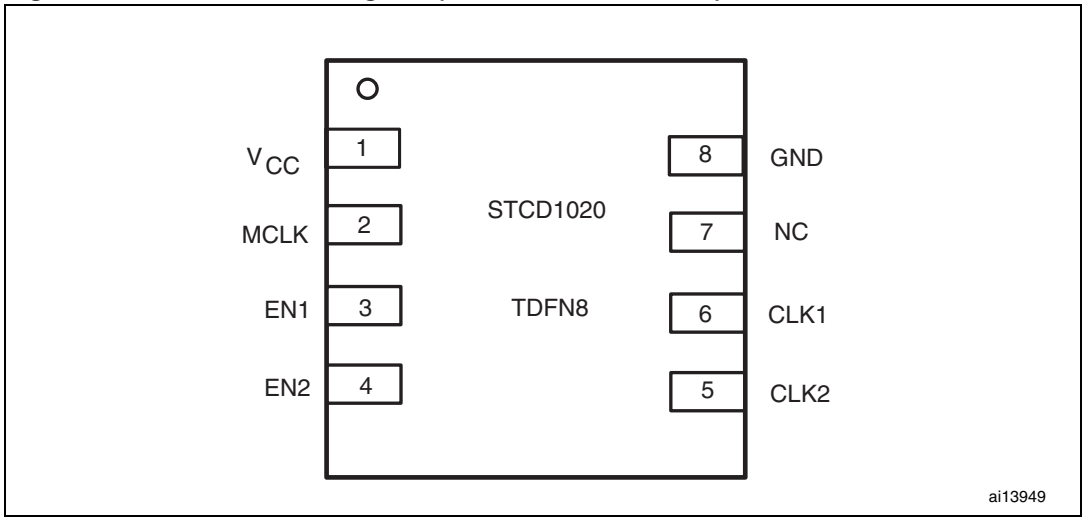


Figure 3. Connections diagram (STCD1030, 3-channel)

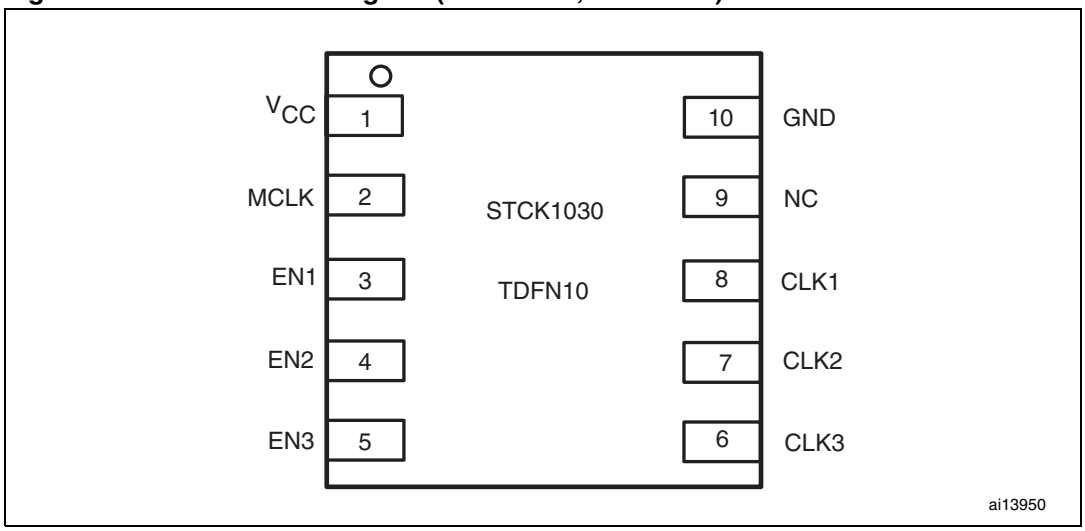


Figure 4. Connections diagram (STCD1040, 4-channel)

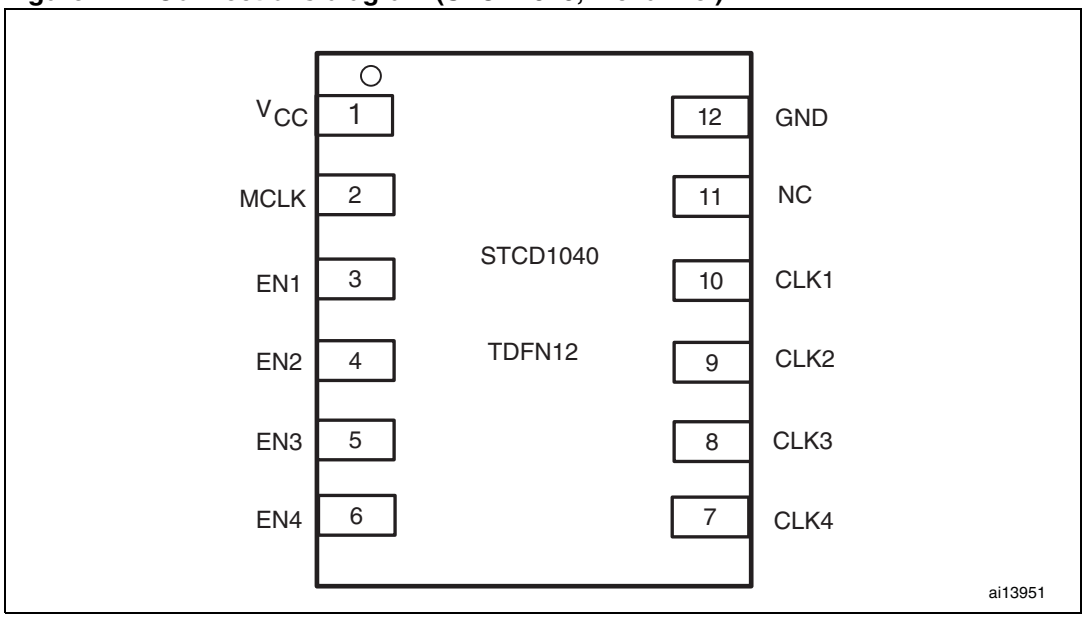


Table 2. Pin names and functions

Pin	Type	Function
CLK1, CLK2, CLK3, CLK4	Output	Clock output channel #1, #2, #3, #4. A 0.001 µF DC cut capacitor needed outside.
EN1, EN2, EN3, EN4	Input	Clock output channel #1, #2, #3, #4 enable, active high
MCLK	Input	Master clock input
V_{CC}	Supply	Supply voltage. Bypass to GND with a 0.1 µF capacitor.
GND	Supply	Supply ground
NC		Not connected

Figure 5. Block diagram

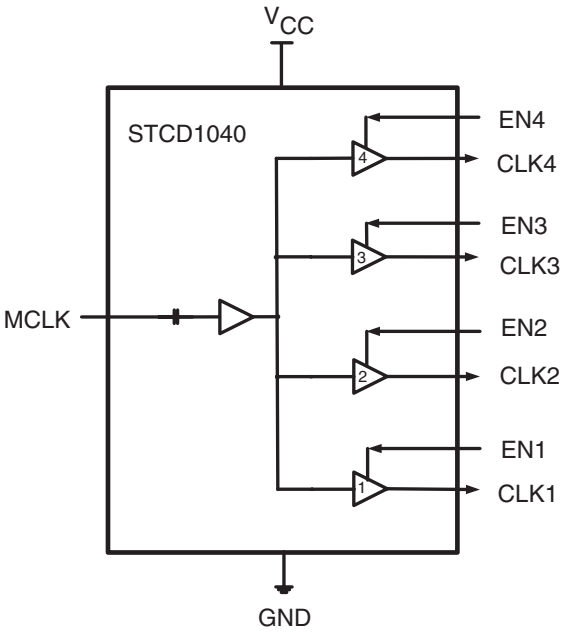
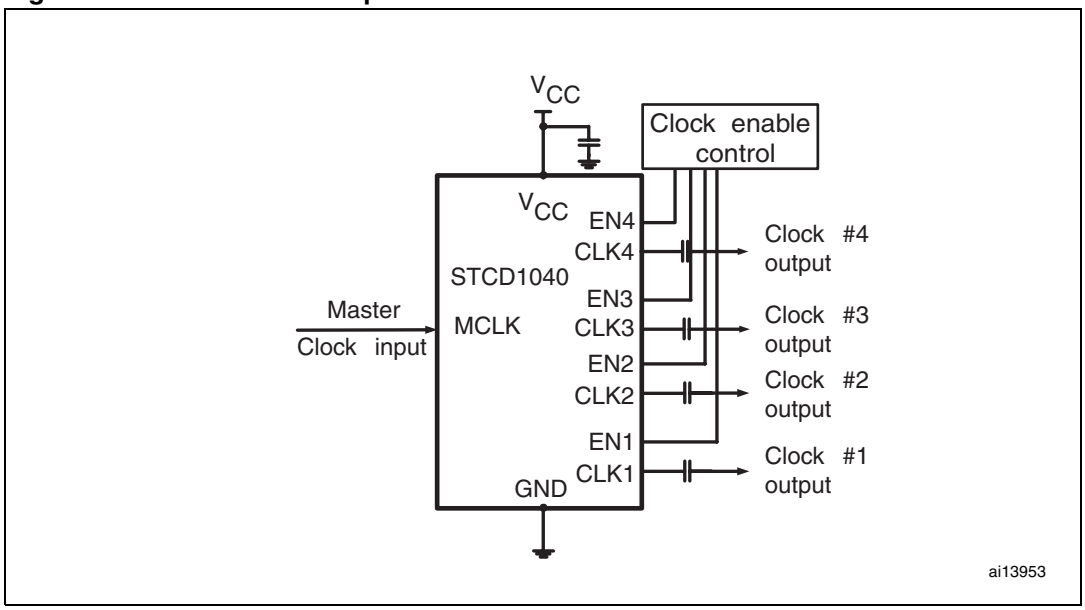


Figure 6. Hardware hookup



3 Device operation

The STCD1020, STCD1030 and STCD1040 are 2, 3 or 4 buffered unity gain clock distribution circuits. They accept the clock input from an external clock source and send 2, 3 or 4 buffered outputs to different devices.

Each clock output of the STCD1020, STCD1030 and STCD1040 can be enabled for the device connected to it. If the device connected is in standby and does not require a clock, the buffer can be disabled to save power consumption. If all the devices connected are in standby, the STCD1020, STCD1030 and STCD1040 will also be put into standby mode for further power consumption saving. The enable signals and output clock signals truth table are given in *Table 3*.

The input DC cut capacitor is embedded in STCD1020, STCD1030 and STCD1040. A capacitor outside is needed for each of the clock outputs. The STCD1020, STCD1030 and STCD1040 are internally biased at 1/2 V_{CC} DC voltage level at the outputs.

Table 3. Truth table for enable signals (EN 1-4) and output clocks (CLK1-4)

EN1	EN2	EN3	EN4	CLK1	CLK2	CLK3	CLK4
0	0	0	0	NO CLOCK	NO CLOCK	NO CLOCK	NO CLOCK
1	0	0	0	CLOCK	NO CLOCK	NO CLOCK	NO CLOCK
1	1	0	0	CLOCK	CLOCK	NO CLOCK	NO CLOCK
...	...	...	...	...	...	...	...
1	1	1	1	CLOCK	CLOCK	CLOCK	CLOCK

Note: "0" means logic low and "1" means logic high. When NO CLOCK outputs, the CLKx pins stay at high impedance.

4 Application information

4.1 Typical applications

The STCD1020, STCD1030 and STCD1040 distribute a source clock (for example, from VCTCXO) to 2, 3 or 4 channel outputs. The typical application circuits using STCD1040 are shown in *Figure 7* and *Figure 8* below.

In *Figure 7*, the clock from VCTCXO is distributed to the TD-SCDMA transmitter and receiver and GSM transceiver separately.

In *Figure 8*, the buffer #4 output is fed into the Bluetooth system. In order to allow minimum power consumption, a Bluetooth system always has a clock request feature. If the Bluetooth system does not require the clock, the clock request will disable the clock output.

The enable pins can also be connected to logic high to let the channel output always on. If the channels of STCD1020, STCD1030 and STCD1040 are not used in the application, the enable pins of the channels should be connected to ground on PCB.

Figure 7. Typical application circuit using STCD1040 for RF ends of TD-SCDMA/GSM dual-mode mobile phone

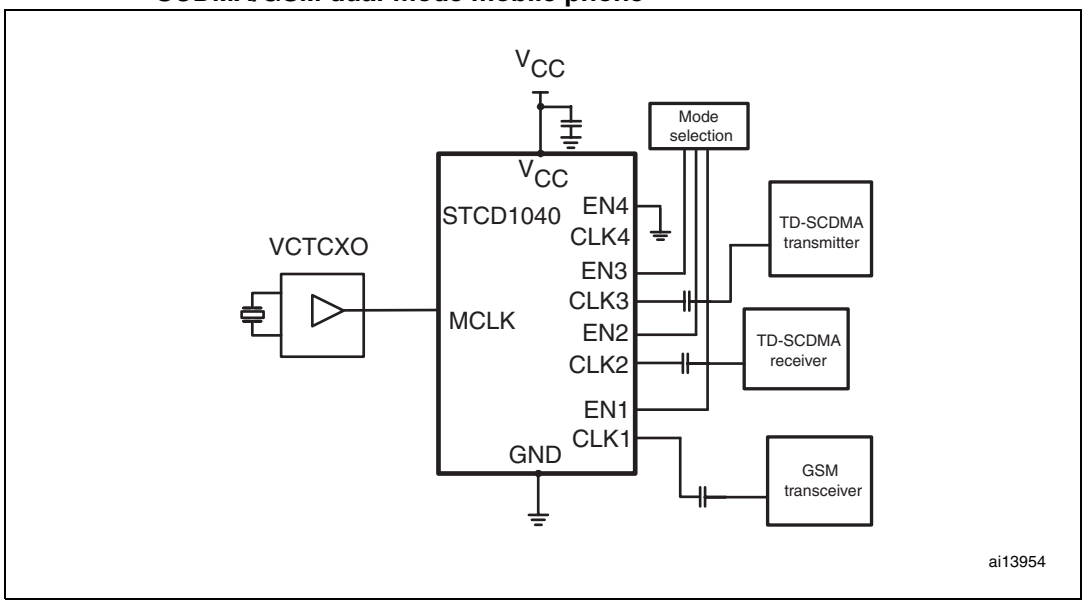
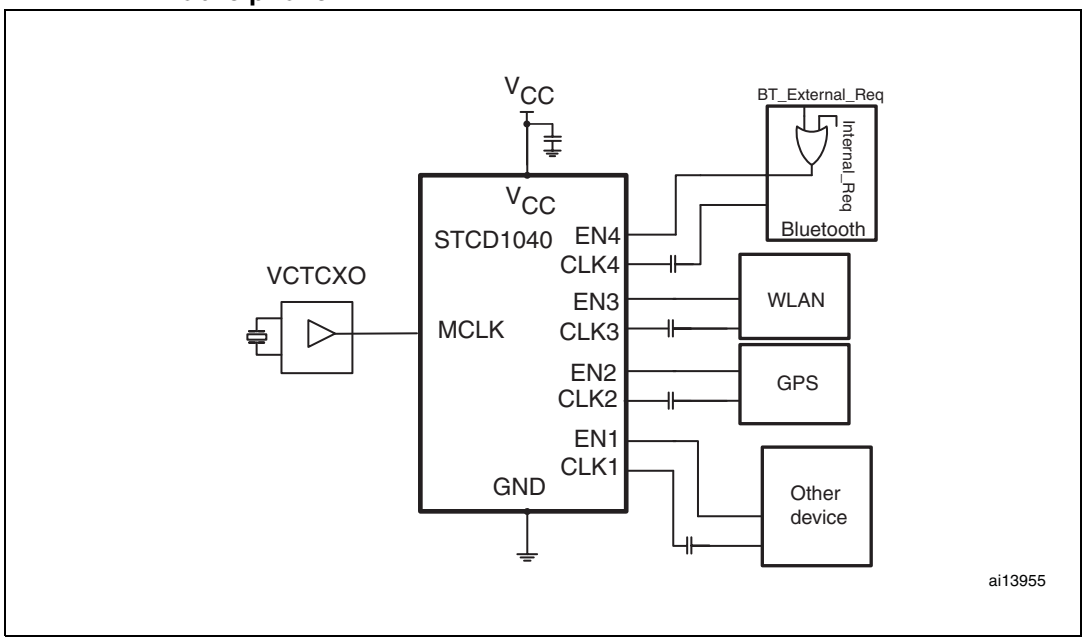


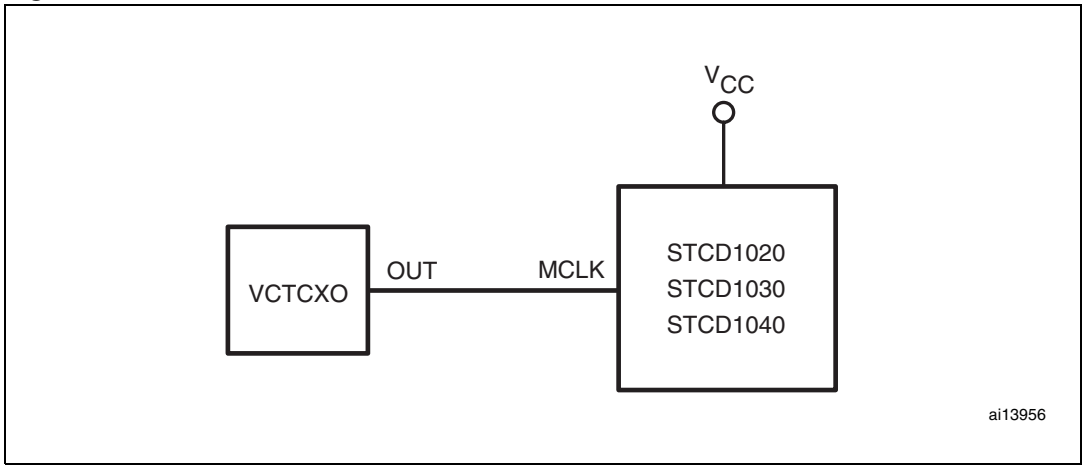
Figure 8. Typical application circuit using STCD1040 for baseband peripherals in mobile phone



4.2 Connection of the source clock to MCLK

If the output of the clock source voltage level is within the supply rails of the STCD1020, STCD1030 and STCD1040, the output of the source clock should be connected directly to the MCLK of the clock distribution circuits. This is described in *Figure 9*. The direct connection of the source clock is the common case and a DC-CUT capacitor is saved on PCB.

Figure 9. Direct connection of the source clock

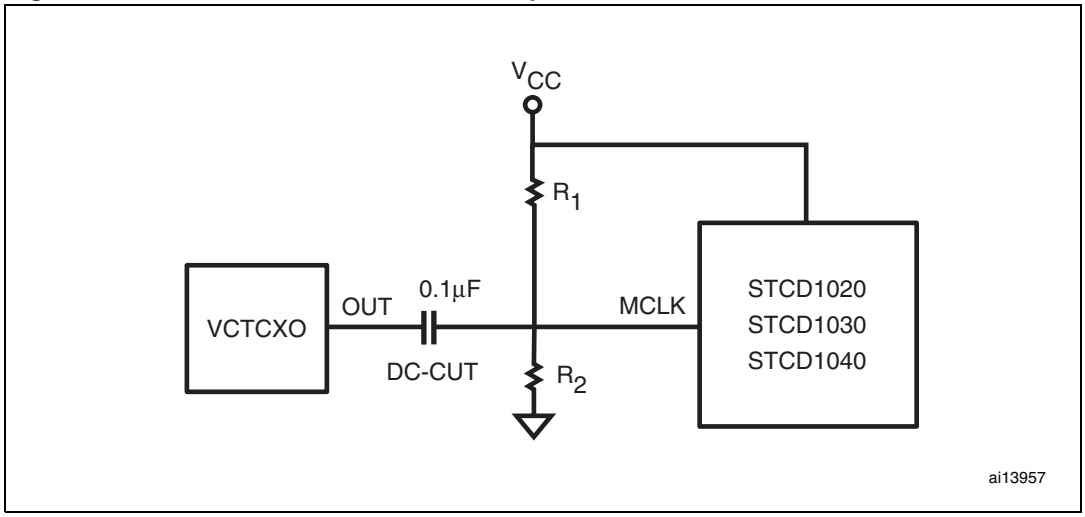


Note: The input clock voltage level of the STCD1020, STCD1030, and STCD1040 cannot exceed the supply rails when it is directly connected to the source clock. If it is needed to connect a source clock with the voltage level exceeds the supply rails of the clock distribution circuits, the user needs to connect a DC-CUT capacitor serially as shown in Figure 10. A voltage divider formed by a resistor string is also needed to set a proper DC bias for the clock input

of the STCD1020, STCD1030 and STCD1040. The proper DC voltage is around half of the supply.

The connection of the DC-CUT capacitor and bias for the STCD1020, STCD1030 and STCD1040 is only needed when the output of VCTCXO voltage level exceeds the supply of the clock distribution circuit (see *Figure 10*).

Figure 10. Connection of the DC-CUT capacitor and bias



5 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings (1.8 V supply)

Symbol	Parameter		Value	Unit
T_{STG}	Storage temperature (V_{CC} off)		–55 to 150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds		260	°C
T_J	Maximum junction temperature		150	°C
V_{CC}	Supply voltage		–0.3 to 3.6	V
V_{IN}	Input voltage level		–0.3 to 3.6	V
V_{EN}	Voltage on enable pins		–0.3 to 3.6	V
θ_{JA}	Thermal resistance (junction to ambient)	TDFN8	149.0	°C/W
		TDFN10	136.6	°C/W
		TDFN12	132.4	°C/W

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

Table 5. Absolute maximum ratings (2.8 V supply)

Symbol	Parameter		Value	Unit
T_{STG}	Storage temperature (V_{CC} off)		–55 to 150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds		260	°C
T_J	Maximum junction temperature		150	°C
V_{CC}	Supply voltage		–0.3 to 6	V
V_{IN}	Input voltage level		–0.3 to 6	V
V_{EN}	Voltage on enable pins		–0.3 to 6	V
θ_{JA}	Thermal resistance (junction to ambient)	TDFN8	149.0	°C/W
		TDFN10	136.6	°C/W
		TDFN12	132.4	°C/W

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

6 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the measurement conditions summarized in *Table 6*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 6. Operating and AC measurement conditions (1.8 V supply)

Parameter	Condition	Unit
V_{CC} supply	1.65 to 2.75	V
Output clock voltage (CLK1…CLK4)	0 to V_{CC}	V
Device enable voltage (EN1…EN4)	0 to V_{CC}	V
Ambient operating temperature (T_A)	–40 to +85	°C

Table 7. DC and AC characteristics (1.8 V supply)

Symbol	Parameter	Condition(1)	Min	Typ	Max	Unit
f_{MCLK}	Master clock (eg. from VCTCXO)	Sine wave/square wave	10	26	52	MHz
V_{CC}	Supply voltage		1.65	1.8	2.75	V
Vin	Input clock voltage level(2)		0.75	1		Vpp
Vout	Output gain level(3)	C_L = 10 pF	–1.5	–0.5		dB
I_Q	Quiescent current(4)	2 buffers version		1.6	2.6	mA
		3 buffers version		2.0	3.3	
		4 buffers version		2.6	4	
I_{ACT}	Active current(5)	1 channel enabled		1.7		mA
		2 channels enabled		2.2		
		3 channels enabled		2.7		
		4 channels enabled		3.2		
I_{SB}	Standby current	All buffers disabled			1	µA
R_{IN}	Input resistance	At DC level		>100		kΩ
C_{IN}	Input capacitance	f = 26 MHz		3	4	pF
$t_{r/f}$	Rise/fall time(6)	Vin = 1 Vpp, C_L = 10 pF Square wave input/output		2	5	ns
BW	Signal bandwidth(3)	Vin = 1 Vpp, –1 dB, C_L = 10 pF Sine wave input/output		52		MHz
V_{ENH}	Enable voltage high(7)	EN1~EN4	1.2			V
V_{ENL}	Enable voltage low(7)	EN1~EN4			0.6	V

Table 7. DC and AC characteristics (1.8 V supply)

Symbol	Parameter	Condition(1)	Min	Typ	Max	Unit
P_N	Additive phase noise(3)(8)	at 1 kHz offset		–135		dBc/Hz
		at 10 kHz offset		–145		
		at 100 kHz offset		–150		
t_{RECB}	Buffer recovery time from off to on	STCD10x0 active		20		µs
t_{RECC}	STCD10x0 active recovery time from standby to active			50		µs
C_L	Capacitive load for each channel			10	20	pF
R_L	Resistive load for each channel		10			kΩ

1. Valid for ambient operating temperature: T_A = –40 °C to 85 °C; V_{CC} = 1.65 V to 2.75 V; typical T_A = 25 °C; Load capacitance = 10 pF (except where noted).
2. Clock input voltage level should not exceed supply rails.
3. Simulated and determined via design and NOT 100% tested.
4. The quiescent current is measured when the enable pins are active, but without input master clock signal (fmclk = 0 Hz).
5. The active current is dependent on the master clock input Vpp and frequency and the capacitive load condition. The typical test condition is 26 MHz sine wave with 1 Vpp master clock input, C_L = 10 pF.
6. The rise time is measured when clock edge transfers from 10% V_{CC} to 90% V_{CC}. The fall time is measured when clock edge transfers from 90% V_{CC} to 10% V_{CC}.
7. Other test results are under test condition V_{ENH} = 1.8 V and V_{ENL} = 0 V.
8. Guaranteed with the supply noise of 30 µ Vrms from 300 Hz to 50 kHz.

Table 8. Operating and AC measurement conditions (2.8 V supply)

Parameter	Condition	Unit
V_{CC} supply	2.5 to 3.6	V
Output clock voltage (CLK1…CLK4)	0 to V_{CC}	V
Device enable voltage (EN1…EN4)	0 to V_{CC}	V
Ambient operating temperature (T_A)	–40 to +85	°C

Table 9. DC and AC characteristics (2.8 V supply)

Symbol	Parameter	Condition(1)	Min	Typ	Max	Unit
f_{MCLK}	Master clock (eg. from VCTCXO)	Sine wave/square wave	10	26	52	MHz
V_{CC}	Supply voltage		2.5	2.8	3.6	V
Vin	Input clock voltage level(2)		0.75	1		Vpp
Vout	Output gain level(3)	C_L = 10 pF	–1.5	–0.5		dB
I_Q	Quiescent current(4)	2 buffers version		1.7	2.6	mA
		3 buffers version		2.2	3.3	
		4 buffers version		2.8	4	

Table 9. DC and AC characteristics (2.8 V supply) (continued)

Symbol	Parameter	Condition(1)	Min	Typ	Max	Unit
I_{ACT}	Active current(5)	1 channel enabled		1.8		mA
		2 channels enabled		2.3		
		3 channels enabled		2.85		
		4 channels enabled		3.4		
I_{SB}	Standby current	All buffers disabled			1	µA
R_{IN}	Input resistance	At DC level		>100		kΩ
C_{IN}	Input capacitance	f = 26 MHz		3	4	pF
$t_{r/f}$	Rise/fall times(6)	Vin = 1Vpp, C_L = 10 pF Square wave input/output		2	5	ns
BW	Signal bandwidth(3)	Vin =1 Vpp, -1dB, C_L = 10 pF Sine wave input/output		52		MHz
V_{ENH}	Enable voltage high(7)	EN1~EN4	1.2			V
V_{ENL}	Enable voltage low(7)	EN1~EN4			0.6	V
P_N	Additive phase noise(3)(8)	at 1 kHz offset		–135		dBc/ Hz
		at 10 kHz offset		–145		
		at 100 kHz offset		–150		
t_{RECB}	Buffer recovery time from off to on	STCD10x0 active		20		µs
t_{RECC}	STCD10x0 active recovery time from standby to active			50		µs
C_L	Capacitive load for each channel			10	20	pF
R_L	Resistive load for each channel		10			kΩ

1. Valid for ambient operating temperature: T_A = –40 °C to 85 °C; V_{CC} = 2.5 V to 3.6 V; typical T_A = 25 °C; Load capacitance = 10 pF (except where noted).
2. Clock input voltage level should not exceed supply rails.
3. Simulated and determined via design and NOT 100% tested.
4. The quiescent current is measured when the enable pins are active, but without input master clock signal (f_{MCLK} = 0 Hz).
5. The active current is dependent on the master clock input Vpp and frequency and the capacitive load condition. The typical test condition is 26 MHz sine wave with 1 Vpp master clock input, C_L = 10 pF.
6. The rise time is measured when clock edge transfers from 10% V_{CC} to 90% V_{CC}. The fall time is measured when clock edge transfers from 90% V_{CC} to 10% V_{CC}.
7. Other test results are under test condition V_{ENH} = 1.8 V and V_{ENL} = 0 V.
8. Guaranteed with the supply noise of 30 µ Vrms from 300 Hz to 50 kHz.

7 Typical operating characteristics

Typical operating characteristics of STCD1040 are V_{CC} = 2.8 V; T_A = 25 °C;
load capacitance = 10 pF, 26 MHz TCXO ENE3127B from NDK (except where noted).

Figure 11. Quiescent current (I_Q) vs. supply voltage (V_{CC}) (STCD1040, 2.8 V version, EN1=EN2=EN3=EN4=1, no master clock input)

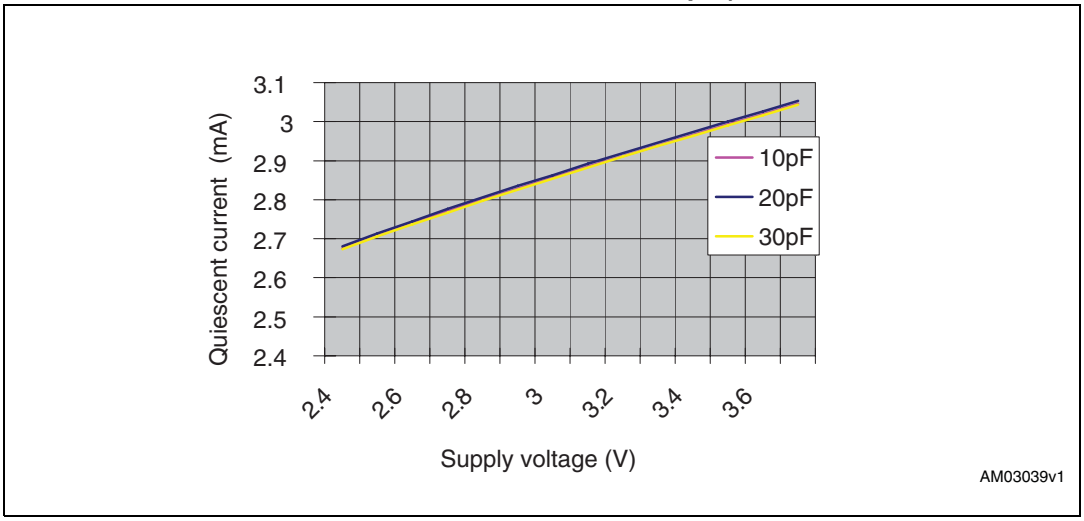


Figure 12. Quiescent current (I_Q) vs. temperature (STCD1040, 2.8 V version, EN1=EN2=EN3=EN4=1, C_L = 30 pF, no master clock input)

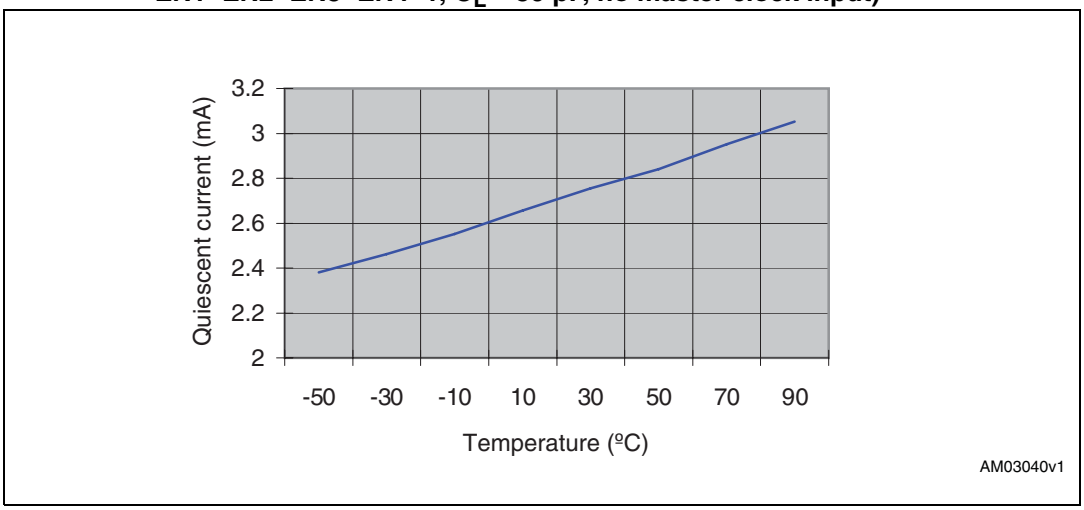


Figure 13. Standby current (I_{SB}) vs. supply voltage (V_{CC}) (STCD1040, 2.8 V version, EN1=EN2=EN3=EN4=0, no master clock input)

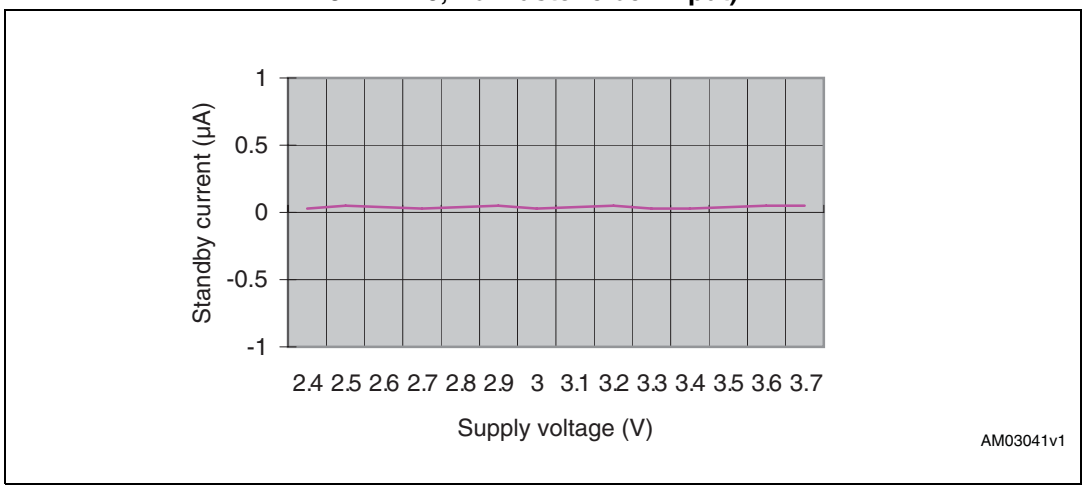


Figure 14. Active current (I_{ACT}) vs. supply voltage (V_{CC}) (STCD1040, 2.8 V version, EN1=EN2=EN3=EN4=1, 26 MHz sine wave master clock input from TCXO)

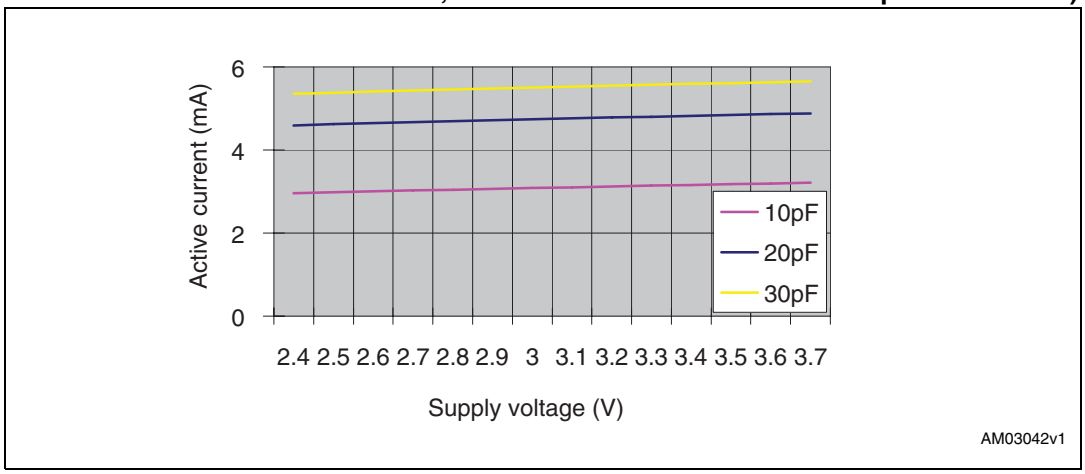


Figure 15. Active current (I_{ACT}) vs. master clock input voltage level (Vpp) (STCD1040, 2.8 V version, EN1=EN2=EN3=EN4=1, 26 MHz sine wave master clock input)

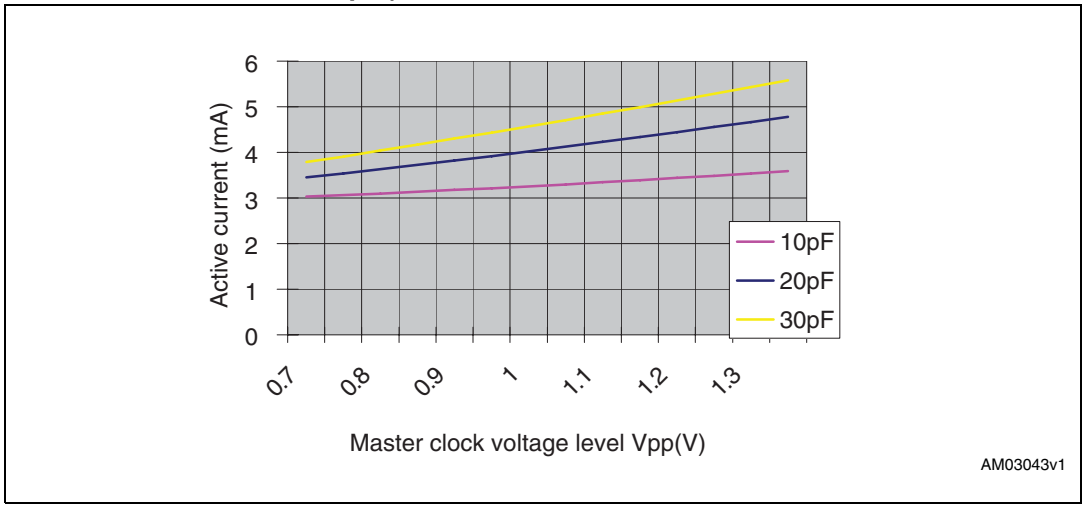


Figure 16. Active current (I_{ACT}) vs. input frequency (STCD1040, 2.8 V version, EN1=EN2=EN3=EN4=1, master clock input Vpp = 1 V)

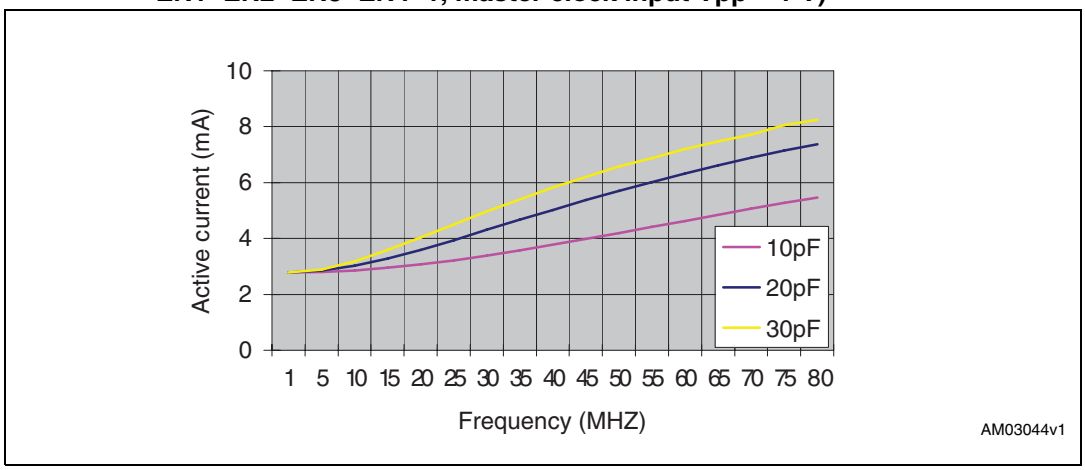


Figure 17. STCD10x0 recovery time from standby to active (STCD1040, 2.8 V version, EN2=EN3=EN4=0, measure CLK1 when EN1 from 0 to 1)

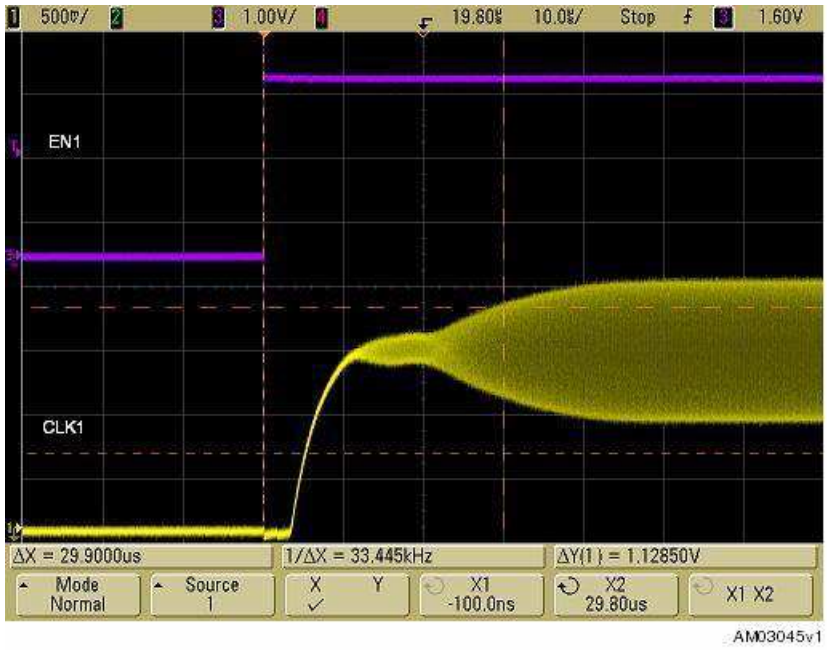


Figure 18. STCD10x0 buffer recovery time from off to on (STCD1040, 2.8 V version, EN2=EN3=EN4=1, measure CLK1 when EN1 from 0 to 1)

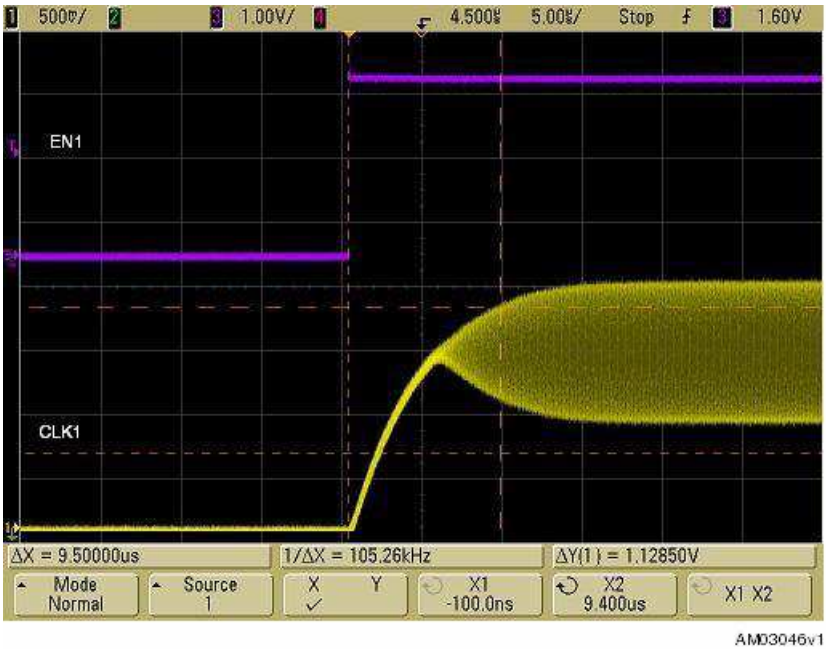


Figure 19. Sine wave input clock vs. output clock (STCD1040, 2.8 V version, 26 MHz sine wave master clock input from TCXO)

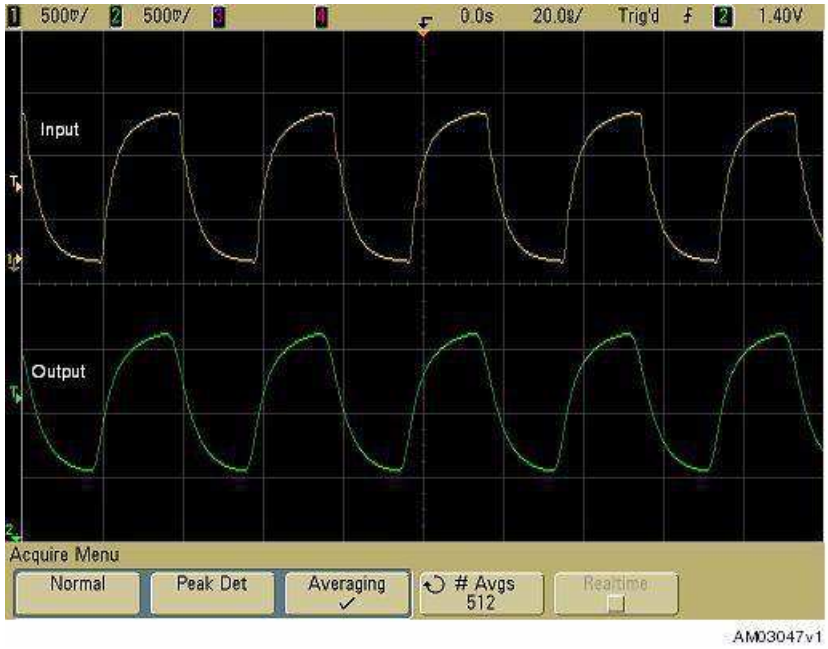


Figure 20. Rise and fall time for square wave output (STCD1040, 2.8 V, 10 MHz square wave master clock input, C_L = 20 pF)

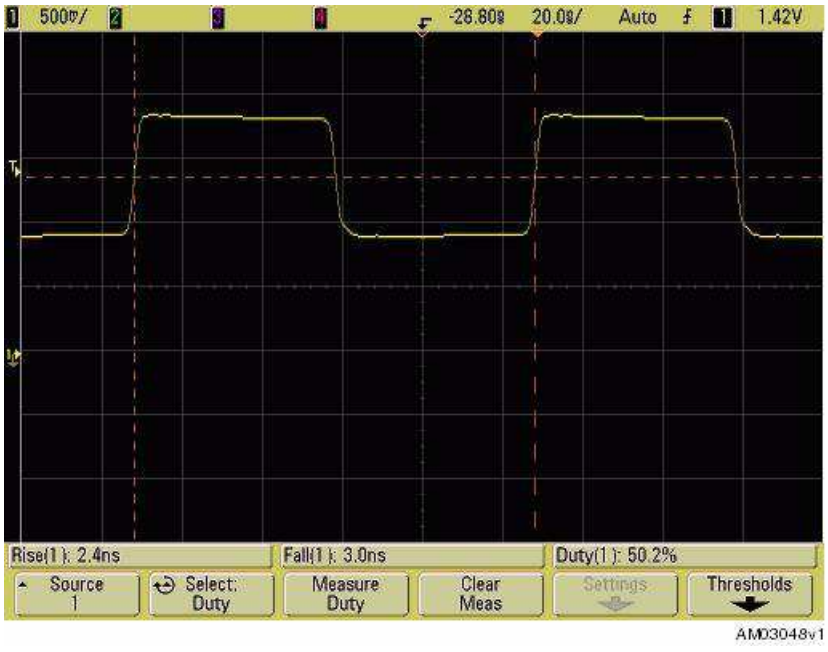


Figure 21. Input clock phase noise (STCD1040, 2.8 V version, 26 MHz master clock input from TCXO)

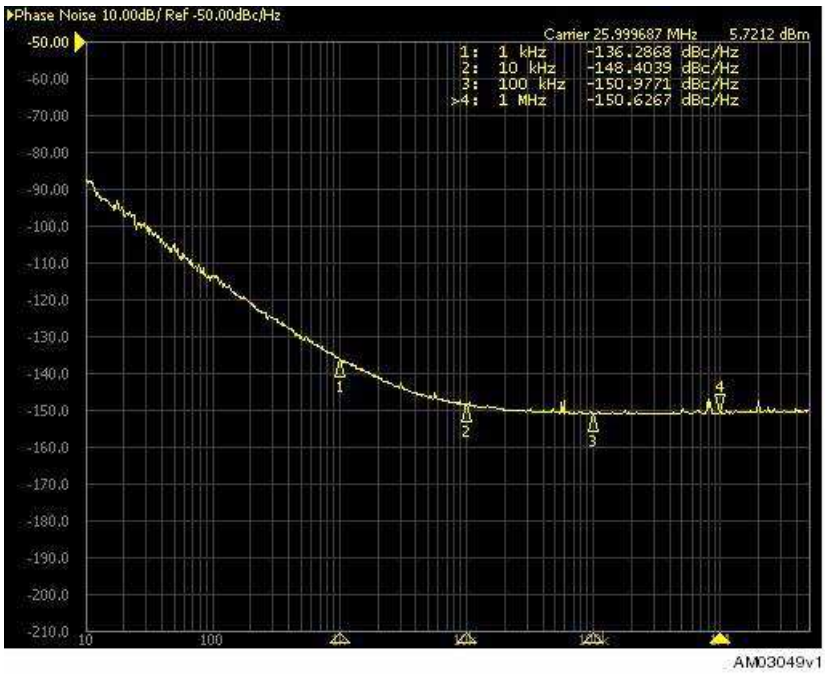


Figure 22. Output clock phase noise (STCD1040, 2.8V version, this phase noise includes the additive phase noise from TCXO and STCD1040)

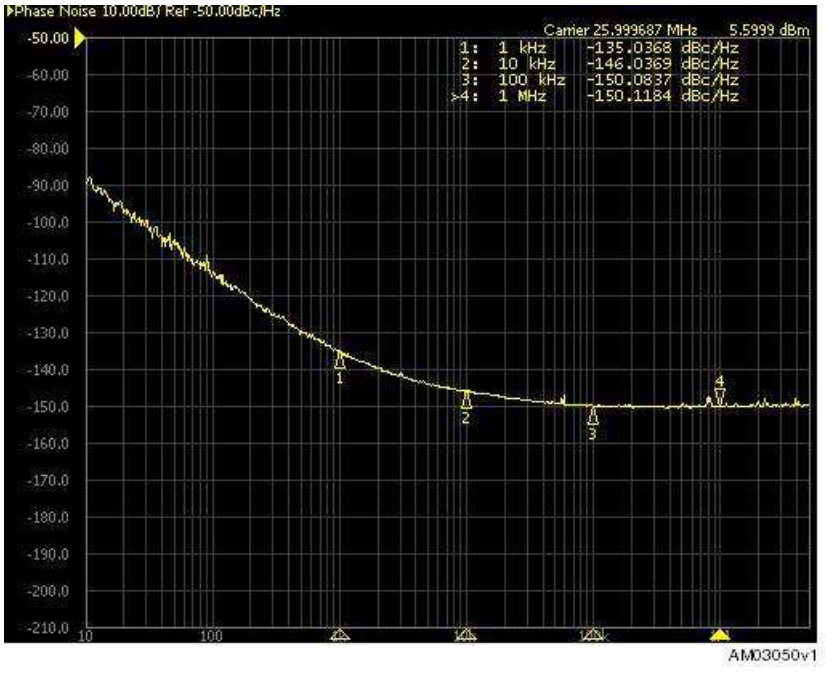


Figure 23. Clock bandwidth (STCD1040, 2.8 V version, C_L = 10 pF)

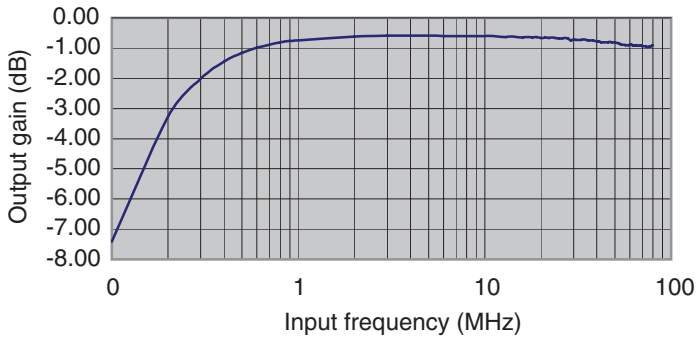


Figure 24. Quiescent current (I_Q) vs. supply voltage (V_{CC}) (STCD1040, 1.8 V version, EN1=EN2=EN3=EN4=1, no master clock input)

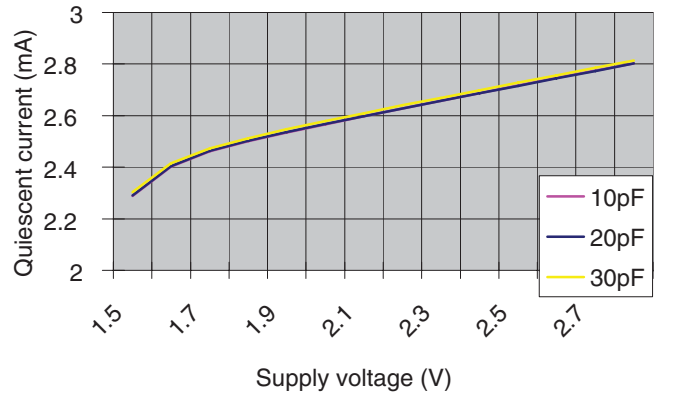


Figure 25. Quiescent current (I_Q) vs. temperature (STCD1040, 1.8 V version, EN1=EN2=EN3=EN4=1, C_L = 30 pF, no master clock input)