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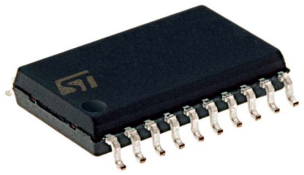
STCMB1

TM PFC with X-cap discharge and LLC resonant combo controller

Datasheet - production data



SO20W

Applications

- Ac-dc adapter, open frame SMPS
- SMPS for LED TV, desktop and all-in-one PC
- Consumer and industrial SMPS compliant with “Energy Using Product” directive (EuP) Lot 6, DOE and European CoC ver. 5, Tier 2
- LED street lighting

Features

- Common features
  - SO20W package
  - 800 V high voltage start-up with integrated input voltage sensing
  - Active input filter capacitor discharge circuitry for reduced standby power compliant with IEC 62368-1 and UL Demko certified
  - Independent debug mode for both converters
- PFC controller features
  - Enhanced constant on-time PFC with input voltage feedforward, THD optimizer
  - Complete set of protections: ac brown-in/out, inrush control, OVP, OCP, inductor saturation, feedback disconnection
- LLC controller features
  - Proprietary timeshift control for improved input ripple rejection and dynamic response
  - Half-bridge operation up to 750 kHz with self-adjusting deadtime
  - Complete set of protections: dc brown-out, two-level OCP, hard switching prevention (HSP) function for anti-capacitive mode protection and safe start-up
  - Synchronous burst mode operation with PFC enhances light-load efficiency

Contents

1 Description

The STCMB1 device embodies a transition mode (TM) PFC, a high voltage double-ended controller for LLC resonant half-bridge, an 800 V-rated high voltage section and the glue logic that supervises the operation of these three blocks.

The PFC section uses a proprietary constant on-time control methodology that does not require a sinusoidal input reference, thereby reducing the system cost and external component count.

It includes also a complete set of protections: a cycle-by-cycle overcurrent (OCP), an output overvoltage (OVP), a feedback failure (FFP, latch-mode), an ac brown-out, boost inductor saturation and inrush current detection both at the start-up and after mains sags or missing cycles.

The half-bridge (HB) section provides two complementary outputs that drive the high-side and low-side MOSFET 180° out-of-phase. The deadtime inserted between the turn-off of an either switch and the turn-on of the other is automatically adjusted to ensure zero voltage switching and higher efficiency from low to full load.

A proprietary control method, timeshift control - TSC, improves dynamic behavior and input ripple rejection resulting in a cleaner output voltage.

At the light-load the IC can be forced to enter a controlled burst mode operation where both the HB and the PFC work intermittently synchronized one to another. This helps to reduce the average switching frequency, thus keeping converter input consumption as low as possible.

At the start-up, in addition to the traditional soft-start based on the frequency-shift, a proprietary hard switching prevention (HSP) function controls the half-bridge to prevent hard switching in the initial cycles. Additionally, the HSP function prevents the converter from working in or too close to the capacitive mode to ensure soft-switching.

The HB is provided with a two-level OCP. The first level is with the frequency shift and delayed shutdown with an automatic restart. A fast shutdown with an automatic restart occurs if this first-level protection cannot limit the primary current. Finally, the device embeds the logic circuitry to coordinate the operation of the PFC, HB and HV start-up generator; in particular: the power-on/off sequencing, X-capacitor discharge, fault handling and synchronous burst mode operation. For the application debug purposes it is possible to externally disable one section at a time and have the other section working standalone.

2 Block diagrams

Figure 1. STCMB1 block diagram

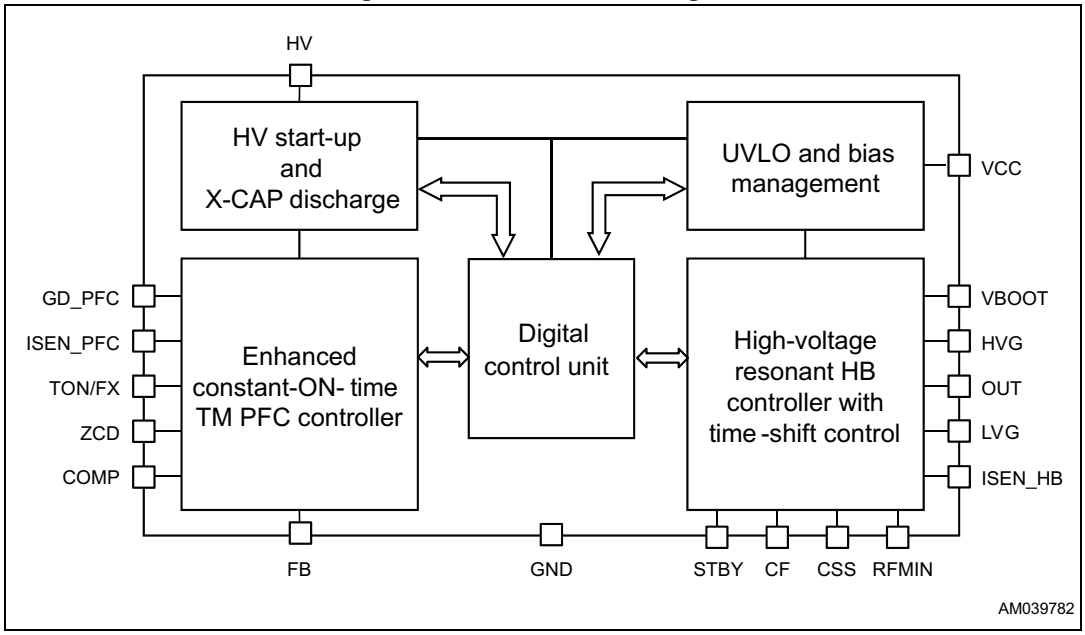
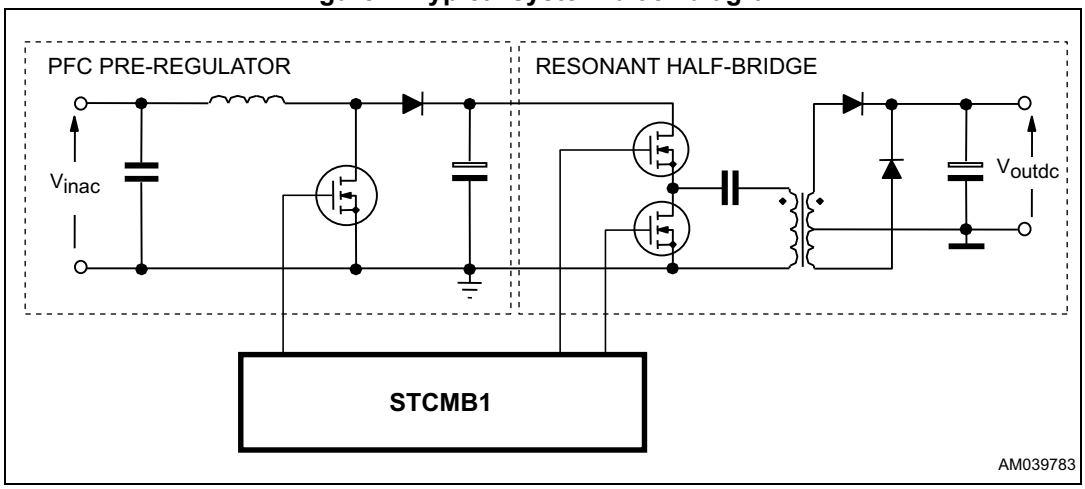


Figure 2. Typical system block diagram



3 Pin connections and description

Figure 3. Pin connections, top view

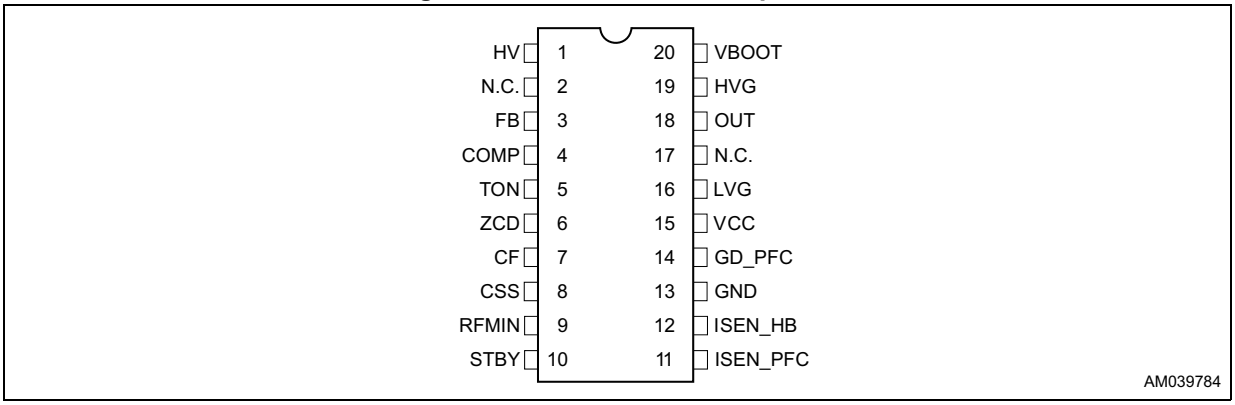


Table 1. Pin description

Pin no.	Name	Function
1	HV	High voltage start-up generator / ac voltage sensing input. The pin, able to withstand 800 V, has to be connected to the ac side of the input bridge via a pair of diodes (1N400x type) to sense the ac input voltage. If the voltage on the pin is higher than 20 V (typical value), an internal pull-up circuit charges the capacitor connected between the VCC pin and GND. Initially the current is low for safety in case of a shorted VCC, and then it goes to the normal level as far as the VCC pin reaches the start-up threshold. To reduce the hold-up requirement on the VCC cap, the generator is turned off when the half-bridge section starts up. In case of a fault that prevents the half-bridge from starting up, the HV generator is shut down after a timeout of 80 ms. The generator is re-enabled when the voltage on the VCC pin falls below the UVLO threshold. In case of a latched shutdown, when the VCC cycles between the start-up threshold and the UVLO threshold, the current is reduced to keep power dissipation low. The same occurs in case of a restart after a fault to create a longer restart delay. The pin is used also to sense the ac voltage, which is used by the input voltage feedforward and the ac brown-out functions. When a brown-out condition is detected any latched protection converging on the FB pin is cleared. An internal logic circuit detects that the unit has been detached from the power line and activates the high voltage start-up generator to discharge the X-capacitors of the EMI filter to a safe level. This allows the unit to meet safety regulations (such as IEC 61010-1 or IEC 62368-1) without using the traditional discharge resistor in parallel to the X-capacitor, thus saving the associated power losses and enabling ultra-low consumption in standby conditions. A series resistor between 3 kΩ and 9 kΩ has to be mandatorily inserted in series to the pin.
2, 17	N.C.	High voltage spacer. These pins are not internally connected to isolate the high voltage sections and ease compliance with safety regulations (creepage distance) on the PCB.

Table 1. Pin description (continued)

Pin no.	Name	Function
3	FB	Being the pin uncommitted, its voltage is proportional to the instantaneous output voltage of the PFC stage. Under steady state conditions the voltage on the pin sits at the internal reference of the error amplifier (2.5 V). If the voltage exceeds the steady state value by 7% (e.g.: due to an output voltage overshoot) switching is stopped until it gets back close to it. If the FB voltage falls below 0.5 V, a failure of the output divider is assumed and both the PFC stage and the half-bridge are latched off. The HV start-up generator is intermittently turned on to keep the device supplied. To restart the device it is necessary to disconnect the unit from the input source. As the input voltage monitor for the half-bridge, the pin handles power-on and power-off sequencing. As the device is turned on, the PFC stage starts first and the half-bridge is kept disabled until the FB voltage exceeds 2.4 V. In case the voltage is already above 2.4 V as the PFC starts, the half-bridge waits 0.2 ms before starting, so to have always consistent power-on sequencing. The half-bridge is again inhibited as the voltage on the pin falls below 1.75 V (dc brown-out).
4	COMP	To avoid an uncontrolled rise of the output voltage at the zero load, when the voltage on the pin falls below 1 V (typical value) the gate driver output will be inhibited (burst mode operation).
5	TON	Maximum on-time of the PFC MOSFET. A resistor and a capacitor in parallel are connected from this pin to ground. When the MOSFET of the PFC stage is ON an internal current generator produces a ramp that, along with the voltage on the COMP pin, determines the turn-off instant of the MOSFET.
6	ZCD	Boost inductor's demagnetization sensing input. A negative-going edge triggers the PFC MOSFET's turn-on. The pin can be connected to an auxiliary winding of the boost inductor through a resistor or to the drain of the MOSFET via an RC series.
7	CF	Timing capacitor for HB oscillator. A capacitor connected from this pin to GND is charged by an internal current generator programmed by the external network connected to the RFMIN pin. In each half cycle the ramp starts as the tank current (sensed through the ISEN_HB pin) and the applied square wave voltage has the same sign (e.g.: ISEN_HB positive during the high-side MOSFET on-time and ISEN_HB negative during low-side MOSFET on-time). The ramp is reset as a fixed peak value is reached. This also causes the HB to be toggled.
8	CSS	HB soft-start. This pin connects an external capacitor to GND and a resistor to the RFMIN pin that set both the initial oscillator frequency and the time constant for the frequency shift that occurs as the chip starts up (soft-start). An internal switch discharges this capacitor every time the chip turns off (VCC < UVLO, FB < 1.75 V, ISEN_HB > 1.5 V) to make sure it will be soft-started next. Additionally the switch is activated when the voltage on the current sense pin (ISEN) exceeds 0.8 V or when the converter is working in the capacitive mode operation. As long as the voltage on the pin is lower than 0.3 V, the burst mode operation and second level OCP protection are inhibited.
9	RFMIN	Timeshift setting. This pin provides an accurate 2 V reference, and a resistor connected from this pin to GND defines a current that is used to set the maximum timeshift. To close the feedback loop that regulates the converter output voltage by modulating the timeshift, the phototransistor of an optocoupler will be connected to this pin through a resistor. The value of this resistor will set the minimum timeshift. An R-C series connected from this pin to GND sets the timeshift at the start-up to prevent an excessive energy inrush (soft-start).

Table 1. Pin description (continued)

Pin no.	Name	Function
10	STBY	Burst mode operation threshold for the HB. The pin senses some voltage related to the feedback control, which is compared to an internal reference (1.25 V). If the voltage on the pin is lower than the reference, the IC stops switching, enters an idle state and its quiescent current is reduced. The chip restarts switching as the voltage exceeds the reference by 40 mV. Soft-start is not invoked. When the HB is stopped the PFC is stopped as well; while the HB is switching the PFC stage is enabled and it switches or not depending on the level of the COMP pin. Tie the pin to RFMIN if the burst mode operation is not used. An RC filter is mandatory, with R > 100 Ω and C > 100 pF. Please note that the time constant of the RC filter enters in the loop transfer function, when the pin is directly fed by the phototransistor of the optocoupler.
11	ISEN_PFC	The inductor current is sensed through a resistor RS on the current return side and the resulting negative voltage is applied to this pin through a limiting resistor. When the power MOSFET is turned on an internal comparator enables the PWM ramp to start only when the voltage on the pin is lower than -25 mV (typical value), e.g.: when the inductor current is slightly positive. If the voltage on the pin goes below -0.5 V the internal overcurrent comparator is triggered and terminates the conduction cycle of the external power MOSFET before the normal PWM circuit does. In this way, the peak inductor current is limited at a maximum of 0.5/RS. A voltage on this pin higher than -25 mV (typical value) enables both power MOSFET's turn-on when a cycle is initiated by the demagnetization sensing circuit and when it is initiated by the internal starter. In this way, the unit stops during the current surges occurring at power up or after a mains dip or a missing cycle and restarts switching only when the surge is over. An RC filter is mandatory at the pin, R > 100 Ω and C > 100 pF. The overall time constant should give a negligible delay with respect to the typical operating frequencies of the PFC. The value of the resistor also defines the effect of the THD optimizer (enhanced COT): THD is usually optimized with a value between 100 Ω and 300 Ω.
12	ISEN_HB	Current sense input for the HB. The pin senses the resonant current through a sense resistor or a capacitive divider for lossless sensing. If the voltage exceeds a 0.8 V threshold the soft-start capacitor connected to the CSS pin is internally discharged: the frequency increases hence limiting the power throughput. Under the output short-circuit, this normally results in a nearly constant peak primary current. This condition is allowed for a maximum time internally set at 40 ms minimum. If the current keeps on building up despite this frequency increase, a second comparator referenced to 1.5 V disables switching immediately. In both cases VCC is recycled before restarting (see the HV pin). As long as the voltage on the CSS pin is lower than 0.3 V, this second comparator is inhibited. The pin is used also by the hard switching prevention (HSP) function. Do not short the pin to ground; this would prevent the device from operating correctly. An RC filter is recommended to reduce the noise level at the pin, with R > 50 Ω and C > 100 pF. The overall time constant should give a negligible delay with respect to the typical operating frequencies of the LLC.
13	GND	Ground. Current return for signal parts of the IC, the PFC gate driver and the low-side gate driver of the half-bridge. Keep the PCB trace that goes from this pin to the sources of the PFC and the low-side MOSFETs separate from the trace that collects the grounding of the bias components.
14	GD_PFC	PFC gate driver output. The totem pole output stage is able to drive power MOSFETs and IGBTs. It is capable of a 0.6 A source current and a 0.8 A sink current (minimum values). The pin is actively pulled to GND during UVLO.

Table 1. Pin description (continued)

Pin no.	Name	Function
15	VCC	Supply voltage of the signal part of the IC. An electrolytic capacitor of at least 22 µF (typ. value) must be connected between the pin and GND. Sometimes a small bypass capacitor (0.1 µF typ.) in parallel to the ELCAP might be useful to get a clean bias voltage for the signal part of the IC.
16	LVG	Low-side gate drive output. The driver is capable of a 0.3 A source and a 0.8 A sink peak current (minimum values) to drive the lower MOSFET of the half-bridge leg. The pin is actively pulled to GND during UVLO.
18	OUT	High-side gate drive floating ground. Current return for the high-side gate drive current. Layout carefully the connection of this pin to avoid too large spikes below ground.
19	HVG	High-side gate drive output. The driver is capable of a 0.3 A source and a 0.8 A sink peak current (minimum values) to drive the upper MOSFET of the half-bridge leg. A resistor internally connected to OUT ensures that the pin is not floating during UVLO.
20	BOOT	High-side gate drive floating supply voltage. The bootstrap capacitor connected between this pin and OUT is fed by an internal synchronous bootstrap diode driven in phase with the low-side gate drive. This patented structure replaces the normally used external diode.

4 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Pin no.	Parameter	Value	Unit
V_{HV}	1	Voltage range (referred to GND)	-1 to 800	V
-	3, 5, 7, 8, 9, 10	Analog inputs and outputs voltage range	-0.3 to 3.6	V
-	4, 6	Analog inputs and outputs voltage range	-0.3 to 5.5	V
I_{ZCD}	6	Zero current detector input max. current	3	mA
I_{RFMIN}	9	Maximum source current	2	mA
V_{ISEN_PFC}	11	Current sensing inputs voltage range	-3 to 3.6	V
V_{ISEN_HB}	12	Current sensing inputs voltage range	-3 to 5.5	V
V_{GD_PFC}, V_{LVG}	14, 16	Ground-referenced gate drivers	-0.3 to V_{VCC}	V
V_{VCC}	15	IC supply voltage	-0.3 to 21	V
V_{OUT}	18	Floating ground voltage	-3 up to a value included in the range V_{BOOT} -21 and V_{BOOT}	V
d_{VOUT} /dt	18	Floating ground max. slew rate	50	V/ns
V_{HVG}	19	High-side (floating) gate driver	V_{OUT} - 0.3 to V_{VBOOT} + 0.3	V
V_{BOOT}	20	Floating supply voltage (referred to GND)	-1 to 620	V
ESD HBM	18,19	According to ANSI/ESDA/JEDEC JS-001-2014	± 900	V
	1, 3 to 16, 20		± 2000	

5 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Max. thermal resistance, junction to ambient	90	°C/W
P_{tot}	Power dissipation at T_{amb} = 70 °C	0.6	W
T_j	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

6 Electrical data

T_j = -40 °C to +125 °C, V_{VCC} = V_{VBOOT} = 15 V[a], C_F = 470 pF; R_{RFMIN} = 22.5 kΩ; C_{HVG} = C_{LVG} = C_{GD_PFC} = 1 nF, C_{TON} = 470 pF unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IC supply voltage						
V_{VCC}	Operating range	After turn-on	10	-	20	V
V_{VCCOn}	Turn-on threshold	(1)Voltage rising	15.5	16.5	17.5	V
V_{VCCOff}	Turn-off threshold	(1)Voltage falling	9	9.5	10	V
Supply current						
I_q	Quiescent current after turn-on	V_{FB} = 1 V	-	1.5	2.2	mA
		V_{FB} = 2.5 V	-	3	4	
		Idle during burst mode T_j = 25 °C	-	0.7	0.94	
		IC latched off	-	-	1.2	
I_{CC}	Operating supply current at f_{sw} = 75 kHz	V_{FB} = 1 V, GD_PFC only	-	2.8	3.6	mA
		V_{FB} = 2.5 V, all drivers	-	4.5	6	
High voltage start-up generator						
V_{HV}	Breakdown voltage	I_{HV} < 100 µA	800	-	-	V
$V_{HVstart}$	Start voltage (rising)	(1)I_{VCC} < 100 µA	10	18	25	V
V_{VCC_SO}	VCC switchover threshold	-	1	1.5	2	V
$I_{HV, ON}$	ON-state charge current	V_{HV} > $V_{HVstart}$, V_{VCC} < V_{VCC_SO}	0.5	1	1.6	mA
		V_{HV} > $V_{HVstart}$, V_{VCC} > V_{VCC_SO}	5	8	11	
		IC latched off or restart after overload timeout	3.5	4.5	5.5	
$I_{HV, OFF}$	Off-state leakage current	V_{HV} = 400 V	-	20	24	µA
T_{TOUT}	Generator shutdown timeout	After V_{VCC} exceeds V_{VCCOn}	64	80	96	ms
IC debug functions						
V_{ZCD_D}	PFC disable threshold	At turn-on, voltage rising	-	2.4	-	V
$V_{ISEN\_HB\_D}$	HB disable threshold	At turn-on, voltage rising	-	2.4	-	V
X-capacitor discharge function						
V_{HVmin}	Peak residual voltage	$I_{HV, DIS}$ > 4.2 mA	-	-	45	V
$I_{HV, DIS}$	Discharge current	V_{HV} > 45 V	4.2	-	-	mA

a. Adjust V_{VCC} above V_{VCCOn} before setting at 15 V.

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
PFC - ac brown-out protection						
V_{HVpk_BO}	Brown-out threshold	(1)Peak voltage falling LLC in continuous switching, no burst mode. RHV series = 5.6 KΩ	92	98	104	V
V_{HVpk_BI}	Brown-in threshold	(1)Peak voltage rising LLC in continuous switching, no burst mode. RHV series = 5.6 KΩ	106	113	120	V
T_{DB}	Brown-out debounce time	-	32	40	48	ms
PFC - zero current detector						
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 2.5 mA	2.8	3.3	-	V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = -2.5 mA	-0.3	-	0	V
V_{ZCDA}	Arming voltage	(1)Positive-going edge	-	0.5	-	V
V_{ZCDT}	Triggering voltage	(1)Negative-going edge	-	0.25	-	V
I_{ZCDb}	Input bias current	V_{ZCD} = 1 to 2.2 V	-	-	5	µA
PFC - maximum on-time						
I_{TON}	Charge current	V_{TON} = 3 V, V_{HV_pk} = 160 V dc	180	200	220	µA
		V_{TON} = 3 V, V_{HV_pk} = 320 V dc	640	800	960	
V_{TON}	Linear operating range	-	0	-	3	V
V_{TON}	On-time reference level	GD_PFC goes low V_{COMP} = 3 V	-	2	-	V
R_{DSC}	Discharge resistance	-	-	60	200	Ω
PFC - transconductance error amplifier						
V_{ref}	Internal voltage reference	T_j = 25 °C	2.475	2.5	2.525	V
		(1)10 V < V_{VCC} < 21 V	2.44	-	2.58	
I_{FB}	Input bias current	V_{FB} = 0 to 3 V	-1	-0.2	1	µA
$V_{COMPSAT}$	Upper clamp voltage	I_{SOURCE} = 20 µA	4.0	4.3	-	V
		I_{SOURCE} = 20 µA, T_j > °0	4.2	4.5	-	
I_{COMP}	Max. sink/source current	V_{COMP} = 3 V, V_{FB} = 2.3 V	150	200	-	µA
g_m	Transconductance	V_{FB} = V_{ref}	160	200	240	µS
Ro	Output impedance	-	2	-	-	MΩ
PFC - dynamic and static OVP protections						
V_{FB_S}	D_OVP threshold	T_j = 25 °C	2.595	2.675	2.755	V
		(1)10 V < V_{VCC} < 21 V	2.568	-	2.782	
V_{FB_R}	Restart voltage after D_OVP	(1)	2.47	2.55	2.63	V
T_{DB}	D_OVP debounce time	-	40	50	65	µs
V_{COMP_S}	S_OVP threshold	(1)Voltage falling	0.9	1	1.1	V
V_{COMP_R}	Restart voltage after S_OVP	(1)Voltage rising	0.92	1.02	1.15	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
PFC - feedback failure protection (FFP)						
V_{FB_D}	Disable threshold	(1)Voltage falling	0.42	0.46	0.5	V
T_{DB}	FFP debounce time	-	40	50	65	µs
PFC - current sensing comparators						
I_{ISEN_PFC}	Input bias current	VISEN_PFC = -0.5 V	-	-	4.8	µA
V_{ISEN_PFC}	OCP threshold	(1)VCOMP = upper clamp	-0.46	-0.5	-0.54	V
$td_{(H-L)}$	Delay to output	-	-	220	280	ns
$V_{ISEN\_PFC\_Z}$	ZCD anticipation level and THD optimizer threshold	-	-	-25	-	mV
PFC - internal start-up timer						
t_{START_DEL}	Start-up delay	After $V_{ISEN\_PFC} > V_{ISEN\_PFC\_Z}$	8	10	13	µs
PFC - GATE DRIVER						
V_{OL}	Output low voltage	I_{sink} = 100 mA	-	0.4	0.7	V
V_{OH}	Output high voltage	I_{source} = 5 mA	14.7	14.9	-	V
t_f	Voltage fall time	From 15 to 1.5 V	-	30	70	ns
t_r	Voltage rise time	From 0 to 10 V	-	60	110	ns
	UVLO saturation	V_{VCC} = 0 to V_{VCCon}, I_{sink} = 1 mA	-	-	1.1	V
HB - high-side floating gate drive supply						
$R_{DS(on)}$	Synchronous bootstrap diode on-resistance	V_{LVG} = HIGH	-	230	-	Ω
HB - input voltage sensing (dc brown-out)						
V_{FB_E}	Enable voltage	(1)Voltage rising	2.34	2.4	2.49	V
V_{FB_D}	Disable voltage	(1)Voltage falling	1.7	1.75	1.8	V
HB - oscillator						
V_{CFp}	Ramp peak	(1)V_{STBY} > 1.34 V	1.44	1.5	1.56	V
		(1)V_{STBY} < 1.26 V	1.775	1.85	1.925	
V_{CFv}	Ramp valley	-	0	-	20	mV
V_{RFMIN}	Voltage reference	(1)	1.93	2	2.08	V
		(1)I_{RFMIN} = -2 mA	1.93	2	2.08	
D	Output duty cycle (HVG and LVG)(2)	V_{STBY} = 2 V R_{RFMIN} = 5.15 kΩ	49	50	51	%
T_{SH}	Time-shift	R_{RFMIN} = 22.5 kΩ	8.5	9	9.5	µs
		R_{RFMIN} = 5.15 kΩ	2.1	2.25	2.4	
f_{HB}	Max. operating frequency	-	500	-	-	kHz
K_M	Mirroring ratio I_{CF} / I_{RFMIN}	-	0.97	1	1.03	-
R_{RFMIN}	Timing resistor range	-	1	-	100	kΩ

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
HB - adaptive deadtime function						
T_{D_max}	Maximum deadtime	-	0.7	-	-	µs
T_{D_min}	Minimum deadtime	-	-	-	270	µs
HB - zero-current comparator						
V_{ISEN_Z}	Threshold voltage	Negative-going edge	-	-35	-	mV
		Positive-going edge	-	35	-	
HB - overcurrent comparator and overload delays						
I_{ISEN_HB}	Input bias current	V_{ISEN_HB} = 0 to 1.4 V	-1	-	1	nA
$V_{ISEN\_HB\_x}$	Frequency shift threshold	(1)Voltage rising	0.76	0.80	0.84	V
$V_{ISEN\_HB\_dis}$	Immediate stop threshold	(1)Voltage rising	1.42	1.5	1.58	V
HB - soft-start function						
I_{leak}	Open state current	V_{CSS} = 2 V	-	-	0.5	µA
R	Discharge resistance	-	-	120	220	Ω
T_{DISCH}	Css discharge duration	$V_{ISEN\_HB} > V_{ISEN\_HBx}$	-	6	-	µs
$V_{thHSP-SS}$	SS discharge enable (HSP)	(1)Voltage rising	1.77	1.85	1.94	V
HB - standby function						
I_{STBY}	Input bias current	V_{STBY} = 1.3 V	-1	-	1	µA
V_H	V_{CFp} change threshold	(1)Voltage falling	1.26	1.3	1.34	V
$V_{H,Hys}$	V_H hysteresis	Voltage rising	30	40	50	mV
V_L	Disable threshold	(1)Voltage falling	1.21	1.25	1.29	V
$V_{L,Hys}$	V_L hysteresis	Voltage rising	30	45	60	mV
Low-side gate driver (voltages referred to GND)						
V_{OL}	Output low voltage	I_{sink} = 50 mA	-	0.5	0.9	V
V_{OH}	Output high voltage	I_{source} = 5 mA	14.7	14.9	-	V
t_f	Voltage fall time	From 15 to 1.5 V	-	30	70	ns
t_r	Voltage rise time	From 0 to 10 V	-	60	110	ns
	UVLO saturation	V_{VCC} = 0 to V_{VCCon}, I_{sink} = 1 mA	-	0.9	1.1	V
High-side gate driver (voltages referred to OUT)						
V_{OL}	Output low voltage	I_{sink} = 50 mA	-	0.5	0.9	V
V_{OH}	Output high voltage	V_{BOOT} = V_{CC} V, I_{source} = 5 mA	14.7	14.9	-	V
t_f	Voltage fall time	From 15 to 1.5 V	-	30	70	ns
t_r	Voltage rise time	From 0 to 10 V	-	60	110	ns
-	HVG-OUT pull-down	-	21	27	36	kΩ

1. Parameters tracking each other.
2. $D_{HVG} + D_{LVG}$ = 100%.

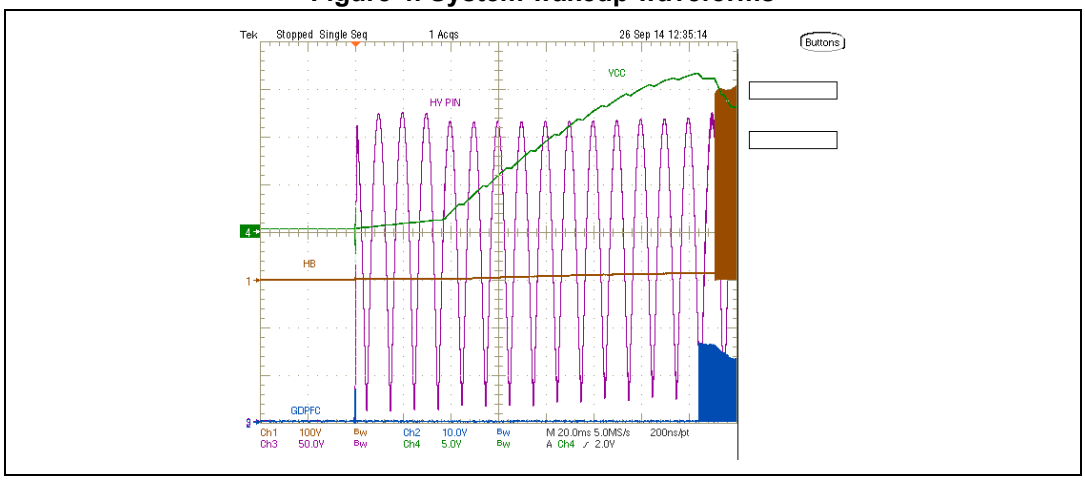
7 Application information

7.1 HV start-up

The STCMB1 is equipped with internal HV start-up circuitry dedicated to supply the IC during the initial start-up phase, before the self-supply winding is operating. An external electrolytic capacitor connected to the VCC pin is charged by the HV start-up circuitry, connected to the HV pin.

As soon as the voltage on the HV pin is higher than $V_{HVstart}$ (18 V typ.), the HV start-up system turns on and the external V_{CC} capacitor is charged up to the turn-on threshold (V_{CCOn}, 16.5 V typ.), then to guarantee a reliable start-up of the STCMB1, the HV start-up system is turned off only after the half-bridge section starts up. In case of a fault that prevents the half-bridge section from starting up, the HV start-up system is automatically shut down after a timeout T_{TOUT} = 80 ms.

Figure 4. System wakeup waveforms



If for any reason the self-supply circuitry cannot power the STCMB1 the HV start-up will be reactivated once the V_{CC} reaches the turn-off threshold ($V_{VCCOff,}$ 9.5 V typ.).

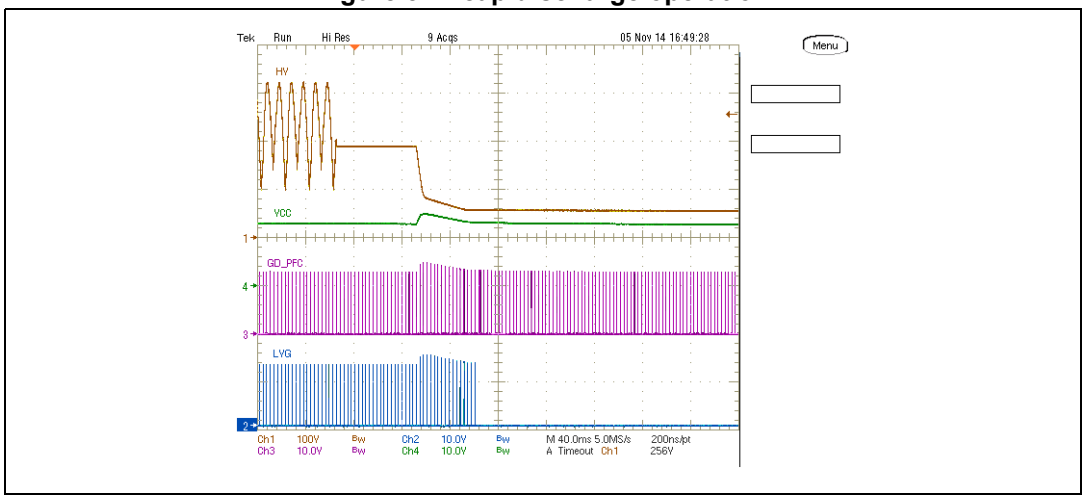
The HV start-up system performs an R-C charge of the VCC pin. A double time constant depending on the voltage value on the VCC pin is implemented to prevent damaging in case of shorts to GND of the V_{CC} circuitry.

The HV startup generator is activated also after detection of the PFC feedback failure, ac brown-out or X-cap discharge condition. Different values of the charging current (IHV,ON) are supplied to the VCC pin according to the state, see *Table 4: Electrical characteristics on page 11*.

7.2 X-cap discharge

The compliance of consumer equipment with the safety regulation such as IEC 61010-1, IEC 62368-1, and others, requires that, when the converter mains connector is removed from the plug, the EMI filter capacitors connected across the line between the phase and the neutral wires (the so called X-caps) have to be discharged bringing their voltage at a safe level to avoid the user any risk of the electrical shock due to the energy stored in the capacitors. This requirement is mandatory in case the total capacitance before the input bridge exceeds 100 nF.

Figure 5. X-cap discharge operation



Typically this function is performed by means of a resistor in parallel but this method cannot be applied in case the converter requires very low power consumption during the light-load or no load operation, because the losses of the X-cap discharging resistor would be too high.

To overcome this issue, enabling the user to design a high performance power supply the STCMB1 device does this operation by means of the HV start-up system, allowing the removal of the traditional X-cap discharge resistor. The STCMB1 internal circuits detect the ac mains plug disconnection by sensing the voltage on the HV pin. After a detection time of 64 ms typical from the mains disconnection, the X-cap discharge operation is triggered and the HV start-up system is turned on: a discharge current (4.2 mA minimum) is drawn from the HV pin ensuring the X-cap discharge until the voltage on the HV pin falls below a safe level (45 V maximum), within the regulation maximum discharging time. The current from the HV pin will flow out from the VCC pin, to keep the IC correctly supplied until the end of the discharge. An internal 15 V clamp is activated to limit the voltage on the VCC pin by sinking the discharge current in excess of the IC consumption.

None additional component is needed by this function, totally embedded in the STCMB1.

7.3 Ac brown-out protection

The STCMB1 device is equipped with brown-out protection to prevent the operation at too low ac input voltage (typically when it falls below 70 V ac). When the brown-out protection is activated, the PFC and HB sections are both turned off, the V_{CC} start falling because no more sustained by the on-board self-supply. When V_{CC} reaches the turn-off threshold (V_{VCCoff}), the HV start-up is turned on and VCC is charged up to VCCon. The HV start-up is then turned off and VCC falls again toward VCCoff, since the switching activity is forbidden by the brown-out protection. The charge and discharge of VCC goes on as long as the abnormal ac mains condition lasts. The brown-out protection is deasserted when the ac voltage goes above the brown-in threshold (typically 80 V ac).

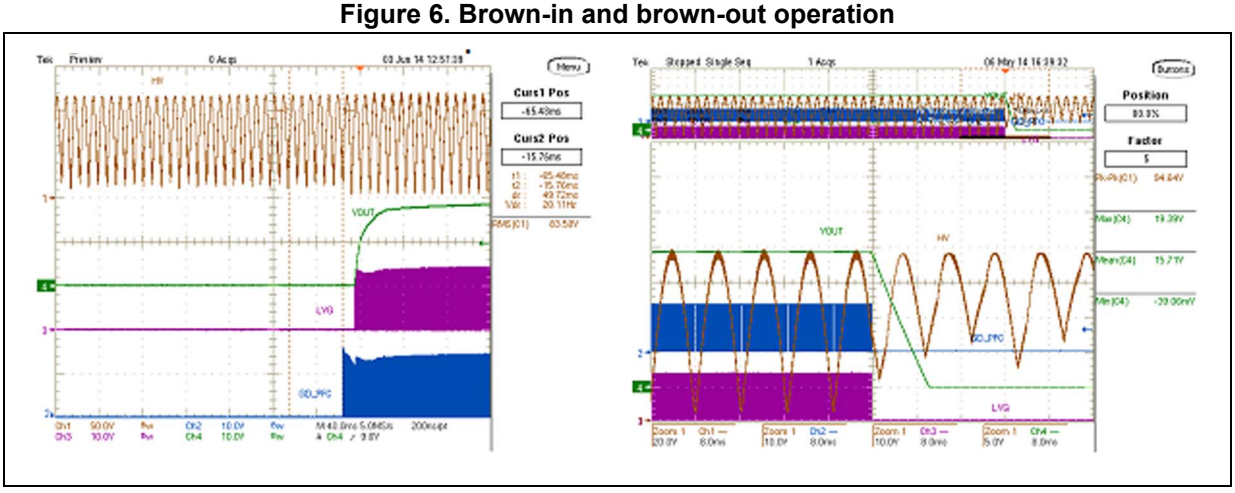
In order to avoid unexpected intervention of AC brown-out protection in case of missing cycles or short dips of the ac mains, a debounce time, T_{DB}, has been introduced: in practice, an AC brown-out condition has to last a time equal to T_{DB} (32 ms, typ.) to stop the converter operation.

To allow correct behavior of the brown-in and brown-out protections, accordingly to the threshold values given in *Table 4 on page 11*, a resistor with value between 3 kΩ and 9 kΩ, in series with the HV pin is mandatory.

The brown-in threshold has to be intended as the voltage at the HV pin right before the adapter turn-on (first GDPFC pulse, in general), when the mains voltage is slowly increased. In detail, before the brown-in, VCC is charged by the HV start-up generator and naturally discharged. During the charge phase, the voltage at the HV pin is about the actual mains voltage minus the drop on the series resistor. When VCC = VCCon, the HV start-up generator is turned off, the voltage drop is reduced to zero and the voltage at the HV pin becomes equal to the actual mains voltage. So, the converter turn-on by brown-in will occur when the mains voltage is above the threshold and the charge phase of VCC is finished.

Conversely, because of the debounce time, the brown-out threshold has to be intended as the last peak voltage at the HV pin at about one debounce time before the adapter turns off (PFC and LLC simultaneously turn off, in general), when the mains voltage is slowly decreased. Note that before the brown-out, the converter is working, so VCC is generated on the board and the HV start-up generator is off; consequently, the voltage at the HV pin is about the actual mains voltage. When the brown-out is triggered, the converter is turned off and the VCC is naturally discharged up to VCCoff when the HV start-up generator is turned on and the charge / discharge operation of VCC starts to maintain the protected condition.

Figure 6. Brown-in and brown-out operation



7.4 VCC pin

This pin is the supply voltage of the IC. An electrolytic capacitor of at least 22 µF (typ. value) must be connected between the pin and GND in order to sustain the voltage during the start-up phase and supply the IC, before the self-supply circuitry from the half-bridge transformer deliver enough voltage. Place also a ceramic capacitor (0.1 µF typ.) in parallel to the electrolytic capacitor to bypass the high frequency noise to GND and supply the STCMB1 device with a proper clean voltage.

The V_{CC} voltage is used also to supply the MOSFET gate drivers, not having a dedicated clamping, supplying the STCMB1 from the auxiliary (self-supply) winding from the resonant transformer may need a small BJT voltage regulator to keep the supply voltage regulated and avoid the aging of the gate oxide due to an excessive V_{CC}, or limit transients that could damage the IC as in case of dead shorts.

A typical V_{CC} operating voltage is 12 - 13 V.

7.5 PFC section

The STCMB1 device implements a transition mode (TM) PFC section that uses a proprietary “Constant On-Time” (COT) control methodology termed “Enhanced Constant On-Time” (ECOT). Like the COT, this control mode does not require a sinusoidal input reference, thereby reducing the system cost and external component count, while providing a distortion of the input current at the same level as current mode control.

It includes also a complete set of protections: the cycle-by-cycle overcurrent (OCP), output overvoltage (OVP), feedback failure (FFP), boost inductor saturation and inrush current detection both at the start-up and after mains sags or missing cycles.

The output voltage (Vout) is controlled by mean of a transconductance error amplifier and an accurate internal voltage reference; “Zero Current Detection” (ZCD) by sensing the voltage on the auxiliary winding on the PFC inductor enables the TM operation.

The current sense on the return path allows continuous monitoring of the inductor current. THD optimization is implemented too.

A “two-level” line voltage feedforward function helps to reduce the changes in the system gain due to changes in input voltage.

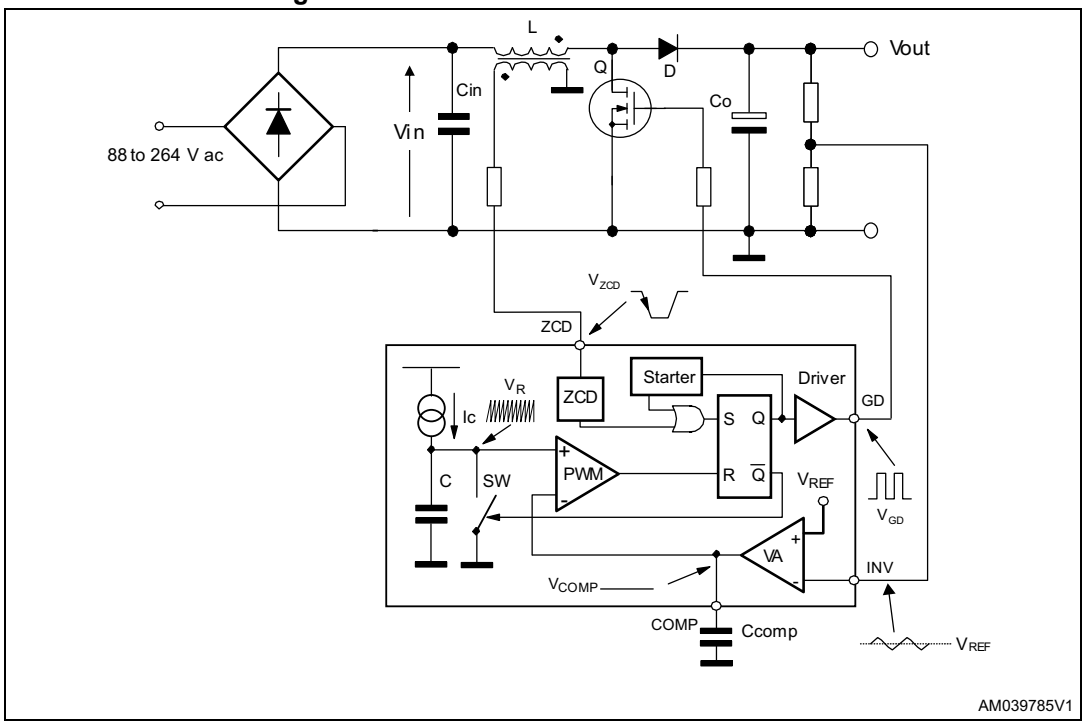
7.6 PFC: enhanced constant on-time control with THD optimizer

TM-operated PFCs are characterized by good efficiency even if the large input current ripple requires bigger EMI filters.

The COT is a common control technique where the turn-on of the power transistor in each cycle is commanded when the current through the boost inductor falls to zero and the turn-off is commanded when the duration of the on-time has reached the value programmed by the control loop. It is well-known that if this on-time is constant or even slowly varying during each line cycle, the converter draws an ideally sinusoidal current from the line.

The combination of the TM operation and COT control is a very popular solution used in several PFC controllers for output power up to 300 W. The block diagram and key waveforms of the traditional approach are shown in *Figure 7* and *Figure 8* respectively.

Figure 7. Conventional COT controlled PFC



Since the slope of the inductor current during the on-time is proportional to the input voltage, there is a perfect linear relation between the instantaneous AC voltage and the current drawn by the circuit, which would ideally provide a perfect unity power factor and no distortion when the on-time is kept constant along a line cycle.

Unfortunately, parasitic elements (essentially, the parasitic capacitance of the drain node, C_{drain}) cause a negative offset in the inductor current shape as can be seen in *Figure 8*. In particular, the negative peak current I_{Lvy} can be calculated as follows:

Equation 1

$$I_{Lvy} = -\left(V_{out} - V_{in\_pk}\, sin\,\theta\right)\sqrt{\frac{C_{drain}}{L}}$$

Approximating the inductor current with a triangular waveshape, the commanded peak current is:

Equation 2

$$I_{Lpk} = I_{Lvy} + \frac{V_{in\_pk}\, sin\,\theta}{L} T_{ON}$$

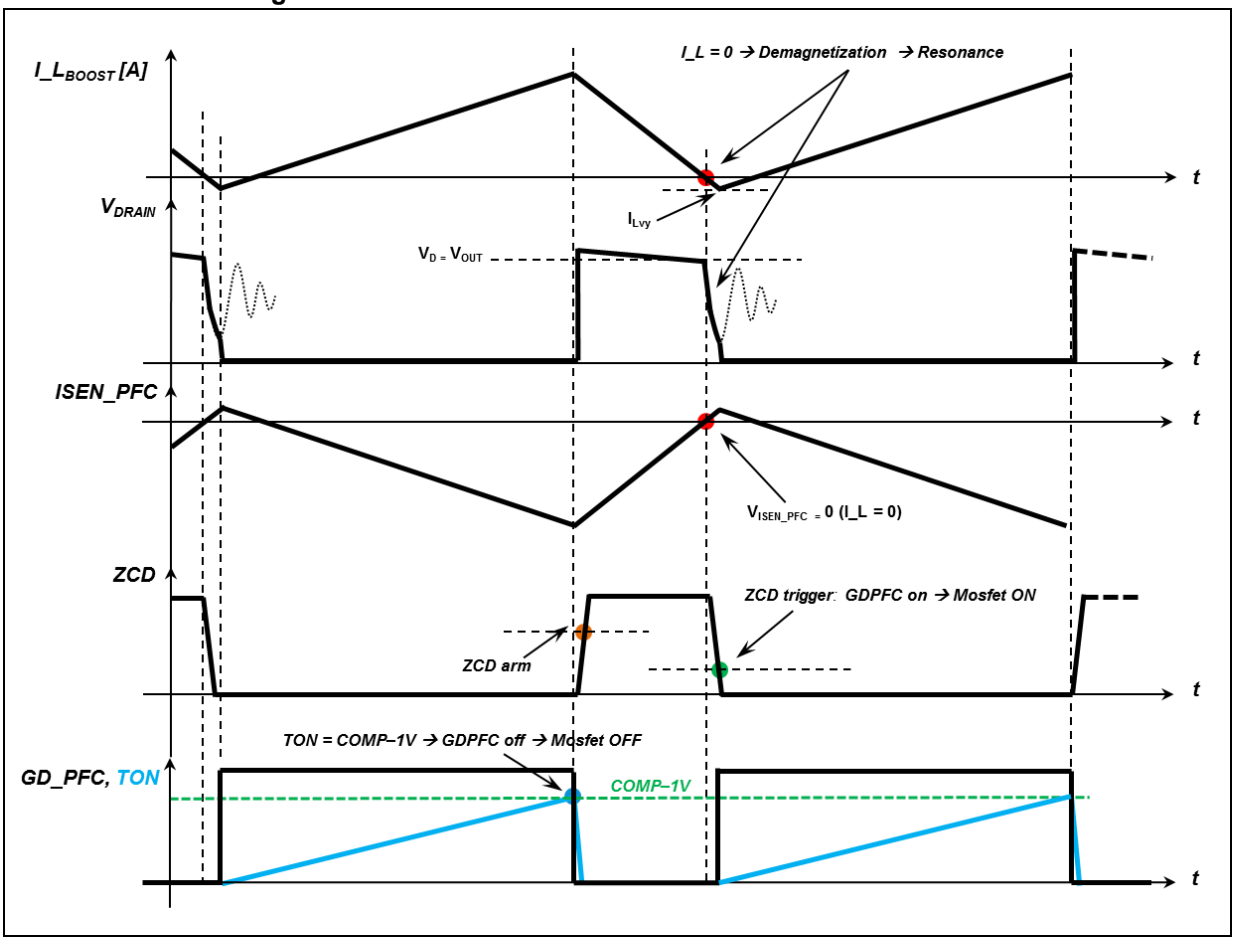
and its average value in a switching cycle is:

Equation 3

$$\left\langle I_L \right\rangle = \frac{1}{2}\left(I_{Lvy} + I_{Lpk}\right) = \frac{V_{in\_pk}\, sin\,\theta}{2\,L} T_{ON} + V_{in\_pk}\, sin\,\theta \sqrt{\frac{C_{drain}}{L}} - V_{out}\sqrt{\frac{C_{drain}}{L}} \quad (x)$$

The last term *"(x)"* in *Equation 3* is non-sinusoidal (constant) and causes distortion in the input current.

Figure 8. Conventional COT controlled TM PFC waveforms



The enhanced constant on-time (ECOT) control integrated in the STCMB1 is a proprietary solution that outperforms the typical THD performance of the conventional COT control. The idea is to cancel out the constant term "(x)" in *Equation 3* with a corresponding positive term. This can be done by delaying the instant start of the timer that sets the on-time until the inductor current reaches a preset value I_{Lth}. In this way it is no longer the ON-time T_{ON} of the power switch that is controlled (and kept constant) but the time T_{ON_C} defined as:

Equation 4

$$I_{Lpk} = I_{Lth} + \frac{V_{in\_pk}\, sin\,\theta}{L} T_{ON\_C} \quad \text{(y)}$$

Of course, the on-time T_{ON} will no longer be constant as in the conventional COT:

Equation 5

$$T_{ON} = T_{ON\_C} + \frac{I_{Lth} - I_{Lvy}}{V_{in\_pk}\, sin\,\theta} L$$

It is possible to prove that, when choosing:

Equation 6

$$I_{Lth} = V_{out}\sqrt{\frac{C_{drain}}{L}}$$

the average value of the inductor current in a switching cycle will be:

Equation 7

$$\langle I_L \rangle = \frac{1}{2}\left(I_{Lvy} + I_{Lpk}\right) = \frac{1}{2}\left(\frac{1}{L}T_{ON\_C} + \sqrt{\frac{C_{drain}}{L}}\right)V_{in\_pk}\,sin\,\theta \quad (z)$$

The block diagram and the relevant waveforms of the ECOT-controlled TM PFC are shown in *Figure 9* and *Figure 10*.

On the one hand, a negative threshold is placed on the current sensing pin ISEN_PFC ($V_{ISEN\_PFC\_Z}$ = -25 mV, typ.): the on-time generator (ramp at pin TON) starts as the (negative) voltage on the pin ISEN_PFC goes below $V_{ISEN\_PFC\_Z}$. This is equivalent to having $I_{Lth} = V_{ISEN\_PFC\_Z}/Rs$, where Rs is the current sensing resistor.

On the other hand, when the threshold $V_{ISEN\_PFC\_Z}$ is crossed by the rising signal on the pin ISEN_PFC at the end of the off-time, an internal generator (Ios = 50 µA typ.) is turned on, which sources the current out of the pin ISEN_PFC. This becomes a positive offset voltage on the pin itself, because of the external series resistor Ros (part of the RC filter of the pin). In this way, the crossing of the threshold $V_{ISEN\_PFC\_Z}$ by the negative-going signal can be further delayed and the equivalent current threshold I_{Lth} set at:

Equation 8

$$I_{Lth} = \frac{\left|V_{ISEN\_PFC\_Z}\right| + I_{OS}\,R_{OS}}{Rs}$$

The value of the series resistor Ros can be adjusted to find the optimum I_{Lth}. As a starting point, one can select Ros based on the theoretical compensation condition:

Equation 9

$$R_{OS} = \frac{Rs\,V_{out}\sqrt{\frac{C_{drain}}{L}} - \left|V_{ISEN\_PFC\_Z}\right|}{I_{OS}}$$

Note in *Figure 10* the effect of this offset in the region $V_{ISEN\_PFC} > V_{ISENPFC\_Z}$ (green portion of the inductor current waveform), compared to the unaffected waveform that would occur with Ros = 0 (black portion of the same waveform in the previous cycle).

Figure 9. Enhanced COT controlled TM PFC block diagram

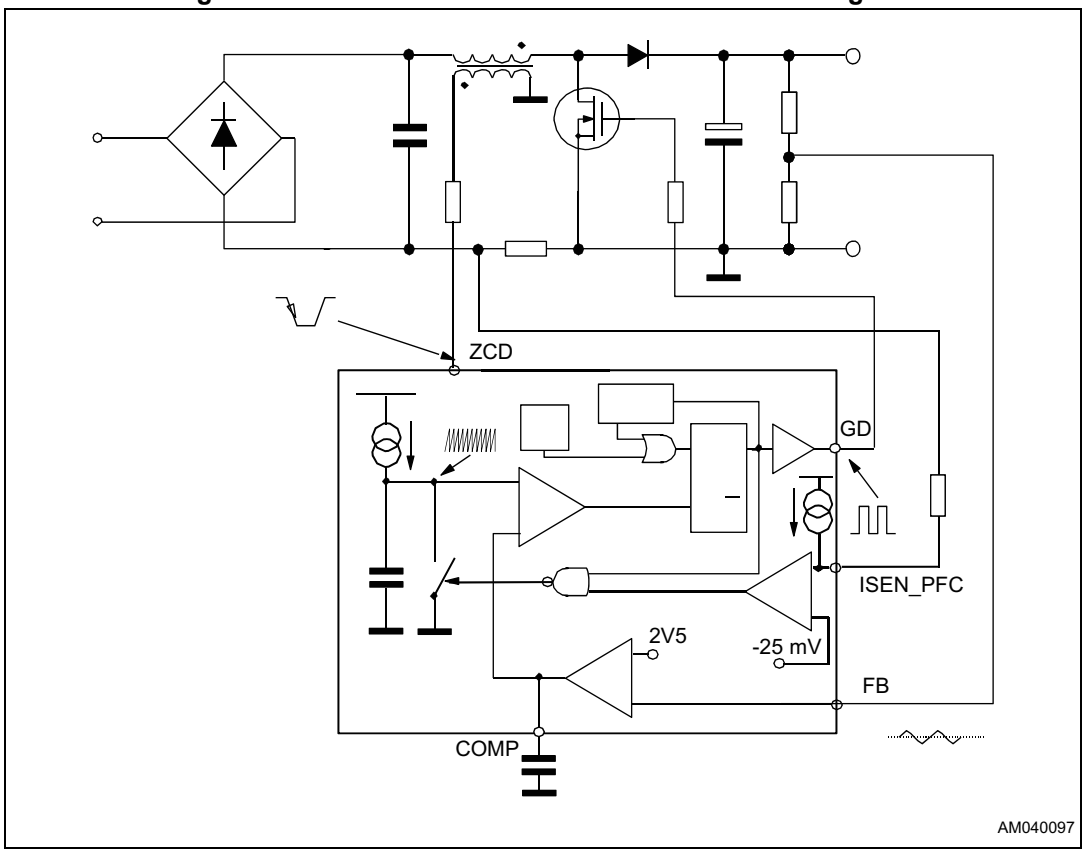
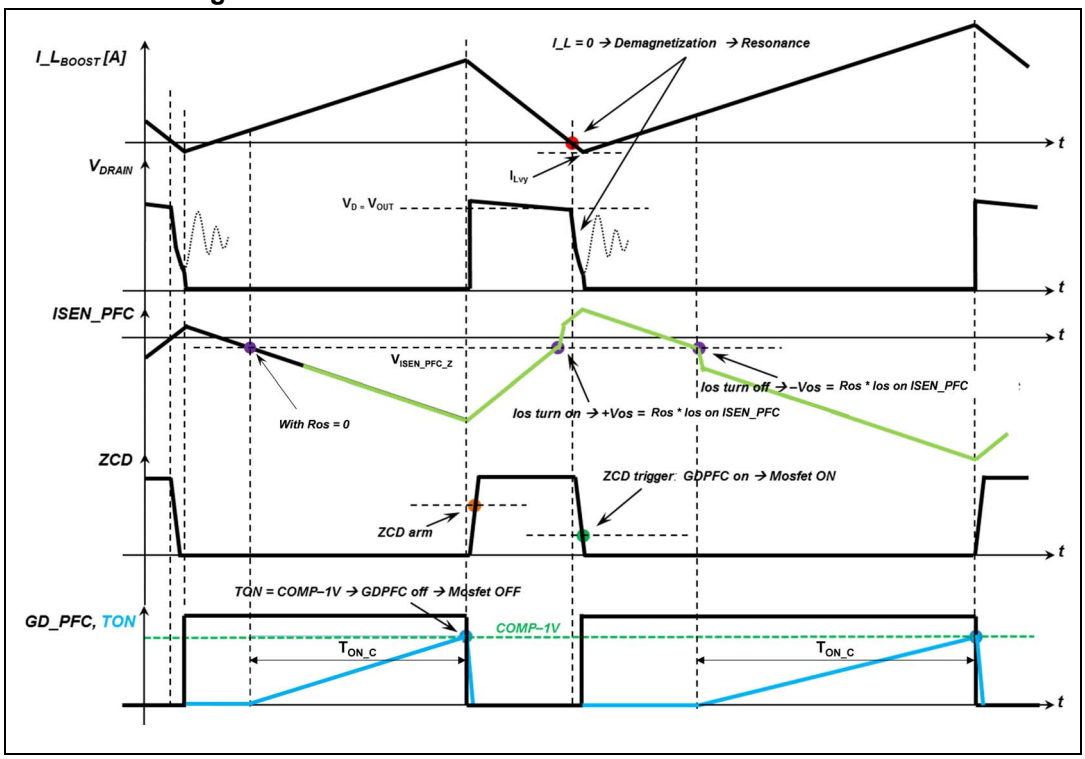


Figure 10. Enhanced COT controlled TM PFC waveforms



7.7 PFC: error amplifier, regulation loop and V_{FF}

The STCMB1 regulation loop keeps the output voltage regulated by means of a transconductance amplifier having an internal 2.5 V reference and a typical gain bandwidth product of 1 MHz. Its inverting input (FB, pin #3) has to be connected to the PFC bulk capacitor via a resistor divider. Since the voltage on this pin is proportional to the PFC output voltage, some other monitoring circuitries are connected to this pin. Because of its high impedance, the FB pin has to be filtered locally by a ceramic capacitor to get a clean and stable voltage. Typical filtering capacitor values are in the range from some nF up to few ten nF.

The error amplifier output (COMP, pin #4), offset by -1 V, is then compared with the Ton ramp signal by the PWM comparator. Thus, the PWM comparator stops the on-time when $V_{TON} = V_{COMP} - 1$ V. The error amplifier output can swing from 1 V (burst mode threshold) up to 4.5 V (upper value).

The on-time generator delivers a constant current charging an external capacitor connected to the Ton pin (#5) used to determine the MOSFET on-time each cycle.

To keep the maximum output power deliverable by the PFC almost constant with respect to the ac input voltage, a two-level, discrete voltage feedforward (VFF) is integrated in the STCMB1. The ac input voltage is monitored via the HV pin (#1) and the signal is fed into a peak detector. This information is used to properly set the value of the current ITON sourced by the TON pin during the normal operation to determine the on-time of the power switch. The threshold aimed to select the proper value of the current ITON is set between 145 and 160 Vac_rms. The proper operation of the PFC, with the right ITON current, is guaranteed below 145 Vac_rms and above 160 Vac_rms.

Whereas mains voltage rises are detected immediately, mains voltage drops are detected after a latency of 16 ms.

Because of this latency, particular attention in the design of the application must be paid to account for line transients that span across the mains ranges. To avoid that the half-bridge shuts down due to the dc brown-out function being triggered (see *Section 7.16: Dc brown-out function (HB enable and disable) on page 30*), the following relationship has to be fulfilled:

Equation 10

$$C_{bulk} \frac{\Delta V_{OUT}}{I_{LOAD}} > 16 \text{ ms}$$

where:

a) C_{bulk} is the output capacitor of the PFC stage.

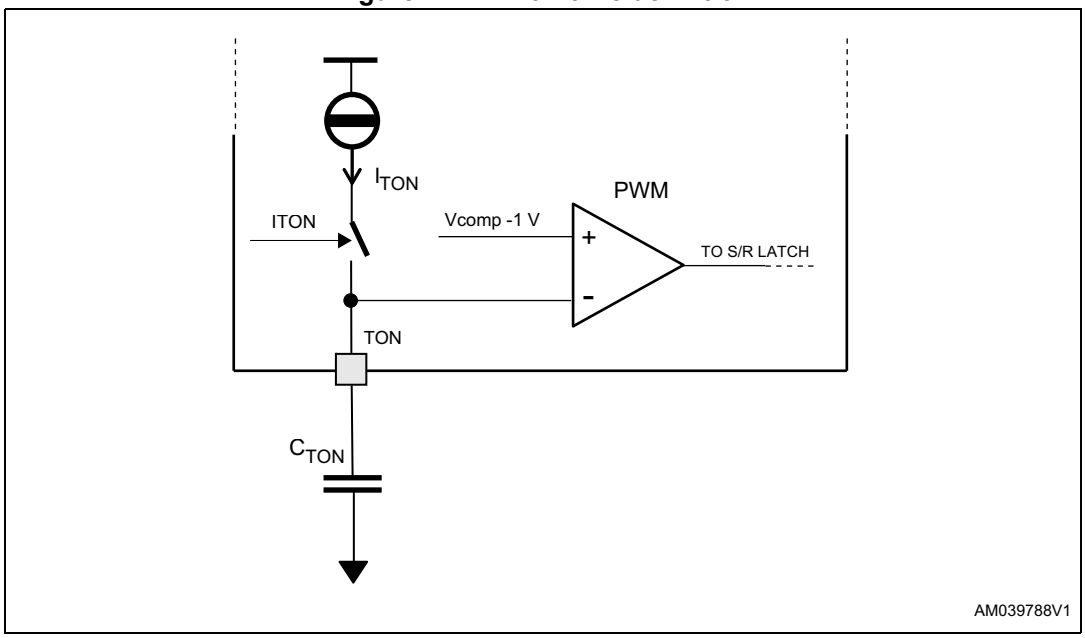
b) ΔV_{OUT} is the maximum allowed output voltage drop (the difference between the regulated output voltage V_{REG} and the dc brown-out threshold (280 V if V_{REG} = 400 V).

c) $I_{LOAD} = P_{OUT}/V_{REG}$ is the output current delivered by the PFC stage and provided to the downstream half-bridge.

7.8 PFC: C_{TON} calculation

Figure 11 shows how the PFC on-time is defined by the PWM comparator, as explained in *Section 7.7: PFC: error amplifier, regulation loop and V_{FF}*.

Figure 11. PFC on-time definition



In detail, C_{TON} must be larger than the maximum on-time T_{ON_MAX} required to carry the maximum power demanded by the load of the PFC stage with the minimum specified ac voltage. The T_{ON_MAX} is a known parameter once the power stage has been designed, in fact:

Equation 11

$$T_{ON\_MAX} = L \frac{ILPk}{\sqrt{2}\ VACmin}$$

The maximum programmable on-time is achieved when the output of the error amplifier is saturated high. This must occur even when the saturation voltage spreads at its minimum value ($V_{COMPSAT\_MIN}$ = 4.2 V for a consumer temperature range design, 4 V for an extended temperature range design).

Therefore, since during the on-time (GD_PFC high) the current generator I_{TON} raises the voltage V(TON) across the capacitor C_{TON}, it is possible to find the minimum C_{TON} value according to the following relationship:

Equation 12

$$C_{TON\_MIN} = T_{ON\_MAX} \cdot \frac{I_{TON\_MAX}}{V_{COMPSAT\_MIN} - 1V}$$

Since this relationship is referred to the minimum input voltage, the appropriate value of I_{TON_MAX} must be used: I_{TON} = 200 µA (I_{TON_MAX} = 220 µA) in US, Japan, or wide-range mains applications, I_{TON} = 800 µA (I_{TON_MAX} = 960 µA) in European mains applications (these value are reported in *Table 4 on page 11*).

7.9 PFC: light-load operation

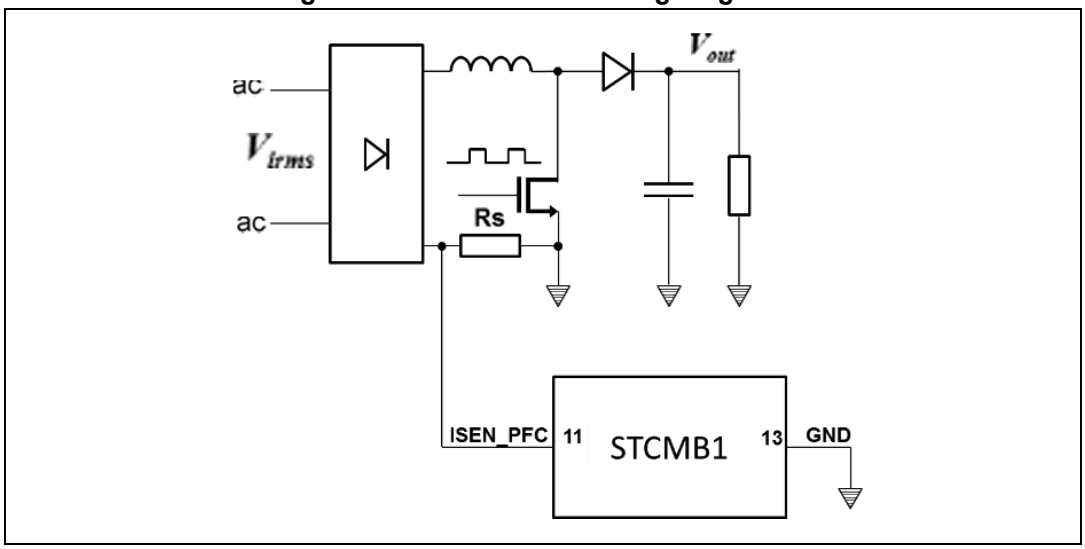
In case of the light-load operation the PFC can work in the burst mode in two ways:

1. If the output of the error amplifier decreases to 1 V an internal comparator stops the switching activity, independently by the HB stage. This burst mode is intended to be used in case of the light-load operation at high mains, in case the burst mode of the HB resonant stage is not used or has a threshold set at the very low load.
2. If the HB resonant stage detects a light-load and begins working in the burst mode will force the PFC working synchronized in the burst mode too. In detail, when the LLC enters in the idle state of the burst mode, the last PFC pulse is reset, in its natural way, by TON reaching COMP - 1 V. Conversely, when the LLC restarts switching, at the end of the idle state, the first PFC pulse is delayed of about 10 µs with respect to the first LLC pulse. Further details in *Section 7.20: HB: improved burst mode operation at light-load on page 37*.

Note that the connection of an oscilloscope probes to the COMP pin, when the PFC is in the deep burst mode, could modify the proper operation of the PFC.

7.10 PFC: inductor current sensing on ground return and PFC OCP

Figure 12. PFC current sensing on ground



The STCMB1 implements the PFC current sensing on the ground return path, by means of the ISEN_PFC pin. In this way the signal fed into that pin has the information of the current level during the entire switching period, differently from other systems monitoring the current during the PFC MOSFET on-time only.

Monitoring the current during the whole switching period allows safe handling of inductor saturation conditions: an internal comparator enables the MOSFET to be turned on only if the inductor has completed its demagnetization, not before. This mechanism prevents the MOSFET from turning on with incomplete inductor demagnetization, for example following a mains dip or during an inrush current charging the bulk capacitor. Both these situations might result in very dangerous condition for the MOSFET because of the very low impedance of a saturated coil.