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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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STCN75

Digital temperature sensor and thermal watchdog

Datasheet – production data

Features

- Measures temperatures from –55 °C to +125 °C (–67 °F to +257 °F)
  - ±0.5 °C (typ) accuracy
  - ±2 °C (max) accuracy from –25 °C to +100 °C
- Low operating current:125 µA (typ)
- No external components required
- 2-wire I^2C/SMBus-compatible serial interface
  - Selectable bus address allows connection of up to eight devices on the bus
- Wide power supply range - operating voltage range: 2.7 V to 5.5 V
- Conversion time is 45 ms (typ)
- Programmable temperature threshold and hysteresis set points
- Pin- and software-compatible with TCN75 (drop-in replacement)
- Power-up defaults permit standalone operation as a thermostat
- Shutdown mode to minimize power consumption
- Output pin (open drain) can be configured for interrupt or comparator/thermostat mode (dual purpose event pin)
- MSOP8 (TSSOP8) package

MSOP8
(TSSOP8)

Contents

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1 Description

The STCN75 is a high-precision digital CMOS temperature sensor IC with a sigma-delta temperature-to-digital converter and an I^2C-compatible serial digital interface. It is targeted for general applications such as personal computers, system thermal management, electronics equipment, and industrial controllers, and is packaged in the industry-standard 8-lead TSSOP package.

The device contains a bandgap temperature sensor and 9-bit ADC which monitor and digitize the temperature to a resolution up to 0.5 °C. The STCN75 is typically accurate to (±3 °C - max) over the full temperature measurement range of –55 °C to 125 °C with ±2 °C accuracy in the –25 °C to +100 °C range. The STCN75 is pin-for-pin and software compatible with the TCN75.

The STCN75 is specified for operating at supply voltages from 2.7 V to 5.5 V. Operating at 3.3 V, the supply current is typically (125 µA).

The onboard sigma-delta analog-to-digital converter (ADC) converts the measured temperature to a digital value that is calibrated in degrees centigrade; for Fahrenheit applications a lookup table or conversion routine is required.

The STCN75 is factory-calibrated and requires no external components to measure temperature.

1.1 Serial communications

The STCN75 has a simple 2-wire I^2C-compatible digital serial interface which allows the user to access the data in the temperature register at any time. It communicates via the serial interface with a master controller which operates at speeds up to 400 kHz. Three pins (A0, A1, and A2) are available for address selection, and enable the user to connect up to 8 devices on the same bus without address conflict.

In addition, the serial interface gives the user easy access to all STCN75 registers to customize operation of the device.

1.2 Temperature sensor output

The STCN75 Temperature Sensor has a dedicated open drain overlimit signal/interrupt ($\overline{OS}$/INT) output which features a thermal alarm function. This function provides a user-programmable trip and turn-off temperature. It can operate in either of two selectable modes:

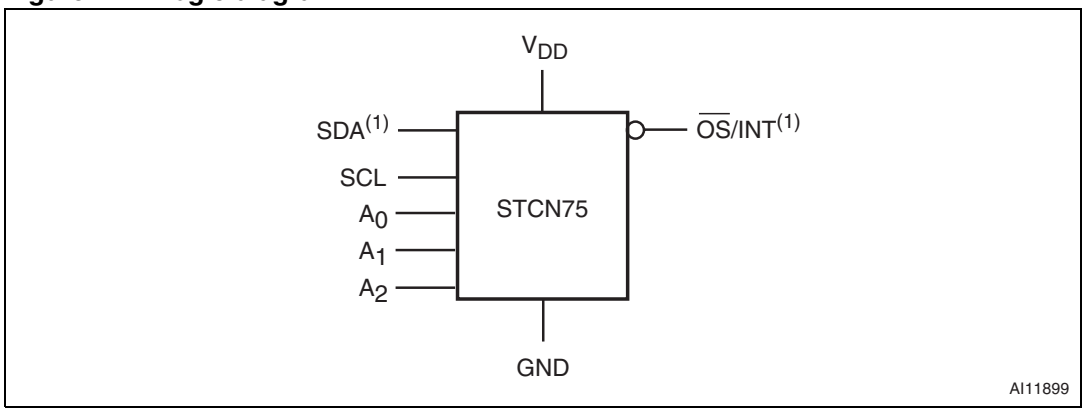
- *Section 2.3: Comparator mode*
- *Section 2.4: Interrupt mode*.

At power-up the STCN75 immediately begins measuring the temperature and converting the temperature to a digital value.

The measured temperature value is compared with a temperature limit (which is stored in the 16-bit (T_{OS}) READ/WRITE register), and the hysteresis temperature (which is stored in the 16-bit (T_{HYS}) READ/WRITE register). If the measured value exceeds these limits, the $\overline{OS}$/INT pin is activated (see *Figure 3 on page 8*).

Note: See Pin descriptions on page 8 for details.

Figure 1. Logic diagram



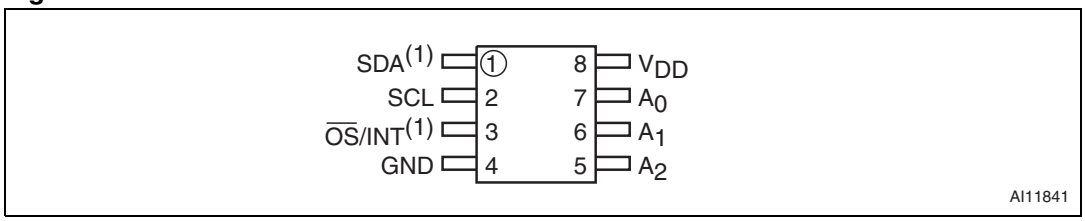
1. SDA and $\overline{OS}$/INT are open drain.

Table 1. Signal names

Pin	Sym	Type/direction	Description
1	SDA(1)	Input/output	Serial data input/output
2	SCL	Input	Serial clock input
3	$\overline{OS}$/INT(1)	Output	Overlimit signal/interrupt alert output
4	GND	Supply ground	Ground
5	A_2	Input	Address2 input
6	A_1	Input	Address1 input
7	A_0	Input	Address0 input
8	V_{DD}	Supply power	Supply voltage (2.7 V to 5.5 V)

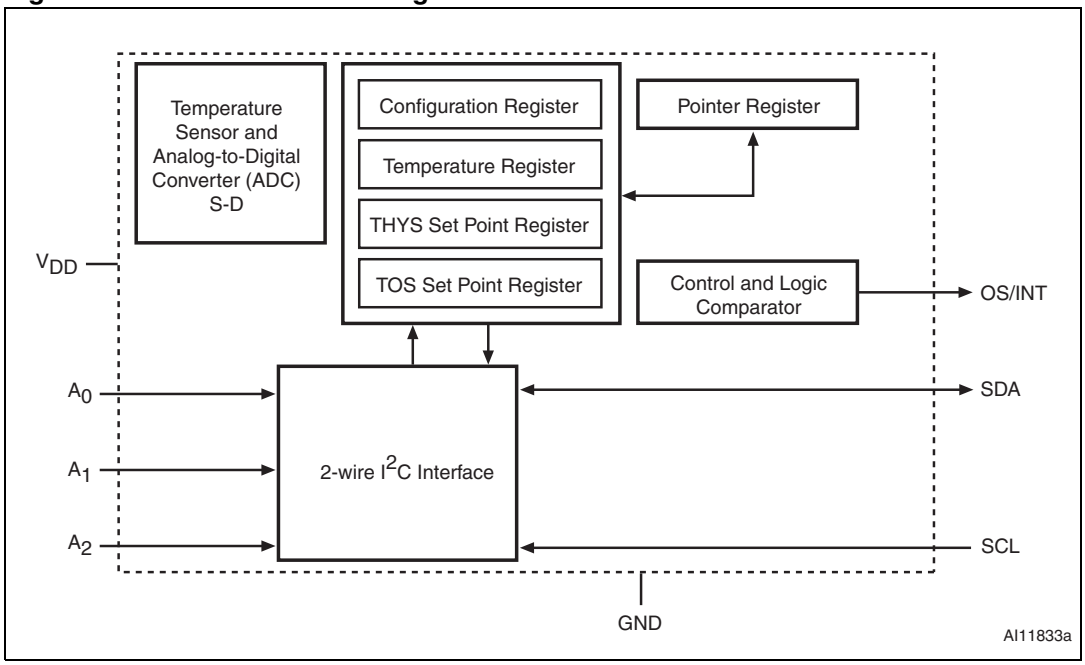
1. SDA and $\overline{OS}$/INT are open drain.

Figure 2. Connections



1. SDA and $\overline{OS}$/INT are open drain.

Figure 3. Functional block diagram



1.3 Pin descriptions

See *Figure 1 on page 7* and *Table 1 on page 7* for a brief overview of the signals connected to this device.

1.3.1 SDA (open drain)

This is the serial data input/output pin for the 2-wire serial communication port.

1.3.2 SCL

This is the serial clock input pin for the 2-wire serial communication port.

1.3.3 $\overline{OS}$/INT (open drain)

This is the overlimit signal/interrupt alert output pin. It is open drain, so it needs a pull-up resistor. In Interrupt mode, it outputs a pulse whenever the measured temperature exceeds the programmed threshold (T_{OS}). It behaves as a thermostat, toggling to indicate whether the measured temperature is above or below the threshold and hysteresis (T_{HYS}).

1.3.4 GND

Ground; it is the reference for the power supply. It must be connected to system ground.

1.3.5 A2, A1, A0

A2, A1, and A0 are selectable address pins for the 3 LSBs of the I^2C interface address. They can be set to V_{DD} or GND to provide 8 unique address selections.

1.3.6 V_{DD}

This is the supply voltage pin, and ranges from +2.7 V to +5.5 V.

2 Operation

After each temperature measurement and analog-to-digital conversion, the STCN75 stores the temperature as a 16-bit two's complement number (see *Table 5: Register pointers selection summary on page 16*) in the 2-byte temperature register (see *Table 7 on page 17*). The most significant bit (S) indicates if the temperature is positive or negative:

- for positive numbers S = 0, and
- for negative numbers S = 1.

The most recently converted digital measurement can be read from the temperature register at any time. Since temperature conversions are performed in the background, reading the temperature register does not affect the operation in progress.

The temperature data is provided by the 9 MSBs (bits 15 through 7). Bits 6 through 0 are unused. *Table 3 on page 14* gives examples of the digital output data and corresponding temperatures. The data is compared to the values in the T_{OS} and T_{HYS} registers, and then the $\overline{OS}$/INT is updated based on the result of the comparison and the operating mode.

The alarm fault tolerance is controlled by the FT1 and FT0 bits in the configuration register. They are used to set up a fault queue. This prevents false tripping of the $\overline{OS}$/INT pin when the STCN75 is used in a noisy environment (see *Table 2 on page 13*).

The active state of the $\overline{OS}$/INT output can be changed via the polarity bit (POL) in the configuration register. The power-up default is active-low.

If the user does not wish to use the thermostat capabilities of the STCN75, the $\overline{OS}$/INToutput should be left floating.

Note: If the thermostat is not used, the T_{OS} and T_{HYS} registers can be used for general storage of system data.

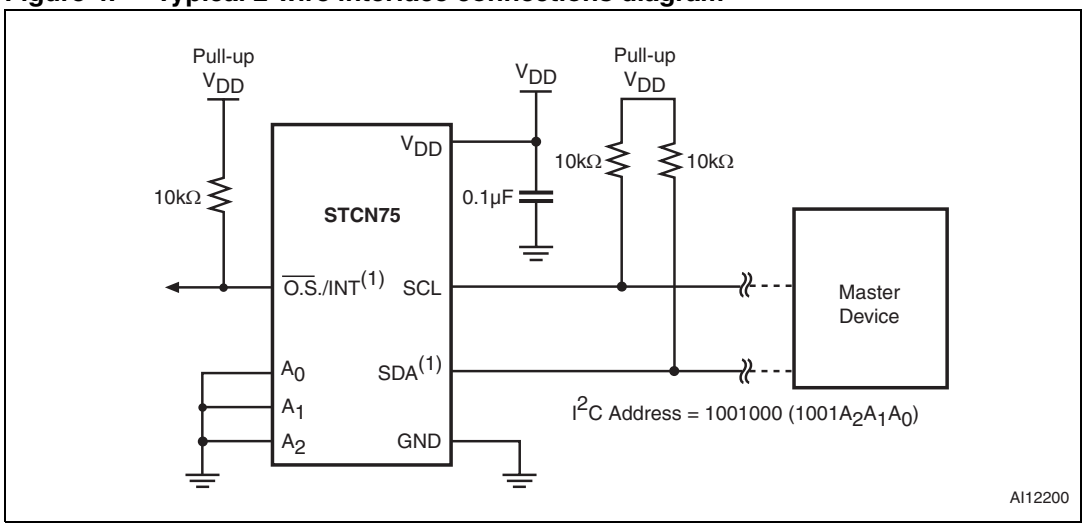
2.1 Applications information

STCN75 digital temperature sensors are optimal for thermal management and thermal protection applications. They require no external components for operations except for pull-up resistors on SCL, SDA, and $\overline{OS}$/INT outputs. A 0.1 µF bypass capacitor on V_{DD} is recommended. The sensing device of STCN75 is the chip itself. The typical interface connection for this type of digital sensor is shown in *Figure 4 on page 11*.

Intended applications include:

- System thermal management
- Computers/disk drivers
- Electronics/test equipment
- Power supply modules
- Consumer products
- Battery management
- Fax/printers management
- Automotive

Figure 4. Typical 2-wire interface connections diagram



1. SDA and $\overline{OS}$/INT are open drain.

2.2 Thermal alarm function

The STCN75 thermal alarm function provides user-programmable thermostat capability and allows the STCN75 to function as a standalone thermostat without using the serial interface. The $\overline{OS}$/INT output is the alarm output. This signal is an open drain output, and at power-up, this pin is configured with active-low polarity by default.

2.3 Comparator mode

In comparator mode, each time a temperature-to-digital (T-to-D) conversion occurs, the new digital temperature is compared to the value stored in the T_{OS} and T_{HYS} registers. If a fault tolerance number of consecutive temperature measurements are greater than the value stored in the T_{OS} register, the $\overline{OS}$/INT output will be asserted.

For example, if the FT1 and FT0 bits are equal to “10” (fault tolerance = 4), four consecutive temperature measurements must exceed T_{OS} to activate the $\overline{OS}$/INT output. Once the $\overline{OS}$/INT output is active, it will remain active until the first time the measured temperature drops below the temperature stored in the T_{HYS} register, whereupon it will reset to its inactive state.

Putting the device into shutdown mode does not clear $\overline{OS}$/INT in comparator mode.

2.4 Interrupt mode

In interrupt mode, the $\overline{OS}$/INT output becomes active when the measured temperature exceeds the T_{OS} value a consecutive number of times as determined by the fault tolerance bits (FT1, FT0) value in the configuration register. Once activated, the $\overline{OS}$/INT can only be cleared by reading from any register (temperature, configuration, T_{OS}, or T_{HYS}) on the device. Once the $\overline{OS}$/INT has been deactivated, it will only be reactivated when the measured temperature falls below the T_{HYS} value a consecutive number of times equal to the FT value. This mode is better suited for interrupt driven microprocessor based systems.

2.5 Fault tolerance

For both comparator and interrupt modes, the alarm “fault tolerance” setting plays a role in determining when the $\overline{OS}$/INT output will be activated. Fault tolerance refers to the number of consecutive times an error condition must be detected before the user is notified. Higher fault tolerance settings can help eliminate false alarms caused by noise in the system. The alarm fault tolerance is controlled by the bits (4 and 3) in the configuration register. These bits can be used to set the fault tolerance to 1, 2, 4, or 6 as shown in *Table 2*. At power-up, these bits both default to logic '0'.

Table 2. Fault tolerance setting

FT1	FT0	STCN75 (consecutive faults)	Comments
0	0	1	Power-up default
0	1	2	
1	0	4	
1	1	6	

Note: $\overline{OS}$ output will be asserted one t_{CONV} after fault tolerance is met, provided that the error condition remains.

2.6 Shutdown mode

For power-sensitive applications, the STCN75 offers a low-power shutdown mode. The SD bit in the configuration register controls shutdown mode. When SD is changed to logic '1,' the conversion in progress will be completed and the result stored in the temperature register, after which the STCN75 will go into a low-power standby state. The $\overline{OS}$/INT output will be cleared if the thermostat is operating in Interrupt mode and the $\overline{OS}$/INT will remain unchanged in comparator mode. The 2-wire interface remains operational in shutdown mode, and writing a '0' to the SD bit returns the STCN75 to normal operation.

2.7 Temperature data format

Table 3 shows the relationship between the output digital data and the external temperature. Temperature data for the temperature, T_{OS}, and T_{HYS} registers is represented as a 9-bit, two's complement word.

The left-most bit in the output data stream contains temperature polarity information for each conversion. If the sign bit is '0', the temperature is positive and if the sign bit is '1,' the temperature is negative.

Table 3. Relationship between temperature and digital output

Temperature	Digital output	
	Binary	HEX
+125 °C	0 1111 1010	0FAh
+25 °C	0 0011 0010	032h
+0.5 °C	0 0000 0001	001h
0 °C	0 0000 0000	000h
–0.5 °C	1 1111 1111	1FFh
–25 °C	1 1100 1110	1CEh
–40 °C	1 1011 0000	1B0h
–55 °C	1 1001 0010	192h

3 Functional description

The STCN75 registers have unique pointer designations which are defined in *Table 5 on page 16*. Whenever any READ/WRITE operation to the STCN75 register is desired, the user must “point” to the device register to be accessed.

All of these user-accessible registers can be accessed via the digital serial interface at anytime (see *Section 3.3: Serial interface on page 19*), and they include:

- Command register/address pointer register
- Configuration register
- Temperature register
- Overlimit signal temperature register (T_{OS})
- Hysteresis temperature register (T_{HYS})

3.1 Registers and register set formats

3.1.1 Command/pointer register

The most significant bits (MSBs) of the command register must always be zero. Writing a '1' into any of these bits will cause the current operation to be terminated (bit 2 through bit 7 must be kept '0', see *Table 4*).

Table 4. Command/pointer register format

MSB							LSB
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0	0	0	0	0	0	P1	P0
These bits must be ‘O’						Pointer/register select bits	

The command register retains pointer information between operations (see *Table 5*). Therefore, this register only needs to be updated once for consecutive READ operations from the same register. All bits in the command register default to '0' at power-up.

Table 5. Register pointers selection summary

Pointer value (H)	P1	P0	Name	Description	Width (bits)	Type (R/W)	Power-on default	Comments
00	0	0	TEMP	Temperature register	16	Read-only	N/A	To store measured temperature data
01	0	1	CONF	Configuration register	8	R/W	00	
02	1	0	T_{HYS}	Hysteresis register	16	R/W	4B00	Default = 75 °C
03	1	1	T_{OS}	Overtemperature shutdown	16	R/W	5000	Set point for overtemperature shutdown (T_{OS}) limit default = 80 °C

3.1.2 Configuration register

The configuration register is used to store the device settings such as device operation mode, $\overline{OS}$/INT operation mode, $\overline{OS}$/INT polarity, and $\overline{OS}$/INT fault queue.

The configuration register allows the user to program various options such as thermostat fault tolerance, thermostat polarity, thermostat operating mode, and shutdown mode. The user has READ/WRITE access to all of the bits in the configuration register except the MSB (Bit7), which is reserved as a “Read only” bit (see *Table 6*). The entire register is volatile and thus powers-up in its default state only.

Table 6. Configuration register format

Byte	MSB							LSB
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STCN75	0	0	0	FT1	FT0	POL	M	SD
Default	0	0	0	0	0	0	0	0

Keys:		
	SD = shutdown control bit	FT1 = fault tolerance1 bit
	M = thermostat mode(1)	Bit 5 = must be set to '0'.
	POL = output polarity(2)	Bit 6 = must be set to '0'.
	FT0 = fault tolerance0 bit	Bit 7 = must be set to '0'.

1. Indicates operation mode; 0 = comparator mode, and 1 = interrupt mode (see *Section 2.3: Comparator mode* and *Section 2.4: Interrupt mode*).
2. The $\overline{OS}$ is active-low ('0').

3.1.3 Temperature register

The temperature register is a two-byte (16-bit) “Read only” register (see *Table 7*). Digital temperatures from the T-to-D converter are stored in the temperature register in two’s complement format, and the contents of this register are updated each time the T-to-D conversion is finished.

The user can read data from the temperature register at any time. When a T-to-D conversion is completed, the new data is loaded into a comparator buffer to evaluate fault conditions and will update the temperature register if a read cycle is not ongoing. If a READ is ongoing, the previous temperature will be read. Accessing the STCN75 continuously without waiting at least one conversion time between communications will prevent the device from updating the temperature register with a new temperature conversion result. Consequently, the STCN75 should not be accessed continuously with a wait time of less than t_{CONV} (max).

All unused bits following the digital temperature will be zero. The MSB position of the temperature register always contains the sign bit for the digital temperature, and bit 14 contains the temperature MSB. All bits in the temperature register default to zero at power-up.

Table 7. Temperature register format(1)

Bytes	HS byte								LS byte							
Bits	MSB	TMSB							TLSB							LSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STCN75	TD8 (S)	TD7 (TMSB)	TD 6	TD 5	TD 4	TD 3	TD 2	TD 1	TD0 (TLSB)	x	x	x	x	x	x	x

Keys:	S = two’s complement sign bit
	TMSB = temperature MSB
	TLSB = temperature LSB
	TDx = temperature data bits

1. These are comparable formats to the LM75.

3.1.4 Overlimit temperature register (T_{OS})

T_{OS} register is a two-byte (16-bit) READ/WRITE register that stores the user-programmable upper trip-point temperature for the thermal alarm in two’s complement format (see *Table 8 on page 18*). This register defaults to 80 °C at power-up (i.e., 0101 0000 0000 0000).

The format of the T_{OS} register is identical to that of the temperature register. The MSB position contains the sign bit for the digital temperature and Bit14 contains the temperature MSB.

For 9-bit conversions, the trip-point temperature is defined by the 9 MSBs of the T_{OS} register, and all remaining bits are “Don’t cares” (x).

3.1.5 Hysteresis temperature register (T_{HYS})

T_{HYS} register is a two-byte (16-bit) READ/WRITE register that stores the user-programmable lower trip-point temperature for the thermal alarm in two's complement format (see *Table 8*). This register defaults to 75 °C at power-up (i.e., 0100 1011 0000 0000).

The format of this register is the same as that of the temperature register. The MSB position contains the sign bit for the digital temperature and bit 14 contains the temperature MSB.

Table 8. T_{OS} and T_{HYS} register format(1)

Bytes	HS byte								LS byte							
Bits	MSB	TMSB							TLSB							LSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STCN75	S	TMSB	TD	TD	TD	TD	TD	TD	9-bit TLSB	0	0	0	0	0	0	0
Keys:	S = two's complement sign bit															
	TMSB = temperature MSB															
	TLSB = temperature LSB															
	TD = temperature Data															

1. These are comparable formats to the DS75 and LM75.

3.2 Power-up default conditions

The STCN75 always powers up in the following default states:

- Thermostat mode = comparator mode
- Polarity = active-low
- Fault tolerance = 1 fault (i.e., relevant bits set to '0' in the configuration register)
- T_{OS} = 80 °C
- T_{HYS} = 75 °C
- Register pointer = 00 (temperature register)

Note: After power-up these conditions can be reprogrammed via the serial interface.

3.3 Serial interface

Writing to and reading from the STCN75 registers is accomplished via the two-wire serial interface protocol which requires that one device on the bus initiates and controls all READ and WRITE operations. This device is called the “master” device. The master device also generates the SCL signal which provides the clock signal for all other devices on the bus. These other devices on the bus are called “slave” devices. The STCN75 is a slave device (see *Table 9*). Both the master and slave devices can send and receive data on the bus.

During operations, one data bit is transmitted per clock cycle. All operations follow a repeating, nine-clock-cycle pattern that consists of eight bits (one byte) of transmitted data followed by an acknowledge (ACK) or not acknowledge (NACK) from the receiving device.

Note: There are no unused clock cycles during any operation, so there must not be any breaks in the data stream and ACKs/NACKs during data transfers. Consequently, having too few clock cycles can lead to incorrect operation if an inadvertent 8-bit READ from a 16-bit register occurs. So, the entire word must be transferred out regardless of the superflous trailing zeroes.

Table 9. STCN75 serial bus slave addresses

MSB							LSB
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
1	0	0	1	A2	A1	A0	R/W

3.4 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined (see *Figure 5 on page 20*):

3.4.1 Bus not busy

Both data and clock lines remain high.

3.4.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

3.4.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

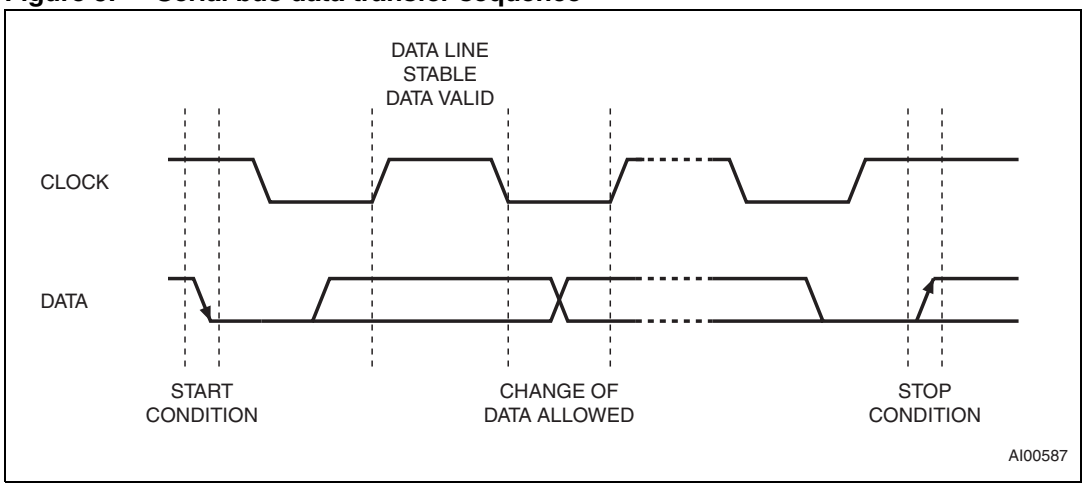
3.4.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter”, the receiving device that gets the message is called “receiver”. The device that controls the message is called “master”. The devices that are controlled by the master are called “slaves”.

Figure 5. Serial bus data transfer sequence

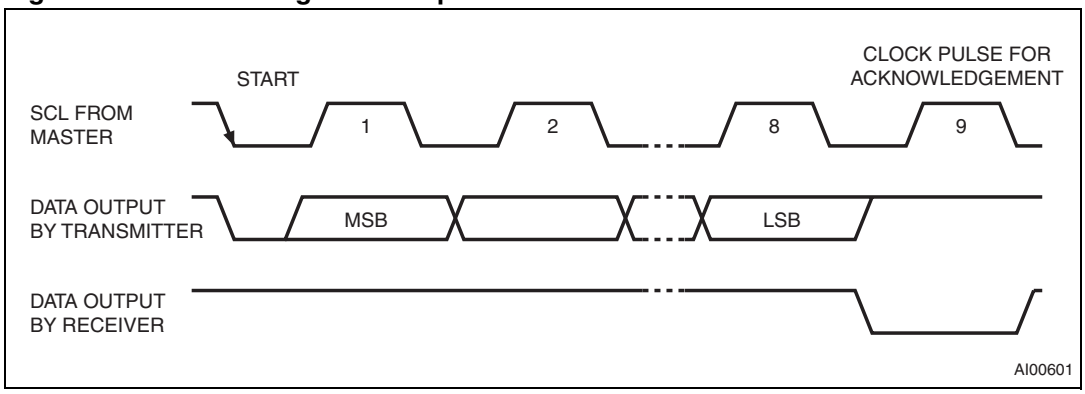


3.4.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse (see *Figure 6 on page 21*). A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 6. Acknowledgement sequence



3.5 READ mode

In this mode the master reads the STCN75 slave after setting the slave address (see *Figure 7*). Following the WRITE mode control bit (R/$\overline{W}$=0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer.

There are two READ modes:

- Preset pointer locations (e.g. temperature, T_{OS} and T_{HYS} registers), and
- Pointer setting (the pointer has to be set for the register that is to be read)

Note: The temperature register pointer is usually the default pointer.

These modes are shown in the READ mode typical timing diagrams (see *Figure 8*, *Figure 9*, and *Figure 10 on page 22*).

Figure 7. Slave address location

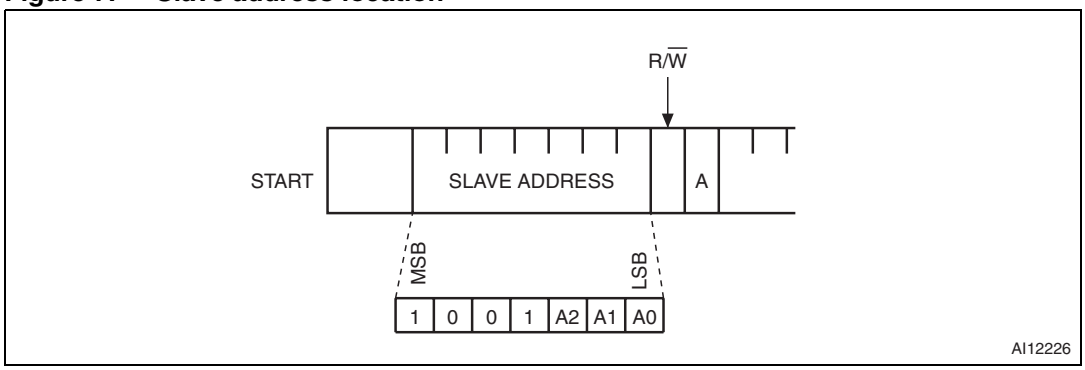


Figure 8. Typical 2-byte READ from preset pointer location (e.g. temp - T_{OS}, T_{HYS})

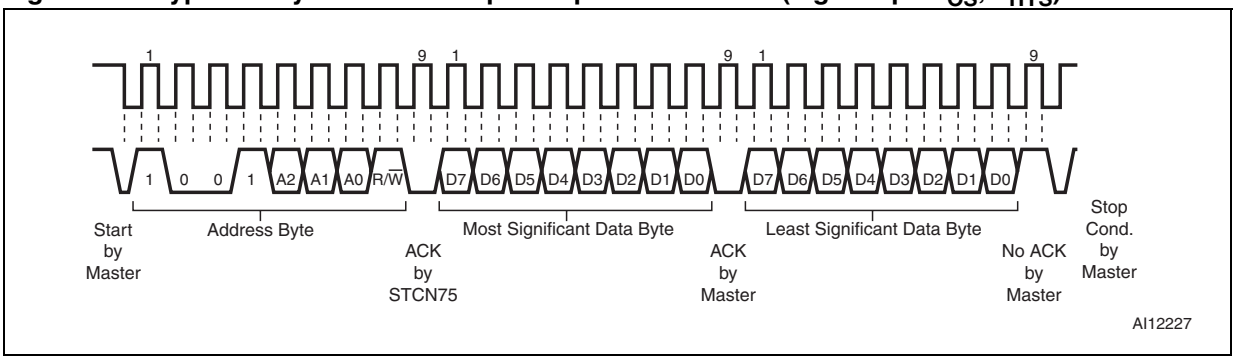


Figure 9. Typical pointer set followed by an immediate READ for 2-byte register (e.g. temp)

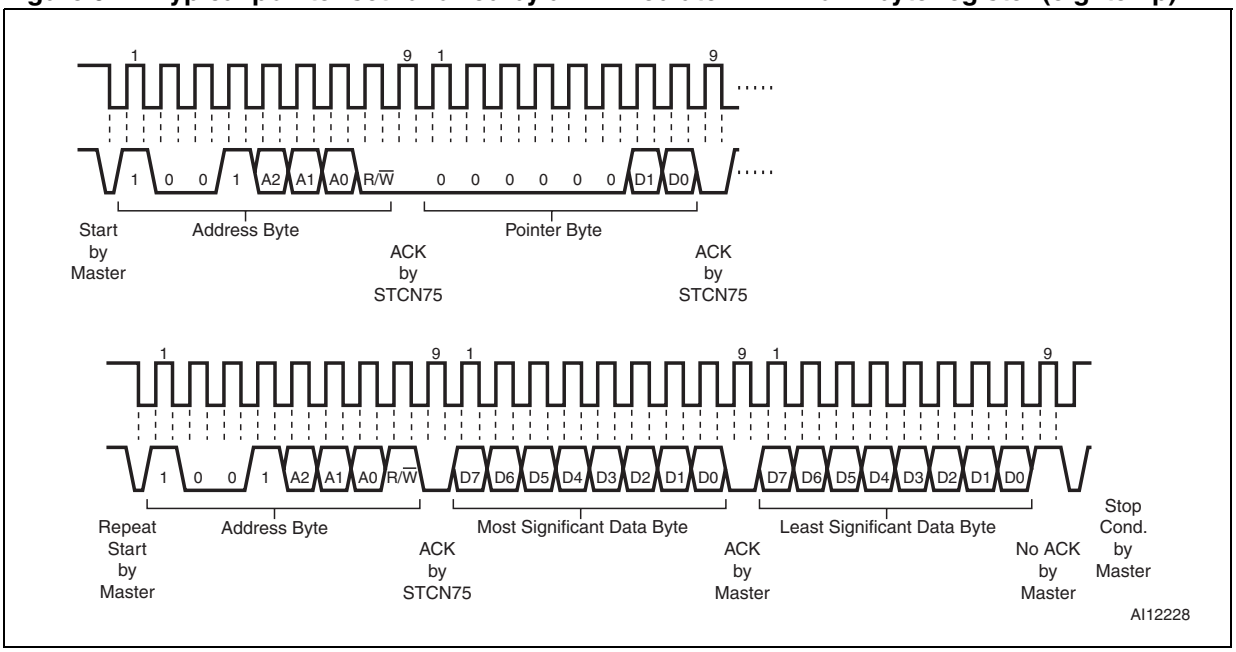
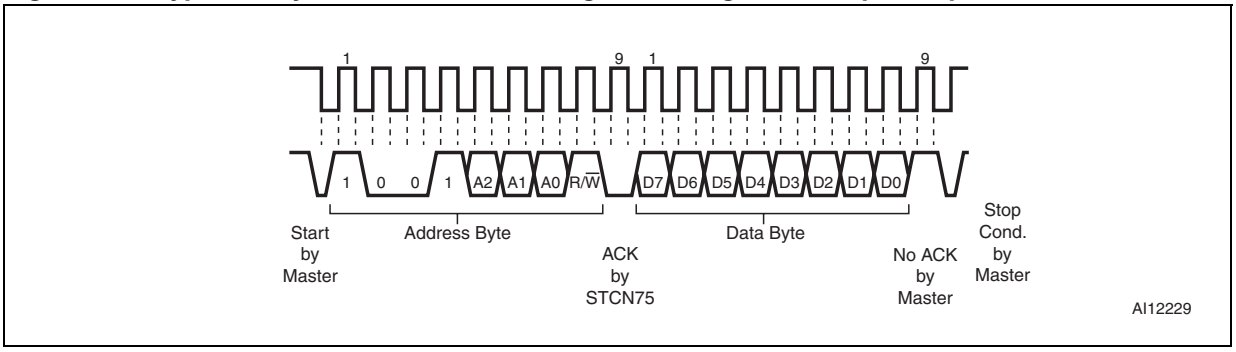


Figure 10. Typical 1-byte READ from the cofiguration register with preset pointer



3.6 WRITE mode

In this mode the master transmitter transmits to the STCN75 slave receiver. Bus protocol is shown in *Figure 11*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$ = 0) is placed on the bus and indicates to the addressed device that word address will follow and is to be written to the on-chip address pointer.

These modes are shown in the WRITE mode typical timing diagrams (see *Figure 11*, and *Figure 12*, and *Figure 13 on page 24*).

Figure 11. Typical pointer set followed by an immediate READ from the configuration register

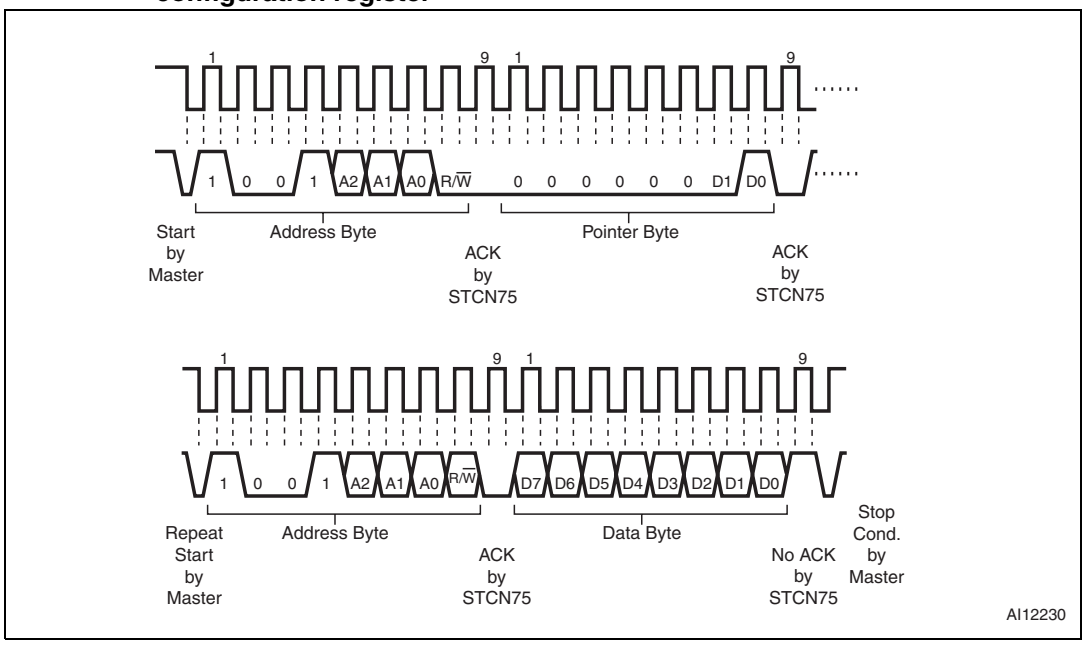


Figure 12. Configuration register WRITE

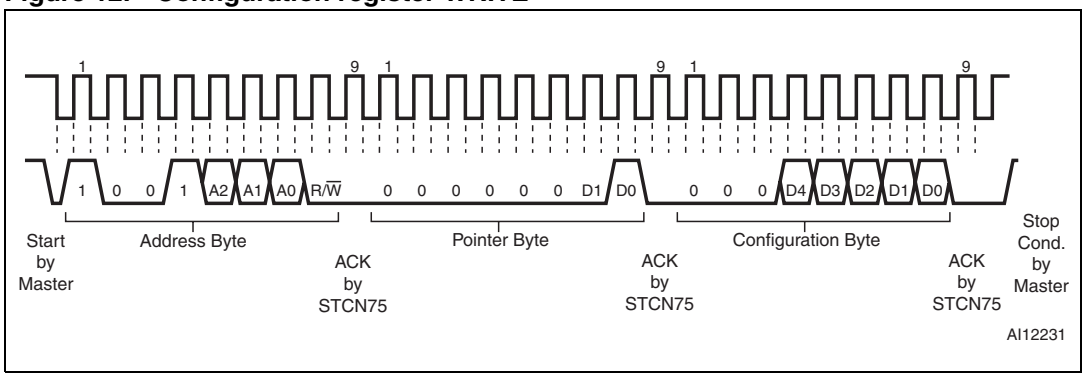
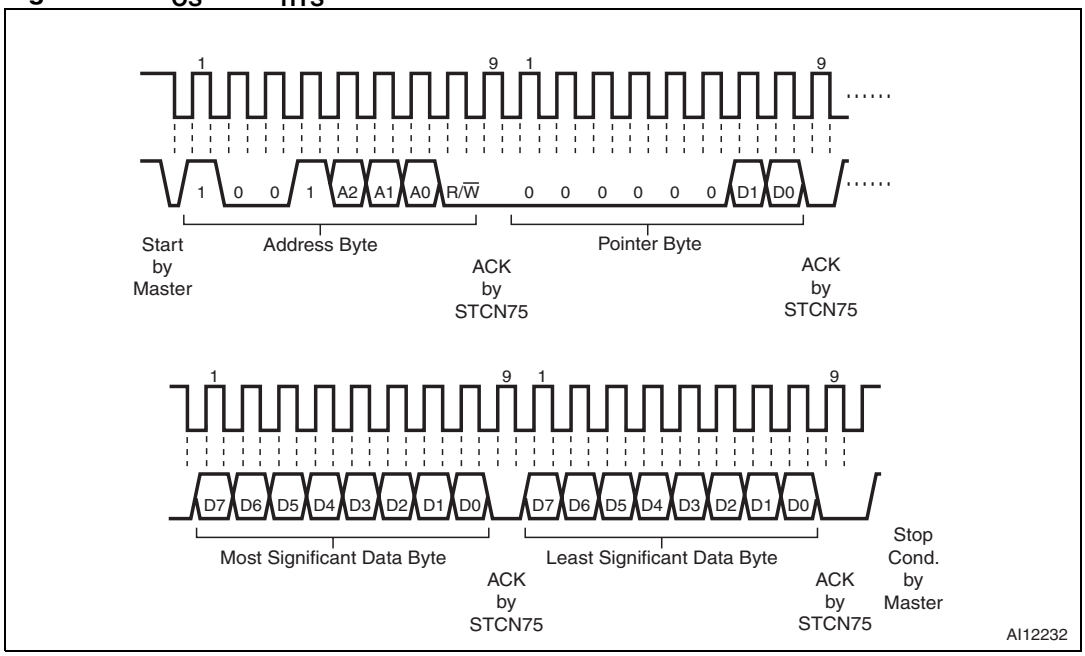


Figure 13. T_{OS} and T_{HYS} WRITE



4 Typical operating characteristics

Figure 14. Temperature variation vs. voltage