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## STD40NF3LL

N-channel 30V - 0.009Ω - 40A - DPAK  
Low gate charge STripFET™ II Power MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD40NF3LL	30V	<0.011Ω	40A

- Logic level device
- Optimal R<sub>DS(on)</sub> x Q<sub>g</sub> trade-off
- Conduction losses reduced
- Switching losses reduced
- Low threshold drive

### Description

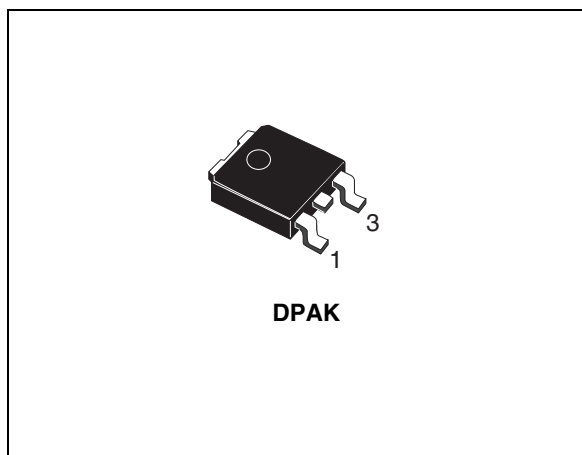
This application specific Power MOSFET is the third generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

### Applications

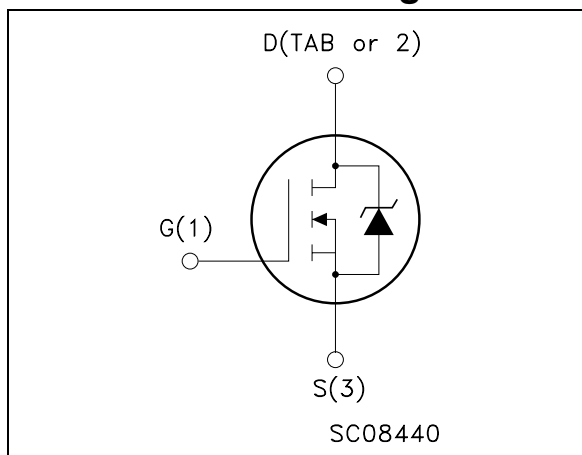
- Switching application

### Order codes

Part number	Marking	Package	Packaging
STD40NF3LLT4	D40NF3LL@	DPAK	Tape & reel



### Internal schematic diagram



## Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )	30	V
$V_{GS}$	Gate- source voltage	$\pm 16$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	40	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	28	A
$I_{DM}^{(2)}$	Drain current (pulsed)	160	A
$P_{tot}$	Total dissipation at $T_C = 25^\circ\text{C}$	80	W
	Derating Factor	0.53	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	5.5	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	850	mJ
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_j$	Max. operating junction temperature		

1. Current limited by package
2. Pulse width limited by safe operating area.
3.  $I_{SD} \leq 40\text{A}$ ,  $di/dt \leq 350\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$
4. Starting  $T_j = 25^\circ\text{C}$ ,  $I_D = 20\text{A}$ ,  $V_{DD} = 25\text{V}$

**Table 2. Thermal data**

$R_{thj-case}$	Thermal resistance junction-case max	1.88	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	100	$^\circ\text{C}/\text{W}$
$T_J$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating},$ $T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 16V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 20A$ $V_{GS} = 4.5V, I_D = 10A$		0.0090 0.0115	0.0110 0.0135	$\Omega$ $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 20A$		23		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1MHz,$ $V_{GS} = 0$		1650		pF
$C_{oss}$	Output capacitance			540		pF
$C_{rss}$	Reverse transfer capacitance			130		pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15V, I_D = 20A$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (see <a href="#">Figure 13</a> )		23		ns
$t_r$	Rise time			156		ns
$t_{d(off)}$	Turn-off delay time			27		ns
$t_f$	Fall time			28		ns
$Q_g$	Total gate charge	$V_{DD} = 15V, I_D = 20A,$ $V_{GS} = 4.5V, R_G = 4.7\Omega$ (see <a href="#">Figure 14</a> )		24	33	nC
$Q_{gs}$	Gate-source charge			8.5		nC
$Q_{gd}$	Gate-drain charge			12		nC

1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5%.

**Table 5. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				40 160	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 40A, V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 40A, di/dt = 100A/\mu s,$ $V_{DD} = 15V, T_j = 150^\circ C$ (see <a href="#">Figure 15</a> )		40 50 2.5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

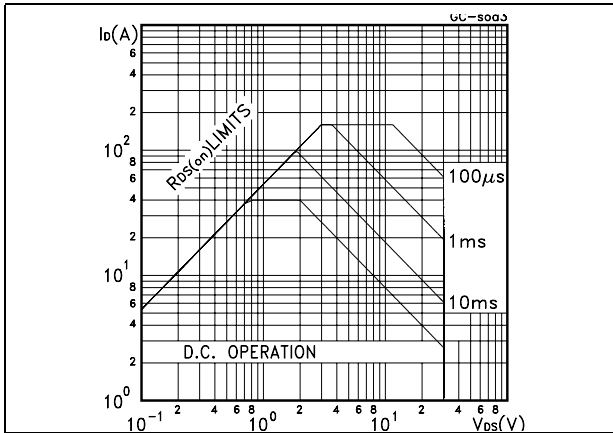


Figure 2. Thermal impedance

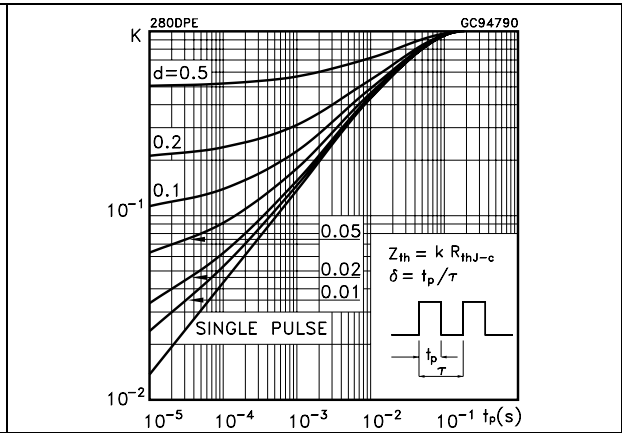


Figure 3. Output characteristics

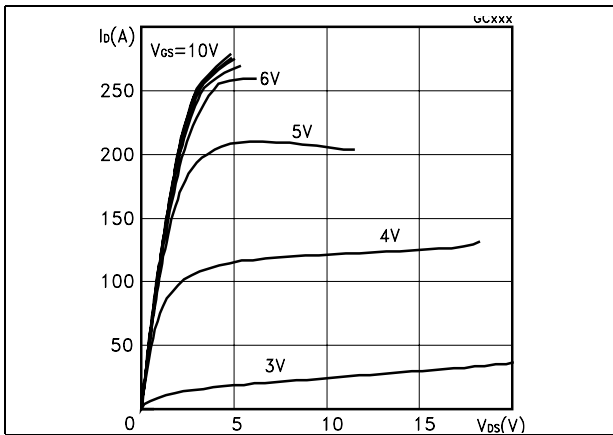


Figure 4. Transfer characteristics

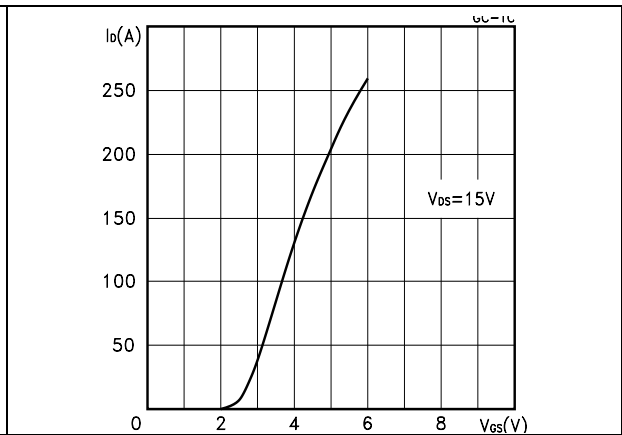


Figure 5. Transconductance

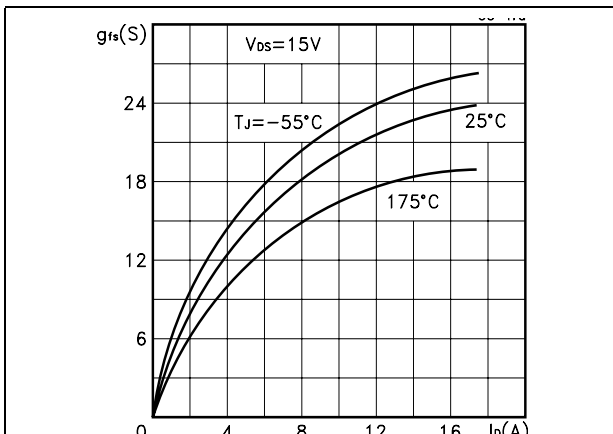


Figure 6. Static drain-source on resistance

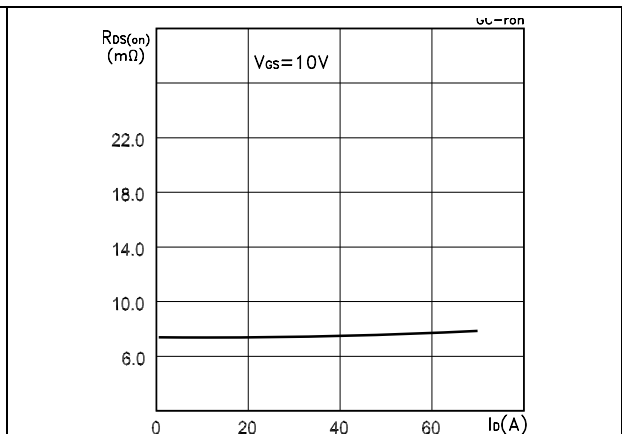


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

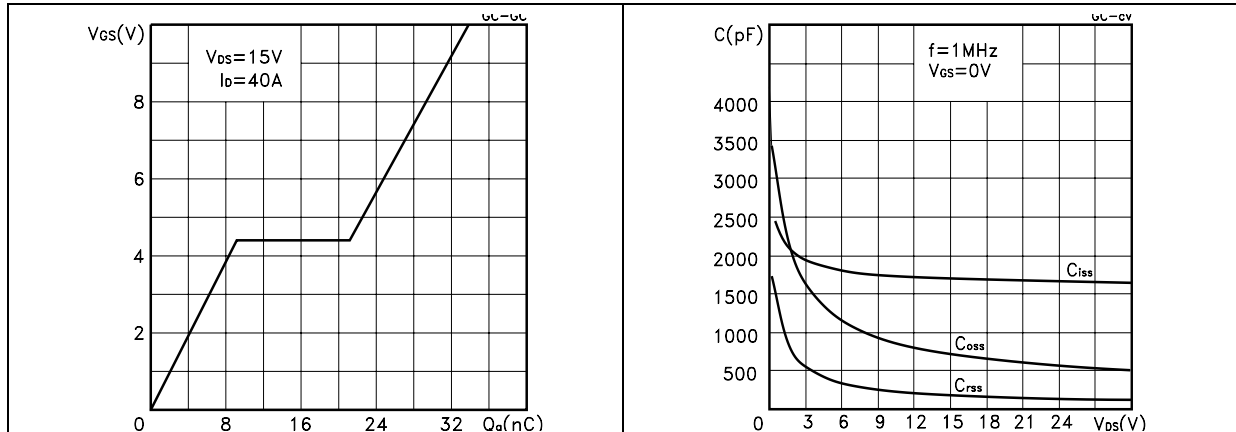


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

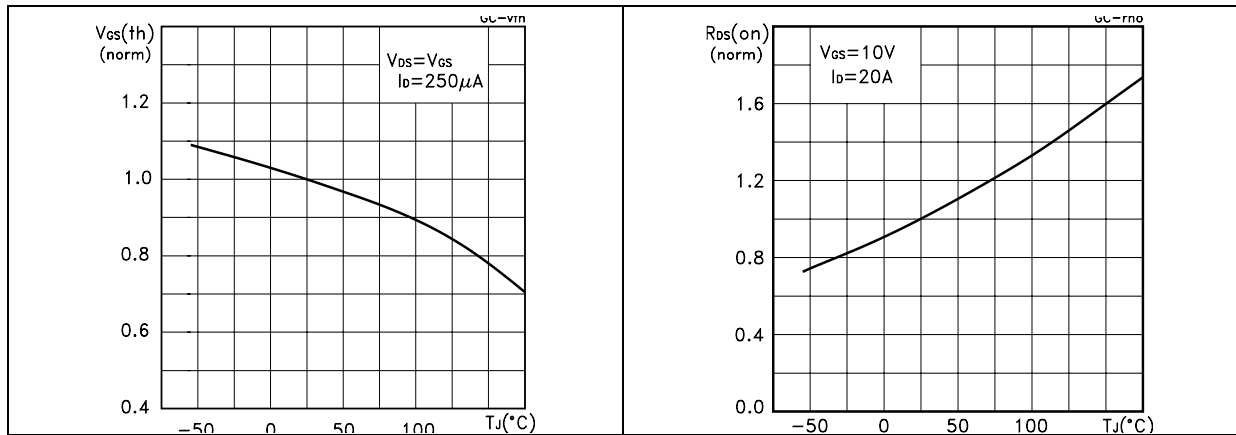
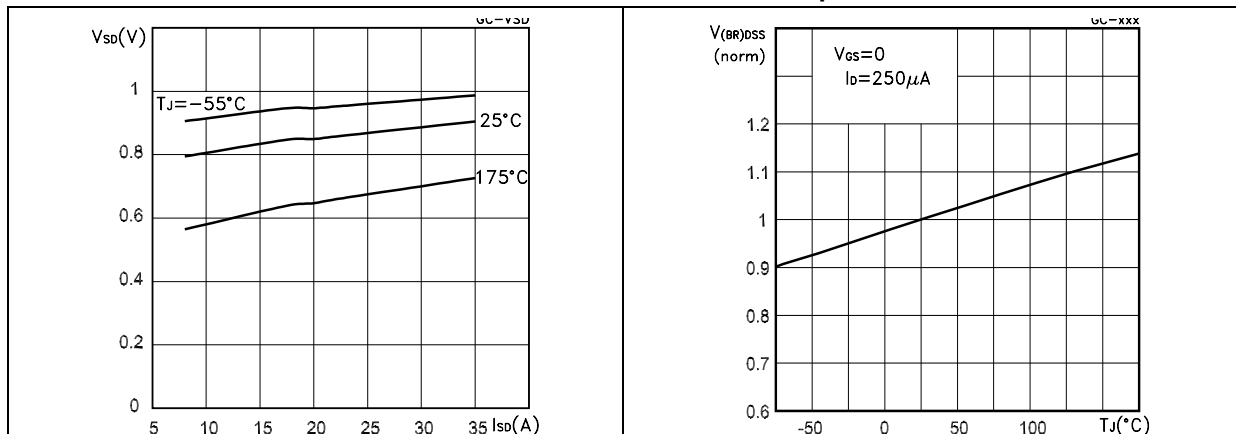


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs. temperature



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

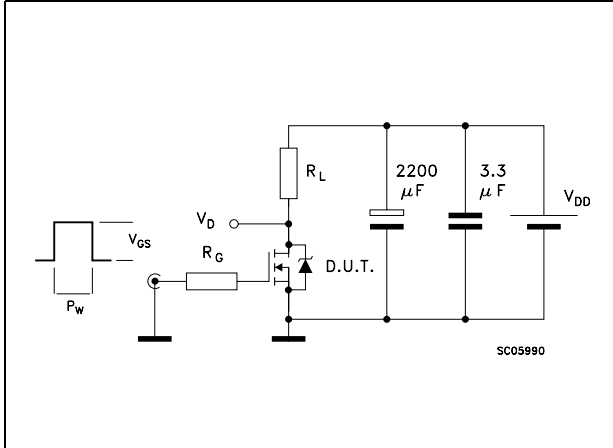


Figure 14. Gate charge test circuit

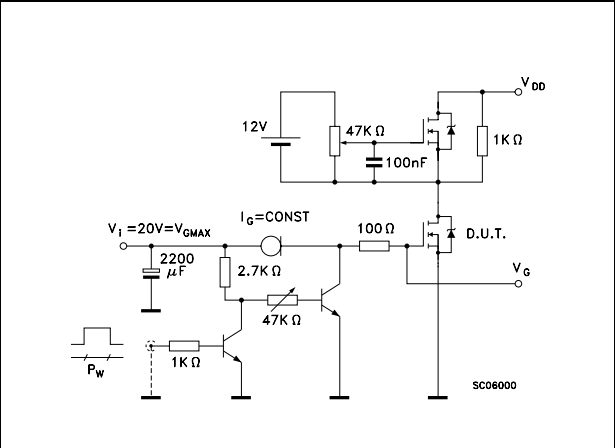


Figure 15. Test circuit for inductive load switching and diode recovery times

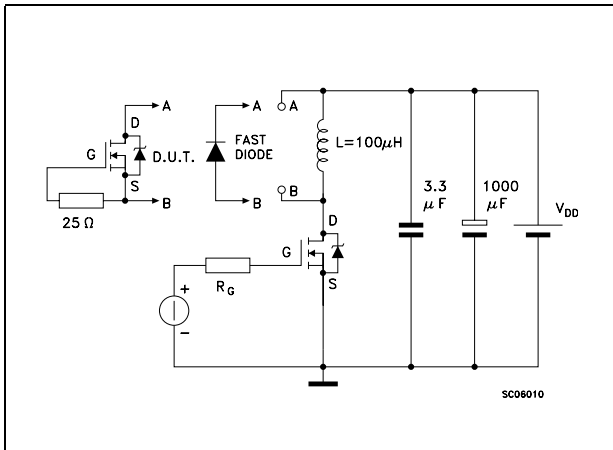


Figure 16. Unclamped Inductive load test circuit

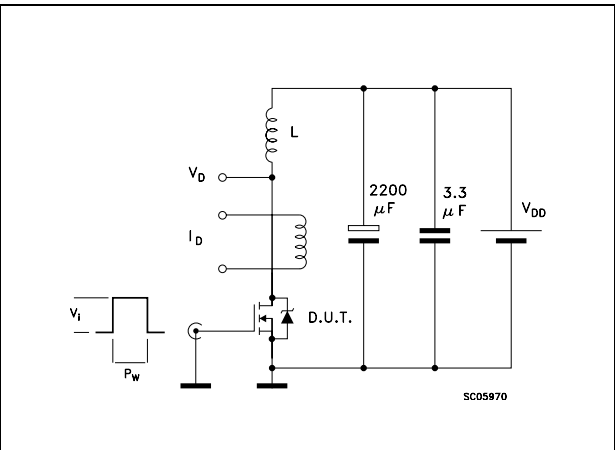


Figure 17. Unclamped inductive waveform

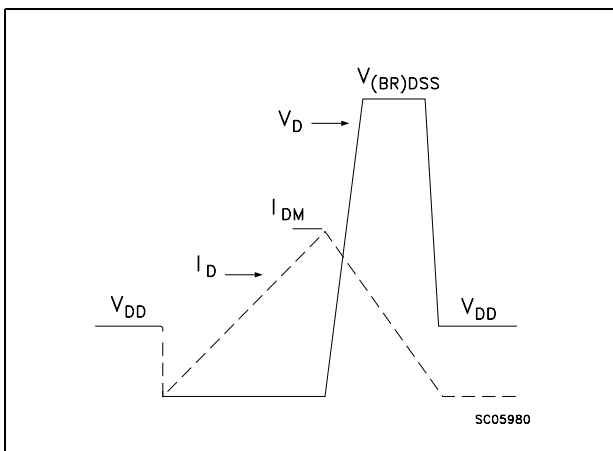
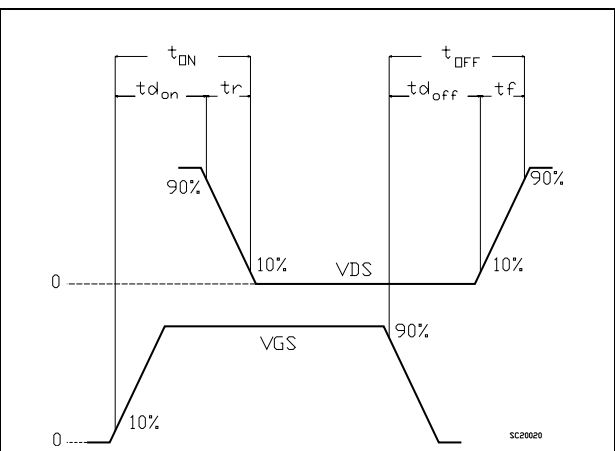


Figure 18. Switching time waveform

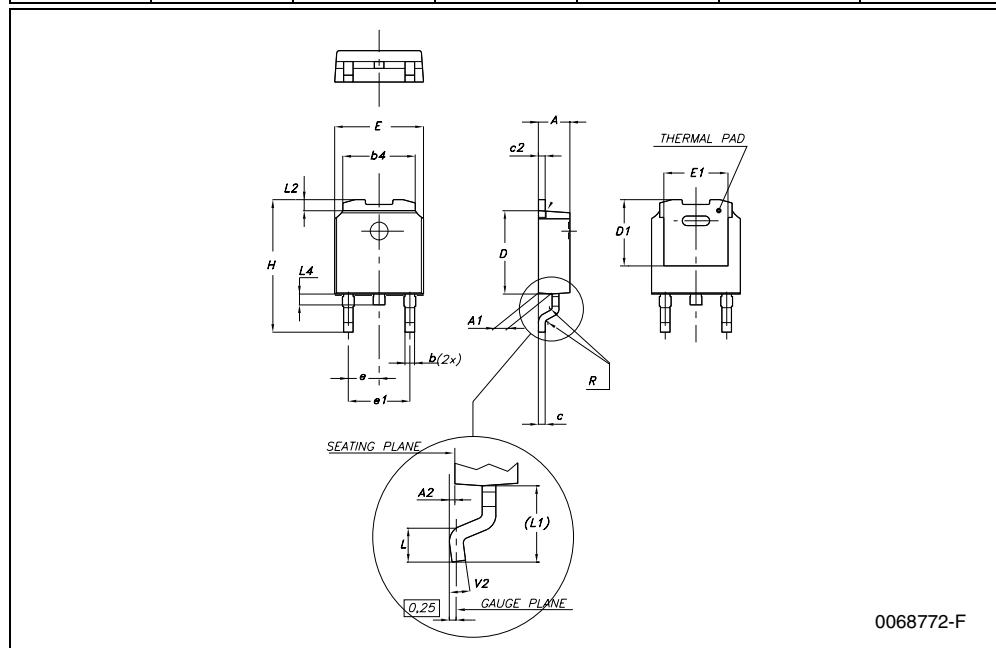


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**DPAK MECHANICAL DATA**

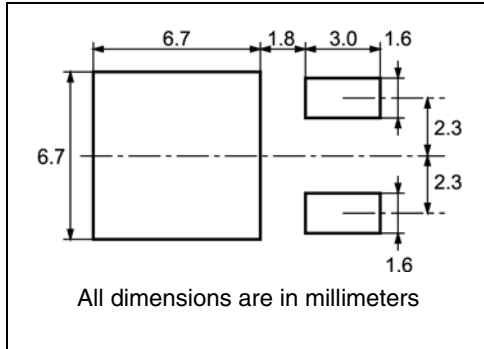
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



0068772-F

# 5 Packing mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

### REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

### TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

User Direction of Feed

Center line of cavity

Bending radius

FEED DIRECTION

TRL

10 pitches cumulative tolerance on tape +/- 0.2 mm

For machine ref. only including draft and radii concentric around B0

## 6 Revision history

**Table 6. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
21-Jun-2004	3	New datasheet according to PCN DSG/CT/2C13 marking:D40NF3LL@
11-Jul-2006	4	New template, no content change
20-Feb-2007	5	Typo mistake on page 1

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