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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Complementary transistor pair in a single package

Datasheet — production data

Features

- Low $V_{CE(sat)}$
- Simplified circuit design
- Reduced component count
- Low spread of dynamic parameters

Application

- Compact fluorescent lamp (CFL) 220 V mains

Description

The STD815CP40 is a hybrid complementary pair of power bipolar transistors manufactured by using the high voltage multi-epitaxial planar technology for high switching speeds and medium voltage capability.

The STD815CP40 is housed in dual island DIP-8 package with separated terminals for higher assembly flexibility, specifically recommended to be used in a new solution for compact fluorescent lamp (CFL).

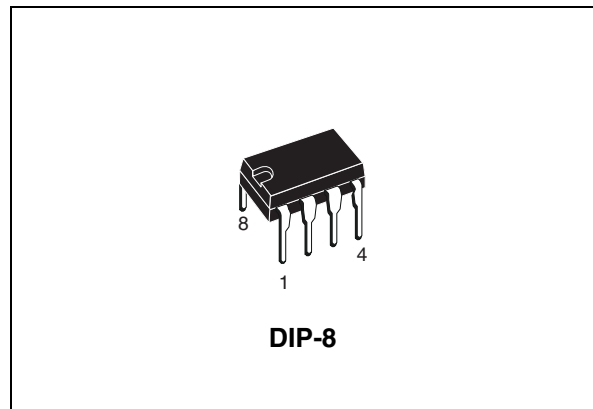


Figure 1. Internal schematic diagram

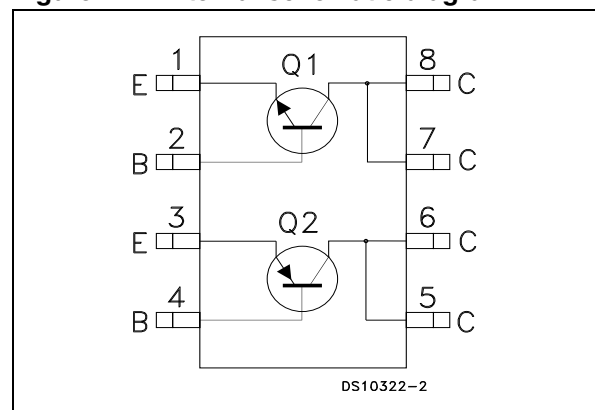


Table 1. Device summary

Order code	Marking	Package	Packing
STD815CP40	D815CP40	DIP-8	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		NPN	PNP	
V_{CBO}	Collector-base voltage ($I_E = 0$)	700	500	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	400		V
V_{EBO}	Emitter-base voltage ($I_C = 0$, $I_B = 0.75$ A, $t_p < 10$ ms)	$V_{(BR)EBO}$		V
I_C	Collector current	1.5		A
I_{CM}	Collector peak current ($t_p < 5$ ms)	3		A
I_B	Base current	0.75		A
I_{BM}	Base peak current ($t_p < 1$ ms)	1.5		A
P_{TOT}	Total dissipation at $T_{amb} = 25$ °C single transistor	2.6		W
P_{TOT}	Total dissipation at $T_{case} = 25$ °C single transistor	45		W
T_{STG}	Storage temperature	- 65 to 150		°C
T_J	Max. operating junction temperature	150		°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance junction-ambient (single transistor)	48	°C/W
$R_{thJC}^{(1)}$	Thermal resistance junction-case (single transistor)	2.7	°C/W

1. When mounted on 25mm square pad of 2 oz. copper, $t \leq 10$ sec.

Note: For PNP types voltage and current values are negative.

2 Electrical characteristics

T_{case} = 25°C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{CES}	Collector cut-off current (V _{BE} = 0)	For NPN: V _{CE} = 700 V V _{CE} = 700 V T _C = 125°C			1 5	mA mA
		For PNP: V _{CE} = 500 V V _{CE} = 500 V T _C = 125°C			1 5	mA mA
V _{(BR)EBO}	Emitter-base breakdown voltage (I _C = 0)	I _E = 10 mA For NPN: For PNP:	12 5		18 10	V V
V _{CEO(sus)} ⁽¹⁾	Collector-emitter sustaining voltage (I _B = 0)	I _C = 5 mA	400			V
V _{CE(sat)} ⁽¹⁾	Collector-emitter saturation voltage	I _C = 0.5 A I _B = 0.1 A			0.5	V
		I _C = 0.35 A I _B = 50 mA			1	V
V _{BE(sat)} ⁽¹⁾	Base-emitter saturation voltage	I _C = 0.5 A I _B = 0.1 A			1	V
h _{FE} ⁽¹⁾	DC current gain	I _C = 10 mA V _{CE} = 5 V	10		34	
		I _C = 0.35A V _{CE} = 5 V	16			
		I _C = 1 A V _{CE} = 5 V	4			
t _r t _s t _f	Resistive load Rise time Storage time Fall time	I _C = 0.35 A V _{CC} = 125 V		100		ns
		I _{B1} = 70 mA I _{B2} = -70 mA		2.2		µs
		t _p ≥ 25 µs		0.2		µs
t _s t _f	Inductive load Storage time Fall time	I _C = 0.5 A I _{B1} = 0.1 A		450		ns
		V _{BE(off)} = -5 V V _{clamp} = 300 V L = 10 mH		80		ns

1. Pulse test: pulse duration ≤ 300 µs, duty cycle ≤ 2 %.

Note: For PNP types voltage and current values are negative

2.1 Electrical characteristics (curves)

Figure 2. DC current gain NPN ($V_{CE} = 5\text{ V}$)

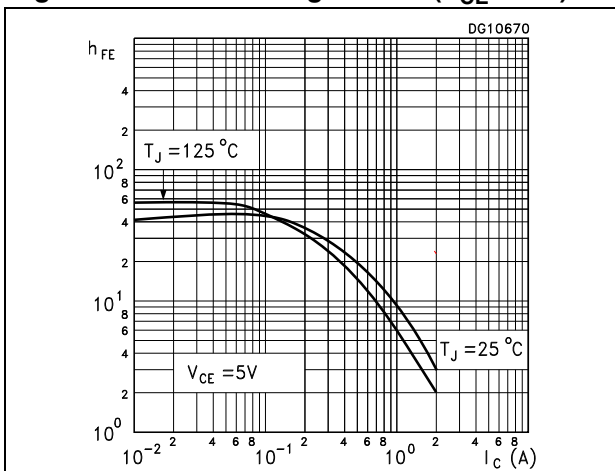


Figure 3. DC current gain PNP ($V_{CE} = -5\text{ V}$)

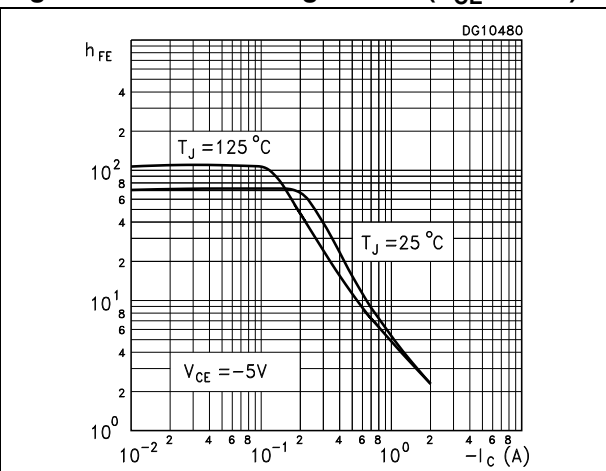


Figure 4. DC current gain NPN ($V_{CE} = 1\text{ V}$)

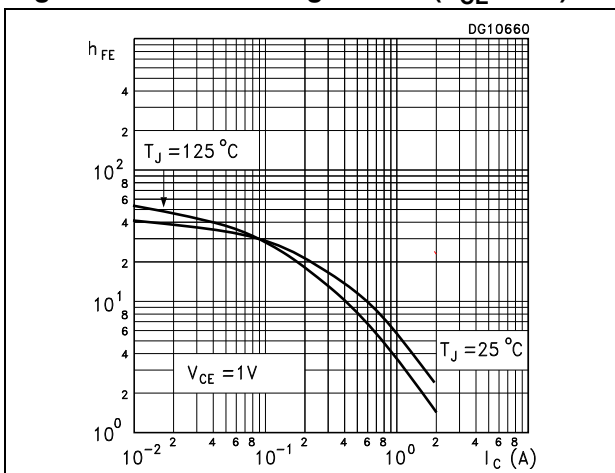


Figure 5. DC current gain PNP ($V_{CE} = -1\text{ V}$)

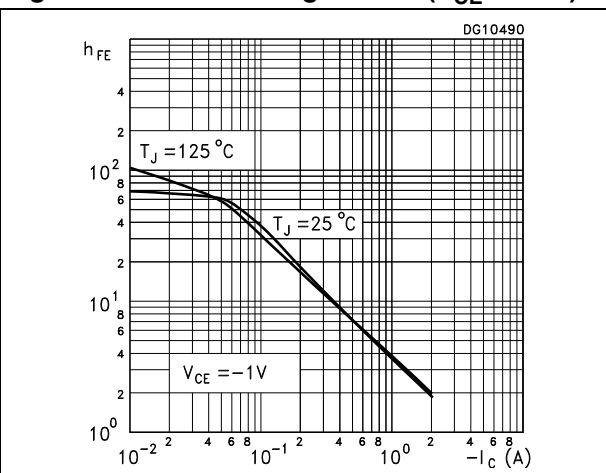


Figure 6. Derating curve

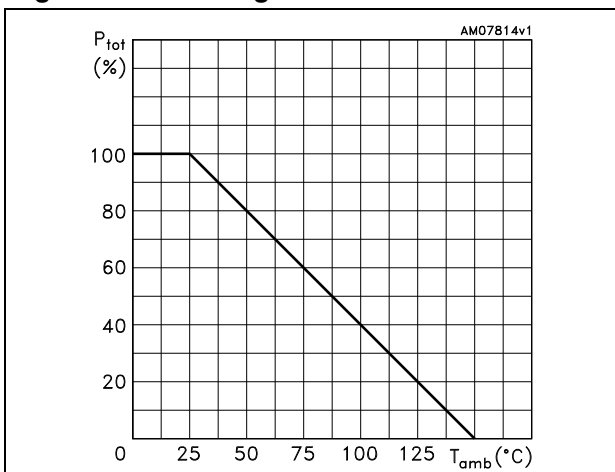


Figure 7. Collector emitter saturation voltage NPN

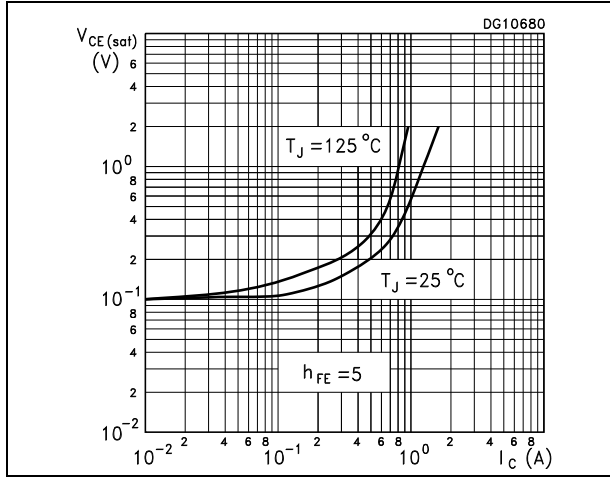


Figure 8. Collector emitter saturation voltage PNP

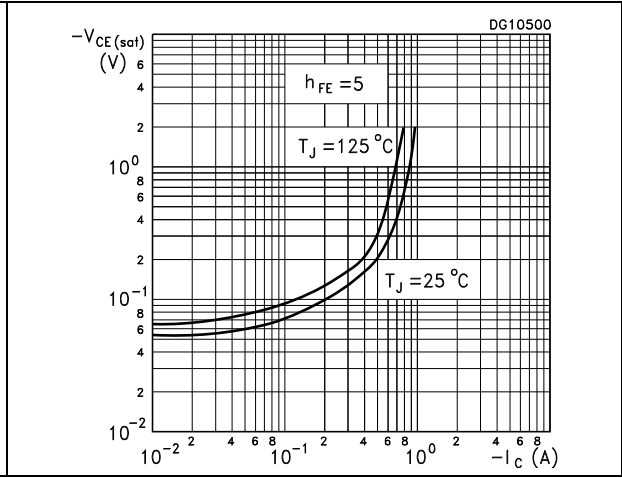


Figure 9. Base emitter saturation voltage NPN

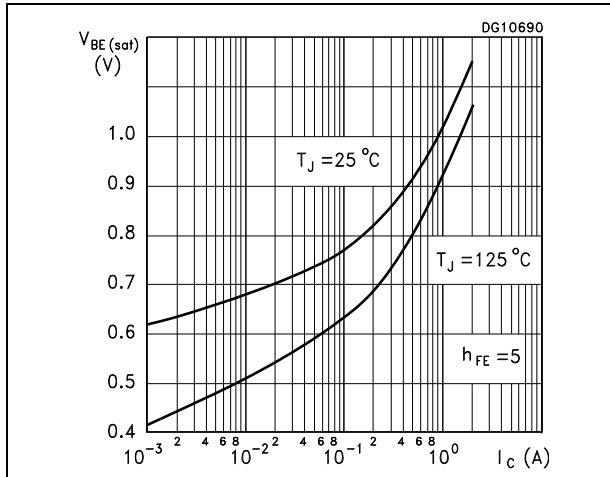


Figure 10. Base emitter saturation voltage PNP

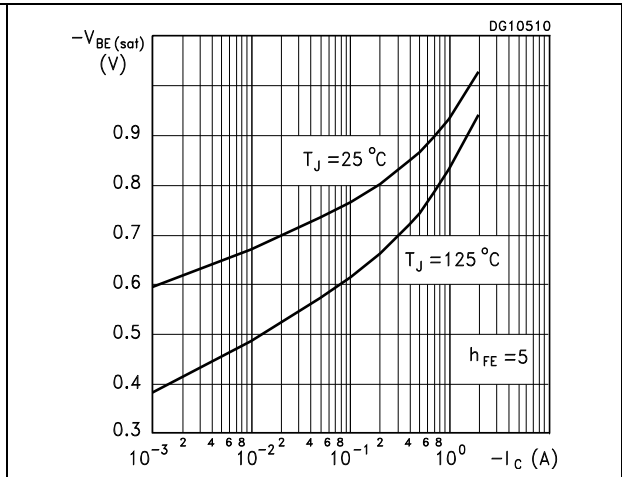


Figure 11. Resistive load fall time NPN

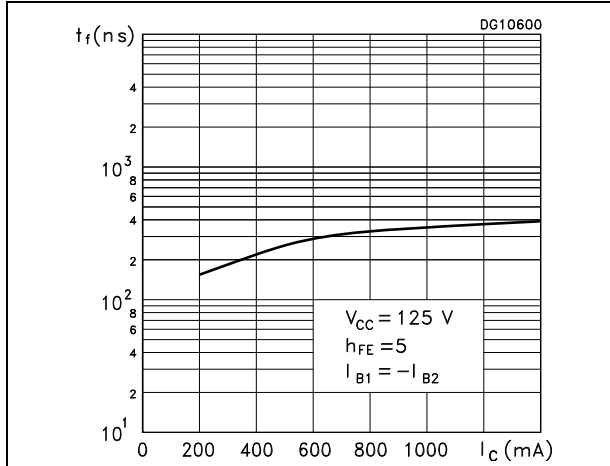


Figure 12. Resistive load fall time PNP

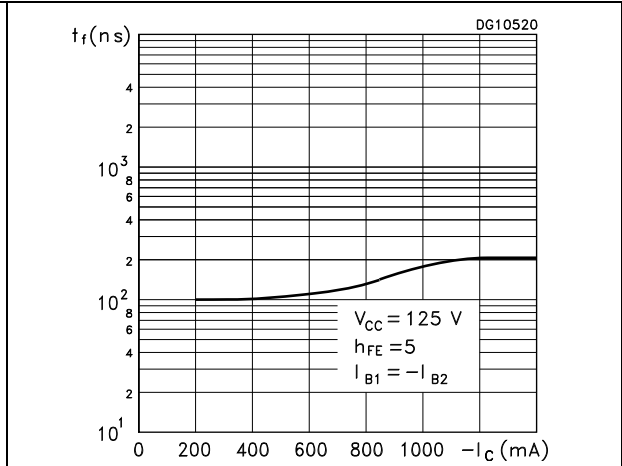


Figure 13. Resistive load storage time NPN

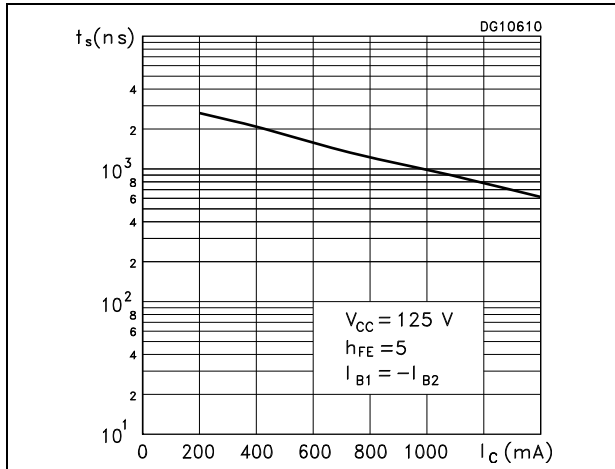


Figure 14. Resistive load storage time PNP

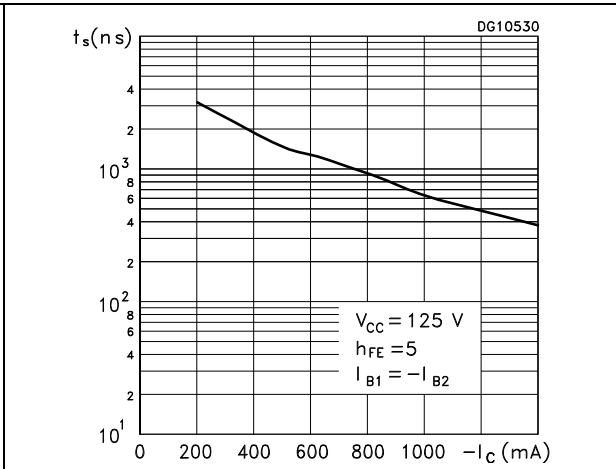


Figure 15. Inductive load fall time NPN

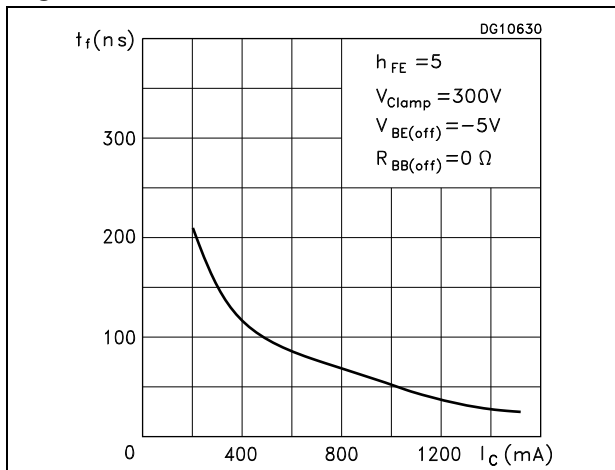


Figure 16. Inductive load fall time PNP

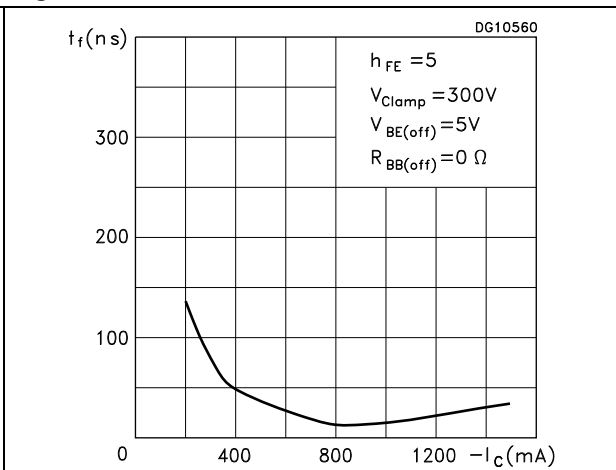


Figure 17. Inductive load storage time NPN

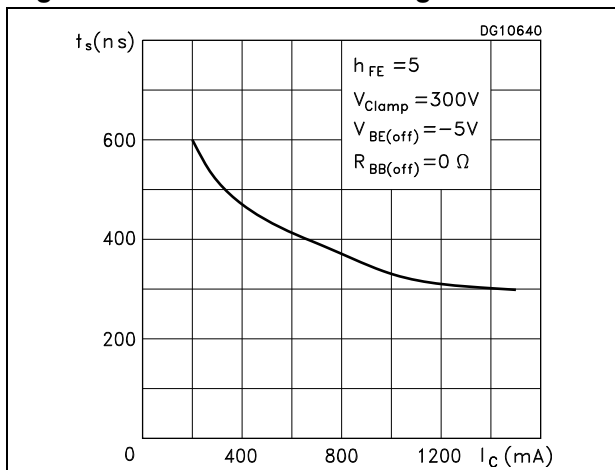


Figure 18. Inductive load storage time PNP

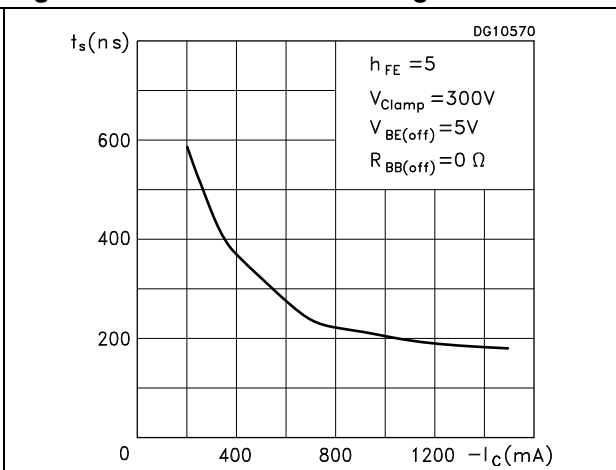


Figure 19. Reverse biased SOA (NPN)

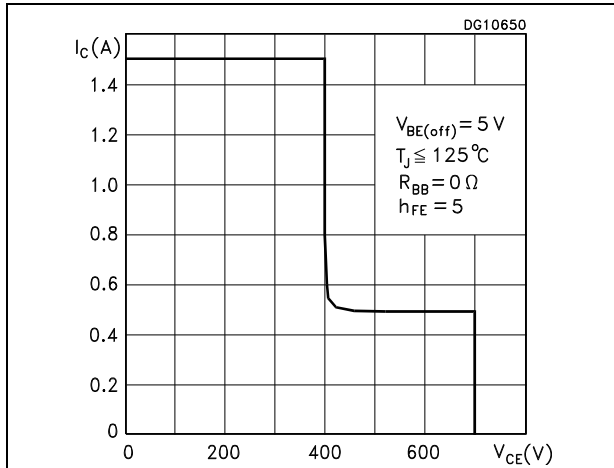
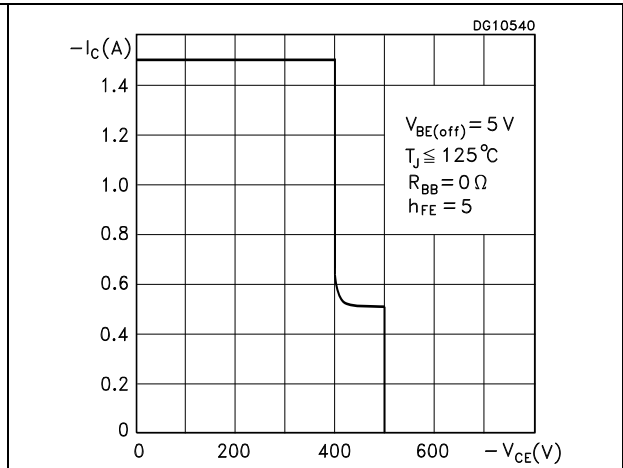


Figure 20. Reverse biased SOA (PNP)



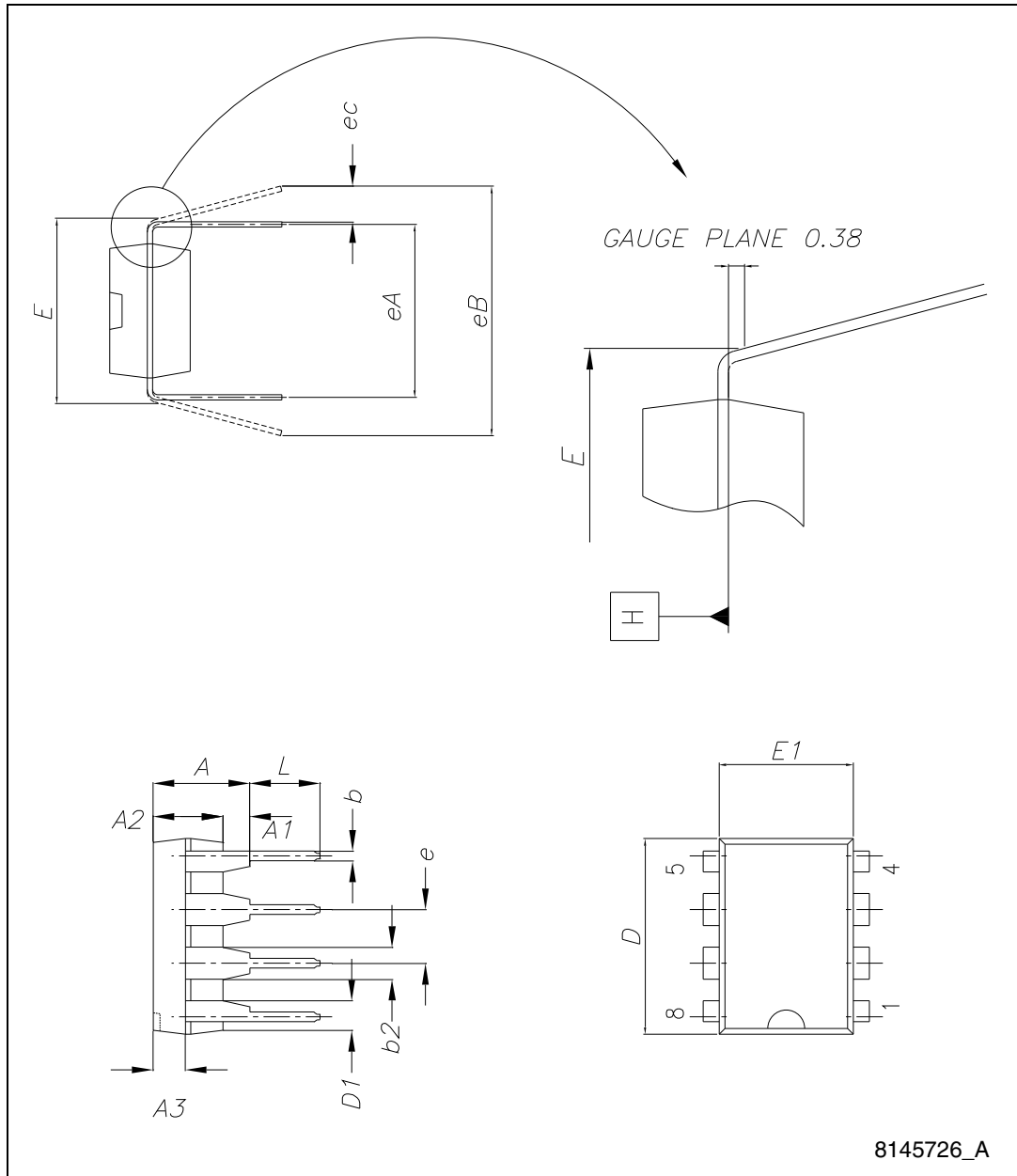
3 Package mechanical data

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Table 5. DIP-8 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			4.80
A1	0.50		
A2	3.10		3.50
A3	1.40		1.60
b	0.38		0.55
b1	0.38		0.51
b2	1.47		1.57
b3	0.89		1.09
c	0.21		0.35
c1	0.20		0.30
D	9.10		9.30
D1	0.13		
E	7.62		8.25
E1	6.25		6.45
e		2.54	
eA		7.62	
eB	7.62		10.90
eC	0		1.52
L	2.92		3.81

Figure 21. Drawing dimension DIP-8



4 Revision history

Table 6. Document revision history

Date	Revision	Changes
20-Jun-2008	1	Initial release
26-May-2009	2	Updated mechanical data Table 5 on page 8 and Figure 21 on page 9 .
29-Jun-2010	3	Modified: Table 2 and Table 3 on page 2 , added Section 2.1: Electrical characteristics (curves) .
05-Oct-2012	4	Table 2 and Table 3 on page 2 have been modified.

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