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STDP4320
DisplayPort 1.2a splitter

Datasheet

Rev A

MegaChips

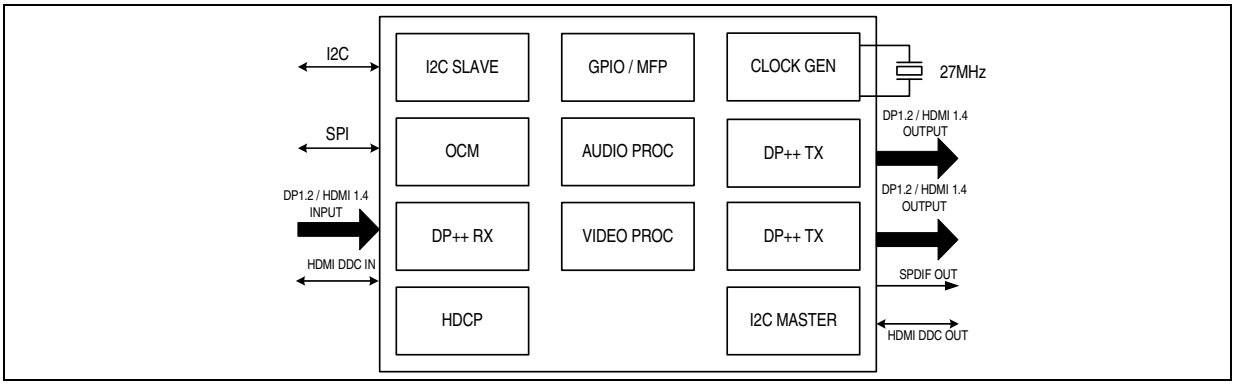
MegaChips' Proprietary Information

Features

- DisplayPort® dual mode receiver
  - DP 1.2a compliant
  - Link rate HBR2/HBR/RBR
  - SST or MST (up to eight streams)
  - 1, 2, or 4 lanes
  - AUX CH 1 Mbps
  - HPD out
  - HDMI/DVI operation (3.2 Gbps link rate)
  - Functions as eDP and MyDP receiver
- DisplayPort dual mode transmitters
  - Two transmitter ports
  - DP 1.2a compliant
  - Link rate HBR2/HBR/RBR
  - SST or MST (up to eight streams)
  - 1, 2, or 4 lanes
  - AUX CH 1 Mbps
  - HPD in
  - HDMI/DVI operation (3.2 Gbps link rate) with external level translator
  - Functions as eDP transmitter
- SPDIF audio output
  - Two SPDIF port pins
  - 192 kHz/24 bits
  - Compressed/LPCM
- Conversion from DP SST to TMDS format and vice versa
- HDCP repeater with embedded keys
- AUX to I2C bridge for EDID/MCCS pass through
  - Maps on DDC ports
- Device configuration options
  - SPI Flash
  - I2C host interface
- Deep color support
  - RGB/YCC (4:4:4) – 16-bit color
  - YCC (4:2:2) – 16-bit color
- Spread spectrum on DisplayPort interface for EMI reduction
- Bandwidth
  - Video resolution up to 4K2K @ 60 Hz
  - Audio 7.1 Ch up to 192 kHz sample rate
- Low power operation
  - Standby 30 mW
- Package
  - 172 LFBGA (12 x 12 mm)
- Power supply voltages
  - 3.3 V I/O; 1.2 V core

Applications

- Audio-video router for PC/notebooks, docking stations, hub, 4K2K TVs, daisy chain monitors, digital signage



Contents

List of Tables

List of Figures

1. Description

The STDP4320 is a high-speed DisplayPort dual mode splitter IC targeted for audio-video de-multiplexing and routing in applications such as notebooks, docking stations, video hub, 4K2K TVs, daisy chainable monitors, digital signage, etc. It consists of one dual mode input port and two dual mode output ports configurable as either DisplayPort or HDMI/DVI. STDP4320 is a VESA DP Standard Ver. 1.2a compliant device that supports advanced features such as MST, HBR2, 3D formats and GTC assist. Designs based on STDP4320 have the flexibility to offer either DP or HDMI/DVI connectors on its end product to interface with legacy and new generation video sources and sinks. In addition, STDP4320-based products with a DisplayPort output connector are DP++ compliant and work with any HDMI or single link DVI sink through a passive level translator (dongle).

The STDP4320 uses MegaChips' latest generation DisplayPort dual mode receiver and transmitter technology that supports both DisplayPort and TMDS signal formats. This device receives MST format up to eight audio-video streams, which can be further routed on either of the two outputs in any combination of eight streams depending on the capability of downstream sinks. This device can also replicate the incoming video streams on both output ports simultaneously, thus allowing cloning on two downstream sinks. For example, a 4K2K 60 Hz video input is replicated on two output ports simultaneously. The DisplayPort receiver and transmitters support HBR2 speed, a data rate of 5.4 Gbps per lane with a total bandwidth of 21.6 Gbps link rate. In HDMI mode, this device supports link rates up to 3.2 Gbps corresponding to a pixel rate of 300 MHz, adequate for supporting video resolution up to FHD 120 Hz with all 3D formats. The device is also capable of delivering deep color video up to 16-bits per color. The STDP4320 allows audio transport from the source to the desired audio rendering devices over the video output port or through an SPDIF port.

The STDP4320 supports RGB and YCbCr colorimetric formats with color depth of 16, 12, 10, and 8 bits. The STDP4320 features the HDCP 1.3 content protection scheme with embedded keys for secure transmission of protected audio-video content. It also operates as an HDCP repeater for the downstream sinks.

The DDC ports in the STDP4320 allow the upstream source to access EDID and transfer MCCS commands to downstream sinks when the physical ports are either HDMI or DVI type. If both the upstream source and downstream sinks are DP type, I2C transactions take place over the AUX CH. If one of them is a DP type and the other is either a HDMI or DVI type, STDP4320 converts the I2C over AUX message protocol to I2C commands and sends it on the DDC port.

The device has an on-chip microcontroller with SPI, UART, and I2C interface. The STDP4320 uses an external SPI Flash ROM for storing device configuration firmware. It has an I2C slave port for external host communication. Other system interface signals include general-purpose IO for source, sink communication, detection, monitoring, etc. When the downstream sink is disconnected, STDP4320 automatically turns off the inactive port for power saving purposes.

2. Application overview

Figure 1. STDP4320 in video hub application

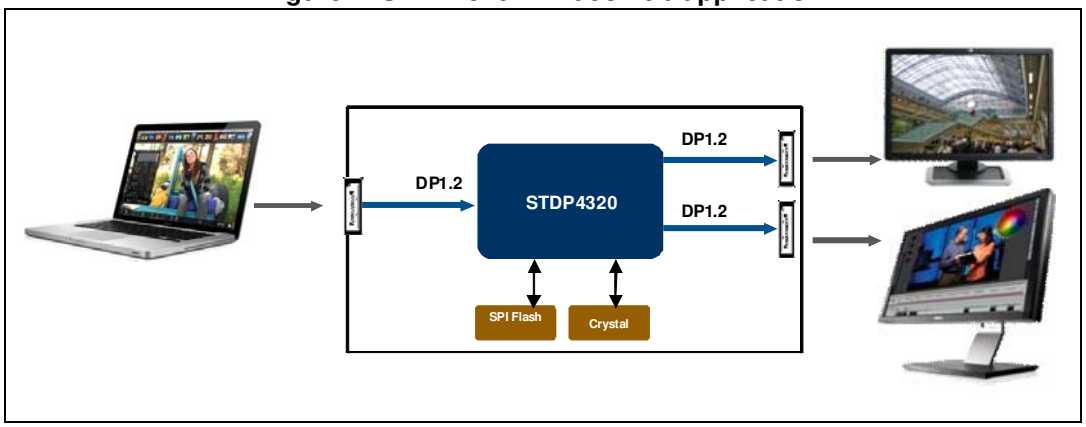
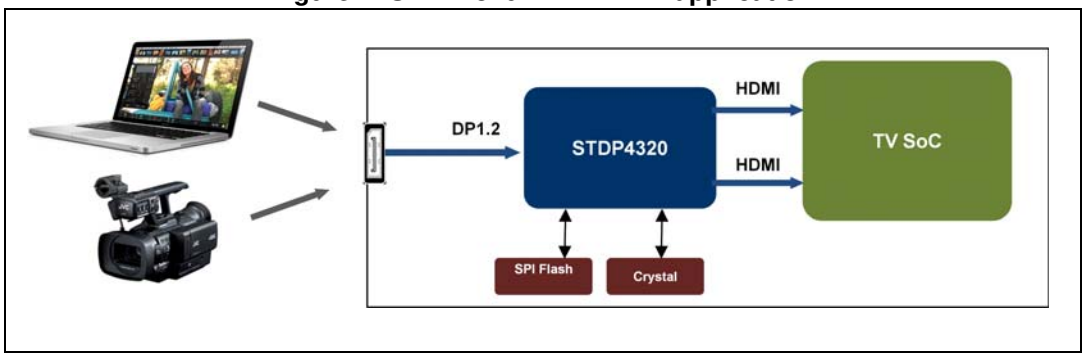


Figure 2. STDP4320 in 4K2K TV application



3. Feature attributes

3.1 Input interface

- Single DP++ interface featuring
  - DisplayPort Ver. 1.2a compliant receiver; supports eDP and MyDP
  - HDMI 1.4 compliant receiver
- Main link configuration
  - SST or MST (up to eight streams)
  - HBR2/HBR/RBR link rate
  - 1, 2, or 4 lanes
- AUX CH: 1 Mbps Manchester transaction format
- HPD: IRQ_HPD assertion
- Video: EDID 1.4 and CEA861 video timing and formats from 24 to 48 bits/pixel in RGB, YCC422, or YCC444 colorimetry
- Audio: DisplayPort 1.2a standard info frame packets and IEC60958/61937 type audio stream packets ranging from 16 to 24 bits/sample, 32 to 192 kHz sample rates
- HDMI link rate: 3.2 Gbps/data pair max

3.2 Output interface

- Two DP++ interfaces featuring
  - AC coupled DisplayPort Ver. 1.2a compliant transmitter: supports eDP
  - AC coupled HDMI 1.4 transmitter
- DP main link configuration
  - SST or MST (up to eight streams)
  - HBR2/HBR/RBR link rate
  - 1, 2, or 4 lanes
- AUX CH: Manchester transaction format
- HPD: IRQ_HPD assertion
- Video: EDID 1.4 and CEA861 video timing and formats from 24 to 48 bits/pixel in RGB, YCC422, or YCC444 colorimetry
- Audio: DisplayPort 1.2a standard info frame packets and IEC60958/61937 type audio stream packets ranging from 16 to 24 bits/sample, 32 to 192 kHz sample rates
- HDMI link rate: 3.2 Gbps/data pair max

3.3 Supported video timings

- 4K2K 60 Hz: 24 bits/pixel in DP 1.2a configuration
- 1920 x 1080 (FHD) 240 Hz, 24 bits/pixel
- All 3D formats defined in DP 1.2a and HDMI 1.4 standards
- All standard CEA861 timing formats

3.4 Supported audio timings

- All audio formats as specified in DP 1.2a and HDMI 1.4 standards
- SPDIF; 2-Ch LPCM, AC3, DTS, bit depth up to 24 bits, sample rate up to 192 kHz (applicable in DP SST/HDMI output use case)

3.5 Control channel interfaces

- AUX CH, DDC, I2C host interface, and UART (UART for test/debug purposes only)

3.6 HDCP 1.3 support

- Key sets for DP/HDMI RX and DP/HDMI TX integrated in one-time programmable ROM (OTP)
- Standalone HDCP repeater capability

3.7 Package

- 172 LFBGA (12 x 12 mm), 0.8 ball pitch

3.8 Power supply voltages

- 3.3 V I/O; 1.2 V core

3.9 ESD

- 2 KV HBM, 450 V CDM

4. BGA footprint and pin lists

4.1 Ball grid array diagram

The ball grid array (BGA) diagrams give the allocation of pins to the package, shown from the top looking down using the PCB footprint.

The STDP4320 is available in a 172-pin LFBGA package.

White = no ball at this location

n/c = no connect: ball present, but must not be connected

Figure 3. STDP4320 BGA diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	RX0_LN2_N			RX0_LN0_P	RX0_AUX_P	RX0_AUX_N	n/c	n/c	n/c			n/c	VSS	A
B	RX0_LN3_P	RX0_LN2_P			RX0_LN0_N	VSS	VSS	VSS	VSS	n/c			n/c	n/c	B
C	RX0_LN3_N	AVDD33_RX	RX0_LN1_N	RX0_LN1_P	AVDD12_RX	AVDD12_RX	AVDD33_RX	AVDD33_RX	AVDD12_RX	AVDD12_RX	n/c	n/c	AVDD33_RX	n/c	C
D	TX1_HPD	TEST	VSS	VSS	VSS	RX0_REXT	VSS	VSS	n/c	VSS	VSS	VSS	HDMI_TX0_DDC_SCL	HDMI_TX0_DDC_SDA	D
E	n/c	SPDIF_OUT0	HDMI_CEC	TX0_HPD	DVDD12					DVDD12	HDMI_TX1_DDC_SDA	GPIO8	GPIO6	HDMI_TX1_DDC_SCL	E
F	MASTER1_IRQ_IN	GPO	SPDIF_OUT1	RX0_HPD	DVDD12	VSS	VSS	VSS	VSS	DVDD12	GPIO9	GPIO10	GPIO11	GPIO7	F
G	MASTER2_IRQ_IN	MASTER3_IRQ_IN	GPIO13	MASTER0_IRQ_IN	DVDD12	VSS	VSS	VSS	VSS	DVDD12	MASTER2_I2C_SDA	MASTER2_I2C_SCL	MASTER0_I2C_SDA	MASTER0_I2C_SCL	G
H	GPIO12	HOST_IRQ_OUT	SPI_CLK	UART_TX	DVDD12	VSS	VSS	VSS	VSS	DVDD12	HDMI_RX0_DDC_SCL	RESET_N	MASTER1_I2C_SDA	MASTER1_I2C_SCL	H
J	SPI_DI	UART_RX	SPI_CSN	GPIO2	DVDD33	VSS	VSS	VSS	VSS	DVDD33	n/c	HOST_I2C_SCL	MASTER3_I2C_SCL	MASTER3_I2C_SDA	J
K	TCLK_3V3_OUT	SPI_DO	GPIO0	GPIO1	DVDD25_SM					GPIO5	n/c	HDMI_RX0_DDC_SDA	AVDD12_PLL	HOST_I2C_SDA	K
L	TCLK_1V2_OUT	TX0_REXT	VSS	VSS	GPIO3	VSS	VSS	VSS	VSS	GPIO4	VSS	VSS	AVDD12_OSC1	AVDD33_RCOSC	L
M	TX0_AUX_N	AVDD12_TX0	TX0_LN2_N	TX0_LN2_P	AVDD12_TX0	AVDD12_OSC0	VSS	VSS	TX1_REXT	AVDD12_TX1	TX1_LN2_N	TX1_LN2_P	AVDD33_TX1	TX1_LN0_P	M
N	TX0_AUX_P	TX0_LN3_P			TX0_LN1_N	AVDD33_TX0	TCLK	XTAL	AVDD12_TX1	TX1_LN3_P			TX1_LN1_N	TX1_LN0_N	N
P	VSS	TX0_LN3_N			TX0_LN1_P	TX0_LN0_N	TX0_LN0_P	TX1_AUX_N	TX1_AUX_P	TX1_LN3_N			TX1_LN1_P	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

4.2 Full pin list sorted by pin number

Table 1. Pin list

Pin number	Net name
A1	VSS
A2	RX0_LN2_N
A5	RX0_LN0_P
A6	RX0_AUX_P
A7	RX0_AUX_N
A8, A9, A10, A13	n/c
A14	VSS
B1	RX0_LN3_P
B2	RX0_LN2_P
B5	RX0_LN0_N
B6, B7, B8, B9	VSS
B10, B13, B14	n/c
C1	RX0_LN3_N
C2	AVDD33_RX
C3	RX0_LN1_N
C4	RX0_LN1_P
C5, C6	AVDD12_RX
C7, C8	AVDD33_RX
C9, C10	AVDD12_RX
C11, C12	n/c
C13	AVDD33_RX
C14	n/c
D1	TX1_HPD
D2	TEST
D3, D4, D5	VSS
D6	RX0_REXT
D7, D8	VSS
D9	n/c
D10, D11, D12	VSS
D13	HDMI_TX0_DDC_SCL
D14	HDMI_TX0_DDC_SDA
E1	n/c
E2	SPDIF_OUT0

Table 1. Pin list (continued)

Pin number	Net name
E3	HDMI_CEC
E4	TX0_HPD
E5	DVDD12
E10	DVDD12
E11	HDMI_TX1_DDC_SDA
E12	GPIO8
E13	GPIO6
E14	HDMI_TX1_DDC_SCL
F1	MASTER1_IRQ_IN
F2	GPO
F3	SPDIF_OUT1
F4	RX0_HPD
F5	DVDD12
F6, F7, F8, F9	VSS
F10	DVDD12
F11	GPIO9
F12	GPIO10
F13	GPIO11
F14	GPIO7
G1	MASTER2_IRQ_IN
G2	MASTER3_IRQ_IN
G3	GPIO13/TX1_CONFIG2
G4	MASTER0_IRQ_IN
G5	DVDD12
G6, G7, G8, G9	VSS
G10	DVDD12
G11	MASTER2_I2C_SDA
G12	MASTER2_I2C_SCL
G13	MASTER0_I2C_SDA
G14	MASTER0_I2C_SCL
H1	GPIO12/TX1_CONFIG1
H2	HOST_IRQ_OUT
H3	SPI_CLK
H4	UART_TX
H5	DVDD12

Table 1. Pin list (continued)

Pin number	Net name
H6, H7, H8, H9	VSS
H10	DVDD12
H11	HDMI_RX0_DDC_SCL
H12	RESETn
H13	MASTER1_I2C_SDA
H14	MASTER1_I2C_SCL
J1	SPI_DI
J2	UART_RX
J3	SPI_CSN
J4	GPIO2
J5	DVDD33
J6, J7, J8, J9	VSS
J10	DVDD33
J11	n/c
J12	HOST_I2C_SCL
J13	MASTER3_I2C_SCL
J14	MASTER3_I2C_SDA
K1	TCLK_3V3_OUT
K2	SPI_DO
K3	GPIO0/TX0_CONFIG1
K4	GPIO1/TX0_CONFIG2
K5	DVDD25_SM
K10	GPIO5
K11	n/c
K12	HDMI_RX0_DDC_SDA
K13	AVDD12_PLL
K14	HOST_I2C_SDA
L1	TCLK_1V2_OUT
L2	TX0_REXT
L3, L4	VSS
L5	GPIO3/RX0_CABLE_DET0
L6, L7, L8, L9	VSS
L10	GPIO4/RX0_CABLE_DET1
L11, L12	VSS
L13	AVDD12_OSC1

Table 1. Pin list (continued)

Pin number	Net name
L14	AVDD33_RCOSC
M1	TX0_AUX_N
M2	AVDD12_TX0
M3	TX0_LN2_N
M4	TX0_LN2_P
M5	AVDD12_TX0
M6	AVDD12_OSC0
M7, M8	VSS
M9	TX1_REXT
M10	AVDD12_TX1
M11	TX1_LN2_N
M12	TX1_LN2_P
M13	AVDD33_TX1
M14	TX1_LN0_P
N1	TX0_AUX_P
N2	TX0_LN3_P
N5	TX0_LN1_N
N6	AVDD33_TX0
N7	TCLK
N8	XTAL
N9	AVDD12_TX1
N10	TX1_LN3_P
N13	TX1_LN1_N
N14	TX1_LN0_N
P1	VSS
P2	TX0_LN3_N
P5	TX0_LN1_P
P6	TX0_LN0_N
P7	TX0_LN0_P
P8	TX1_AUX_N
P9	TX1_AUX_P
P10	TX1_LN3_N
P13	TX1_LN1_P
P14	VSS

5. Connections

5.1 Pin list

I/O Legend: I = Input; O = Output; P = Power; G = Ground; IO = Bi-direction; AI = Analog input; AO = Analog output; AIO = Analog I/O; TRI = Tristate; TOL = Tolerance; PD = Internal 50K pulldown; PU = Internal 50K pull-up; OPENDR = Open drain output

Note: Some pins can have multiple functionalities, which are configured under register control. The alternate functionality for each pin is listed in the Description column.

Table 2. DisplayPort receiver pins

Pin	Assignment	I/O	Description	Reset state
D6	RX0_REXT	AIO, 3V3 TOL	Connect to External 249 Ohm Resistor to VDD33	NA
A5	RX0_LN0_P	AIO, 3V3 TOL	DUAL MODE RX HDMI CLOCKP OR DP RX_LN0P.	TRISTATE
B5	RX0_LN0_N	AIO, 3V3 TOL	DUAL MODE RX HDMI CLOCKN OR DP RX_LN0N.	TRISTATE
C4	RX0_LN1_P	AIO, 3V3 TOL	DUAL MODE RX HDMI RX0P OR DP RX_LN1P.	TRISTATE
C3	RX0_LN1_N	AIO, 3V3 TOL	DUAL MODE RX HDMI RX0N OR DP RX_LN1N.	TRISTATE
B2	RX0_LN2_P	AIO, 3V3 TOL	DUAL MODE RX HDMI RX1P OR DP RX_LN2P.	TRISTATE
A2	RX0_LN2_N	AIO, 3V3 TOL	DUAL MODE RX HDMI RX1N OR DP RX_LN2N.	TRISTATE
B1	RX0_LN3_P	AIO, 3V3 TOL	DUAL MODE RX HDMI RX2P OR DP RX_LN3P.	TRISTATE
C1	RX0_LN3_N	AIO, 3V3 TOL	DUAL MODE RX HDMI RX2N OR DP RX_LN3N.	TRISTATE
A6	RX0_AUX_P	AIO, 1V2 TOL	DUAL MODE RX DP RX_AUXP. AC Couple 0.1uF. Use 20 Ohm damping resistor in series and 1M Ohm pull up to 3.3 V before cap.	TRISTATE
A7	RX0_AUX_N	AIO, 1V2 TOL	DUAL MODE RX DP RX_AUXN. AC Couple 0.1uF. Use 20 Ohm damping resistor in series and 1M Ohm pull down to GND before cap.	TRISTATE

Note: The default DP and HDMI input signals mapping match the standard DP and HDMI connector pin mapping. However, lane swapping and polarity swapping are possible through software configuration.

Table 3. System function pins

Pin	Assignment	I/O	Description	Reset state
D2	TEST	I, 3V3 TOL, INT PD	Connect to GND	INPUT, Internal PD
N7	TCLK	AIO, 1V2 TOL	Connect to 27 MHz crystal oscillator with 22 pF to 1.2 V.	NA
N8	XTAL			
K1	TCLK_3V3_OUT	IO, 3V3 TOL	TCLK output, Tristate 3.3 V pad	TRISTATE
L1	TCLK_1V2_OUT	IO, 1V2 TOL	TCLK output, Tristate 1.2 V pad	TRISTATE
H12	RESETn	AIO, 3V3 TOL	Use external 3K ohm resistor to 3.3 V	TRISTATE, INPUT
J3	SPI_CSN	IO, 3V3 TOL, TRI, INT PU	To SPI chip select. Also see *Table 8: Bootstrap configuration*.	TRISTATE, Internal PU
K2	SPI_DO	IO, 3V3 TOL, TRI, INT PD	To SPI data out. Also see *Table 8: Bootstrap configuration*.	TRISTATE, Internal PD
J1	SPI_DI	I, 3V3 TOL, INT PD	From SPI data in.	INPUT with Internal PD
H3	SPI_CLK	IO, 3V3 TOL, TRI, INT PD	To SPI clock. Also see *Table 8: Bootstrap configuration*.	TRISTATE, Internal PD

Table 4. Multi-function pins

Pin	Assignment	I/O	Description	Reset state
E3	HDMI_CEC	IO, 3.3 TOL, TRI	HDMI CEC not supported in the current silicon rev. Connect this pin to external pull-up DVDD3V3.	TRISTATE
F4	RX0_HPD		To the upstream HPD signal pin on the DP connector. 100K res to GND.	TRISTATE
L5	GPIO3/ RX0_CABLE_DET0		Cable detect1 for DisplayPort connector	TRISTATE
L10	GPIO4/ RX0_CABLE_DET1		Cable detect2 for DisplayPort connector	TRISTATE
K12	HDMI_RX0_DDC_SDA		DDC SDA for upstream HDMI port0. Use external pull up 4.7 K to 3.3 V when used. Else leave as NC.	TRISTATE
H11	HDMI_RX0_DDC_SCL		DDC SCL for upstream HDMI port0. Use external pull up 4.7 K to 3.3 V when used. Else leave as NC.	TRISTATE
E2	SPDIF_OUT0	IO, 3.3 TOL, TRI, INT PU	To external buffer for SPDIF output [Audio corresponding to video on Port0]	TRISTATE, Internal PU
F3	SPDIF_OUT1		To external buffer for SPDIF output [Audio corresponding to video on Port1]	TRISTATE, Internal PU

Table 4. Multi-function pins

Pin	Assignment	I/O	Description	Reset state
E4	TX0_HPD	IO, 3.3 TOL, TRI	HPD in for Downstream DP/HDMI port0	TRISTATE
J4	GPIO2		General Purpose input/output, Tristate 3.3 V pad	TRISTATE
D14	HDMI_TX0_DDC_SDA		DDC SDA for downstream HDMI port0. Use external pull up 4.7 K to 3.3 V when used. Else leave as NC.	TRISTATE
D13	HDMI_TX0_DDC_SCL		DDC SCL for downstream HDMI port0. Use external pull up 4.7 K to 3.3 V when used. Else leave as NC.	TRISTATE
K3	GPIO0/TX0_CONFIG1		Config1 input for Downstream DP port0 or GPIO	TRISTATE
K4	GPIO1/TX0_CONFIG2		Config2 input for Downstream DP port0 or GPIO	TRISTATE
D1	TX1_HPD		HPD in for Downstream DP/HDMI port1	TRISTATE
K10	GPIO5		General Purpose input/output, Tristate 3.3 V pad	TRISTATE
E11	HDMI_TX1_DDC_SDA	IO, 3.3 TOL, TRI	DDC SDA for downstream HDMI port1. Use external pull up 4.7 K to 3.3 V when used. Else leave as NC.	TRISTATE
E14	HDMI_TX1_DDC_SCL		DDC SCL for downstream HDMI port1 . Use external pull up 4.7 K to 3.3 V when used. Else leave as NC.	TRISTATE
H1	GPIO12/ TX1_CONFIG1		Config1 input for Downstream DP port1 or GPIO	TRISTATE
G3	GPIO13/ TX1_CONFIG2		Config2 input for Downstream DP port1 or GPIO	TRISTATE
H4	UART_TX	IO, 3.3 TOL, TRI, INT PU	To debug port UART_TX. Also see *Table 8: Bootstrap configuration*.	TRI, Internal PU
J2	UART_RX	IO, 3.3 TOL, TRI	To debug port UART_RX	TRISTATE
G14	MASTER0_I2C_SCL		Master I2C SCL Port0. Connect to I2C Slave with external Pull Up	TRISTATE
G13	MASTER0_I2C_SDA		Master I2C SDA Port0. Connect to I2C Slave with external Pull Up	TRISTATE
G4	MASTER0_IRQ_IN	IO, 3.3 TOL, TRI, INT PD	Master I2C Port0 interrupt input. Connect to I2C Slave interrupt out	TRISTATE, Internal PD
H14	MASTER1_I2C_SCL	IO, 3.3 TOL, TRI	Master I2C SCL Port1. Connect to I2C Slave with external Pull Up	TRISTATE
H13	MASTER1_I2C_SDA		Master I2C SDA Port1. Connect to I2C Slave with external Pull Up	TRISTATE
F1	MASTER1_IRQ_IN	IO, 3.3 TOL, TRI, INT PD	Master I2C Port01interrupt input. Connect to I2C Slave interrupt out	TRISTATE, Internal PD
G12	MASTER2_I2C_SCL	IO, 3.3 TOL, TRI	Master I2C SCL Port2. Connect to I2C Slave with external Pull Up	TRISTATE
G11	MASTER2_I2C_SDA		Master I2C SDA Port2. Connect to I2C Slave with external Pull Up	TRISTATE

Table 4. Multi-function pins

Pin	Assignment	I/O	Description	Reset state
G1	MASTER2_IRQ_IN	IO, 3.3 TOL, TRI, INT PD	Master I2C Port2 interrupt input. Connect to I2C Slave interrupt out	TRISTATE, Internal PD
J13	MASTER3_I2C_SCL	IO, 3.3 TOL, TRI	Master I2C SCL Port3. Connect to I2C Slave with external Pull Up	TRISTATE,
J14	MASTER3_I2C_SDA		Master I2C SDA Port3. Connect to I2C Slave with external Pull Up	TRISTATE,
G2	MASTER3_IRQ_IN	IO, 3.3 TOL, TRI, INT PD	Master I2C Port3 interrupt input. Connect to I2C Slave interrupt out	TRISTATE, Internal PD
J12	HOST_I2C_SCL	IO, 3.3 TOL, TRI	Slave I2C SCL. Connect to I2C Master with external Pull Up	TRISTATE
K14	HOST_I2C_SDA		Slave I2C SDA. Connect to I2C Master with external Pull Up	TRISTATE
H2	HOST_IRQ_OUT	IO, 3.3 TOL, TRI, INT PD	Interrupt out. Connect to interrupt in of Master	TRISTATE, Internal PD
E13	GPIO6	IO, 3.3 TOL, TRI	General purpose input/output	TRISTATE
F14	GPIO7	IO, 3.3 TOL, TRI		
E12	GPIO8	IO, 3.3 TOL, TRI		
F11	GPIO9	IO, 3.3 TOL, TRI		
F12	GPIO10	IO, 3.3 TOL, TRI		
F13	GPIO11	IO, 3.3 TOL, TRI		
F2	GPO	IO, 3.3 TOL, TRI, INT PD	General purpose input/output. See *Table 8: Bootstrap configuration*.	TRISTATE, Internal PD

Table 5. Transmitter pins

Pin	Assignment	I/O	Description	Reset state
L2	TX0_REXT	AI, 1V2 TOL	TX, EXTERNAL 249 Ohm RESISTOR TO VDD12	NA
N1	TX0_AUX_P	AIO, 1V2 TOL	DUAL MODE TX Port0 DP TX_AUXP. AC Couple to TX Connector. External 100K Resistor to GND.	TRISTATE
M1	TX0_AUX_N	AIO, 1V2 TOL	DUAL MODE TX Port0 DP TX_AUXN. AC Couple to TX Connector. External 100K Resistor to VDD33.	TRISTATE
N2	TX0_LN3_P	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TXCKP OR DP TX_LN3P. AC Couple to TX Connector.	TRISTATE
P2	TX0_LN3_N	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TXCKN OR DP TX_LN3N. AC Couple to TX Connector	TRISTATE
M4	TX0_LN2_P	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TX2P OR DP TX_LN2P. AC Couple to TX Connector	TRISTATE

Table 5. Transmitter pins

Pin	Assignment	I/O	Description	Reset state
M3	TX0_LN2_N	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TX2N OR DP TX_LN2N. AC Couple to TX Connector	TRISTATE
P5	TX0_LN1_P	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TX1P OR DP TX_LN1P. AC Couple to TX Connector	TRISTATE
N5	TX0_LN1_N	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TX1N OR DP TX_LN1N. AC Couple to TX Connector	TRISTATE
P7	TX0_LN0_P	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TX0P OR DP TX_LN1P. AC Couple to TX Connector	TRISTATE
P6	TX0_LN0_N	AO, 1V2 TOL	DUAL MODE TX Port0 HDMI TX0N OR DP TX_LN1N. AC Couple to TX Connector	TRISTATE
M9	TX1_REXT	AI, 1V2 TOL	TX, EXTERNAL 249 Ohm RESISTOR TO VDD12	NA
P9	TX1_AUX_P	AO, 1V2 TOL	DUAL MODE TX Port1 DP TX_AUXP. AC Couple to TX Connector. External 100K Resistor to GND.	TRISTATE
P8	TX1_AUX_N	AO, 1V2 TOL	DUAL MODE TX Port1 DP TX_AUXN. AC Couple to TX Connector. External 100K Resistor to VDD33.	TRISTATE
N10	TX1_LN3_P	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TXCKP OR DP TX_LN3P. AC Couple to TX Connector.	TRISTATE
P10	TX1_LN3_N	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TXCKN OR DP TX_LN3N. AC Couple to TX Connector	TRISTATE
M12	TX1_LN2_P	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TX2P OR DP TX_LN2P. AC Couple to TX Connector	TRISTATE
M11	TX1_LN2_N	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TX2N OR DP TX_LN2N. AC Couple to TX Connector	TRISTATE
P13	TX1_LN1_P	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TX1P OR DP TX_LN1N. AC Couple to TX Connector	TRISTATE
N13	TX1_LN1_N	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TX1N OR DP TX_LN1N. AC Couple to TX Connector	TRISTATE
M14	TX1_LN0_P	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TX0P OR DP TX_LN1P. AC Couple to TX Connector	TRISTATE
N14	TX1_LN0_N	AO, 1V2 TOL	DUAL MODE TX Port1 HDMI TX0N OR DP TX_LN1N. AC Couple to TX Connector	TRISTATE

Table 6. System power and ground

Pin	Assignment	Description
J5, J10	DVDD33	I/O VDD, 3.3V digital supply. De-couple using 100 nF.
E5, E10, F5, F10, G5, G10, H5, H10	DVDD12	Core VDD, 1.2V digital supply. De-couple using 100 nF.
L14	AVDD33_RCOSC	3.3V RC-oscillator analog supply. De-couple using 100 nF.
K13	AVDD12_PLL	1.2V analog PLL supply. De-couple using 10 uF and 100 nF.
C5, C6, C9, C10	AVDD12_RX	1.2V analog receiver supply. EMI filter rail and de-couple using 10 uF and 100 nF.

Table 6. System power and ground

Pin	Assignment	Description
C2, C7, C8, C13	AVDD33_RX	3.3V analog receiver supply. EMI filter rail and de-couple using 10 uF and 100 nF.
N6	AVDD33_TX0	3.3V analog transmitter supply. EMI filter rail and de-couple using 10 uF and 100 nF.
M13	AVDD33_TX1	3.3V analog transmitter supply. EMI filter rail and de-couple using 10 uF and 100 nF.
M2, M5	AVDD12_TX0	1.2V analog transmitter supply. EMI filter rail and de-couple using 10 uF and 100 nF.
M10, N9	AVDD12_TX1	1.2V analog transmitter supply. EMI filter rail and de-couple using 10 uF and 100 nF.
M6	AVDD12_OSC0	1.2V analog crystal oscillator supply. De-couple using 100 nF.
L13	AVDD12_OSC1	1.2V analog crystal oscillator supply. De-couple using 100 nF.
K5	DVDD25_SM	2.5V LDO supply. De-couple using 10 uF and 100 nF.
A1, A14, B6, B7, B8, B9, D3, D4, D5, D7, D8, D10, D11, D12, F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9, L3, L4, L6, L7, L8, L9, L11, L12, M7, M8, P1, P14	VSS	Common GND. Connect to GND plane

Table 7. Reserved pins

Pin	Assignment	Description
A8, A9, A10, A13, B10, B13, B14, C11, C12, C14, D9, E1, J11, K11	n/c	Reserved. Do not connect

5.2 Bootstrap configuration

DC levels on some of the pins are specified during de-asserting edge of power-on reset (RESETn goes high). The levels specified below must be adhered for normal function of the device.

Table 8. Bootstrap configuration

Bootstrap signal name	Internal PU/PD	Pin assignment	Function
Bootstrap_0	PULLUP	UART_TX (H4)	0: Reserved for ATE Test
			1: Normal Operation (Recommended)
Bootstrap_1	PULLDN	GPO (F2)	0: Crystal_OSC is enabled (Recommended)
			1: RC_OSC is enabled,

Bootstrap signal name	Internal PU/PD	Pin assignment	Function
Bootstrap_2	PULLDN	SPI_CLK (H3)	0: OCM boot up from internal ROM (Recommended)
			1: OCM boot up from external ROM
Bootstrap_3	PULLDN	SPI_DO (K2)	0: Reserved for Testing (Recommended)
			1: Reserved for Testing
Bootstrap_4	PULLUP	SPDIF_OUT0 (E2)	0: Select External OSC Operation
			1: Select Internal OSC Operation (Recommended)
Bootstrap_5	PULLUP	SPI_CSN (J3)	0: Debug Mode
			1: Normal Operation (Recommended)
Bootstrap_6	PULLUP	SPDIF_OUT1 (F3)	0: Software Bootstrap for I2C address selection
			1: Software Bootstrap for I2C address selection
Bootstrap_7	PULLDN	HOST_IRQ_OUT (H2)	0: Software Bootstrap for I2C address selection
			1: Software Bootstrap for I2C address selection

Note: When the pin corresponding to a specific bootstrap is left NC, it takes the value of the assigned by the internal PULLUP (Level 1) or PULLDN (Level0). The internal resistor used is around 50 k ohm. To select a non-default value on a bootstrap, an external PULLUP or PULLDN resistor is tied to the opposite direction that overcomes the internal PULLUP or PULLDN needs to be used.

6. Package specifications

Package type: 172 LFBGA (12 x 12 mm / ball pitch 0.8 mm)

6.1 Package drawing

Figure 4. Package drawing