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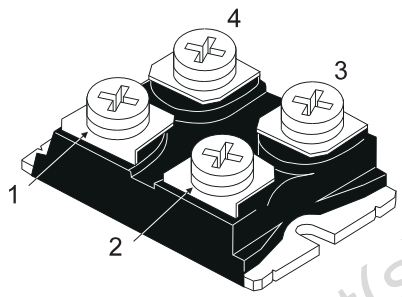
STE50DE100

Hybrid Emitter Switched Bipolar Transistor
ESBT® 1000 V - 50 A - 0.026 Ω

General features

$V_{CS(ON)}$	I_C	$R_{CS(ON)}$
1.3 V	50 A	0.026 Ω

- High voltage / high current Cascode configuration
- Ultra low equivalent on resistance
- Very fast-switch up to 150 kHz
- Ultra low C_{iss}
- Low dynamic $V_{CS(ON)}$



ISOTOP

Applications

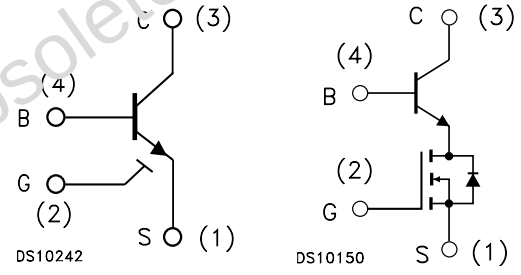
- Industrial converters
- Welding

Description

The STE50DE100 is manufactured in a hybrid structure, using dedicated high voltage Bipolar and low voltage MOSFET technologies, aimed to providing the best performance in ESBT toopogy.

The STE50DE100 is designed for use in industrial converters and/or welding equipment.

Internal schematic diagrams



Order codes

Part Number	Marking	Package	Packing
STE50DE100	STE50DE100	ISOTOP	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum rating

Symbol	Parameter	Value	Unit
$V_{CS(SS)}$	Collector-source voltage (V_{BS} = V_{GS} = 0 V)	1000	V
$V_{BS(OS)}$	Base-source voltage (I_C = 0, V_{GS} = 0 V)	40	V
$V_{SB(OS)}$	Source-base voltage (I_C = 0, V_{GS} = 0 V)	12	V
V_{GS}	Gate-source voltage	± 20	V
I_C	Collector current	50	A
I_{CM}	Collector peak current (t_P < 5ms)	150	A
I_B	Base current	10	A
I_{BM}	Base peak current (t_P < 5ms)	50	A
P_{tot}	Total dissipation at T_c = 25°C	160	W
V_{INS}	Insulation withstand voltage (AC-RMS) from all four leads to external heatsink	2500	V
T_{stg}	Storage temperature	-40 to 150	°C
T_J	Max. operating junction temperature	150	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.78	°C/W
$R_{thc\text{-}h}$	Thermal resistance case-heatsink with conductive grease applied max	0.05	°C/W

2 Electrical characteristics

(T_{case} = 25°C unless otherwise specified)

Table 3. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{CS(SS)}$	Collector-source current ($V_{BS} = V_{GS} = 0$)	V_{CE} = 1000V			100	µA
$I_{BS(OS)}$	Base-source current ($I_C = 0$, $V_{GS} = 0$)	$V_{BS(OS)}$ = 40V			10	µA
$I_{SB(OS)}$	Source-base current ($I_C = 0$, $V_{GS} = 0$)	$V_{SB(OS)}$ = 10V			100	µA
$I_{GS(OS)}$	Gate-source leakage	V_{GS} = ± 20V			500	nA
$V_{CS(ON)}$	Collector-source ON voltage	V_{GS} = 10V I_C = 50A I_B = 10A V_{GS} = 10V I_C = 30A I_B = 3A		1.3 1.1		V V
h_{FE}	DC current gain	V_{GS} = 10V I_C = 50A V_{CS} = 1V V_{GS} = 10V I_C = 30A V_{CS} = 1V	3 6		7 13	
$V_{BS(ON)}$	Base Source ON voltage	V_{GS} = 10V I_C = 50A I_B = 10A V_{GS} = 10V I_C = 30A I_B = 3A		2.2 1.4		V V
$V_{GS(th)}$	Gate threshold voltage	$V_{BS} = V_{GS}$ I_B = 250µA	3	3.7	4.5	V
C_{ISS}	Input capacitance	V_{CS} = 25V f = 1MHz $V_{GS} = V_{CB}$ = 0		2500		pF
$Q_{GS(tot)}$	Gate-source charge	V_{CS} = 25V V_{GS} = 10V V_{CB} = 0 I_C = 50A		60		nC
t_s t_f	INDUCTIVE LOAD Storage time Fall time	I_C = 25A I_B = 5A V_{GS} = 10V V_{Clamp} = 800V R_G = 47Ω t_p = 4µs (see figure 13)		650 10		ns ns
t_s t_f	INDUCTIVE LOAD Storage time Fall time	I_C = 25A I_B = 2.5A V_{GS} = 10V V_{Clamp} = 800V R_G = 47Ω t_p = 4µs (see figure 13)		430 6		ns ns
V_{CSW}	Maximum collector-source voltage switched without snubber	R_G = 47Ω h_{FE} = 5A I_C = 35A	1000			V
$V_{CS(dyn)}$	Collector-source dynamic voltage (500ns)	$V_{CC} = V_{Clamp}$ = 300V V_{GS} = 10V R_G = 47Ω I_C = 5A I_B = 5A $I_{Bpeak} = I_C$ = 25A t_{peak} = 500ns		5.5		V
$V_{CS(dyn)}$	Collector-source dynamic voltage (1 µs)	$V_{CC} = V_{Clamp}$ = 300V V_{GS} = 10V R_G = 47Ω I_C = 5A I_B = 5A $I_{Bpeak} = I_C$ = 25A t_{peak} = 500ns		4.8		V

2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

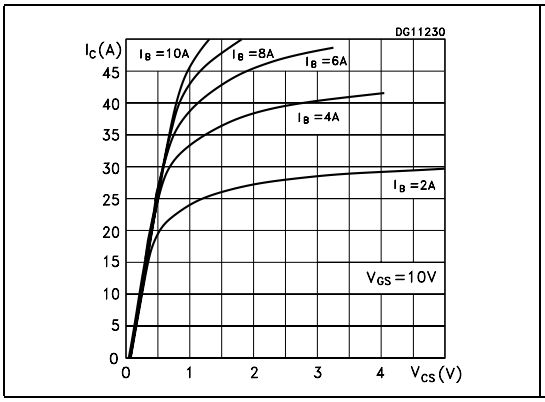


Figure 2. DC current gain

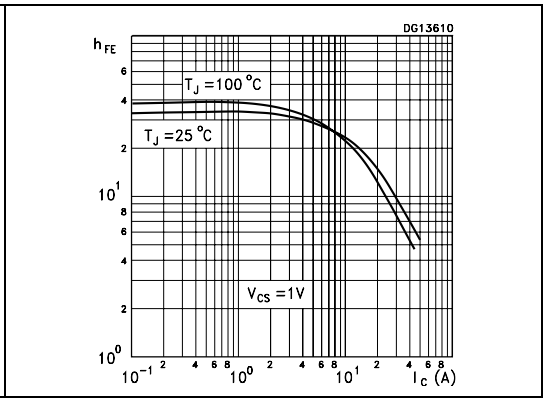


Figure 3. Collector-source On voltage

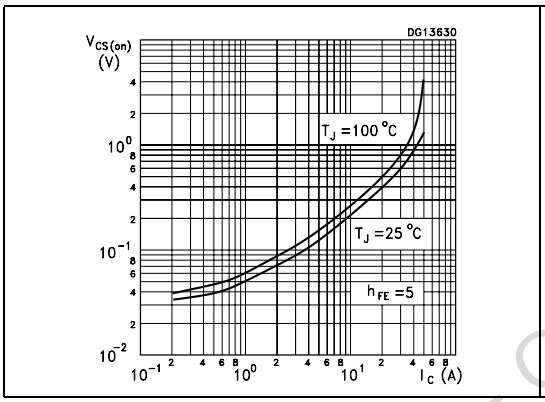


Figure 4. Collector-source On voltage

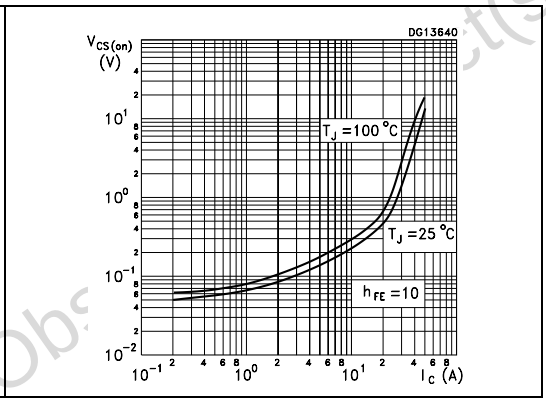


Figure 5. Base-source On voltage

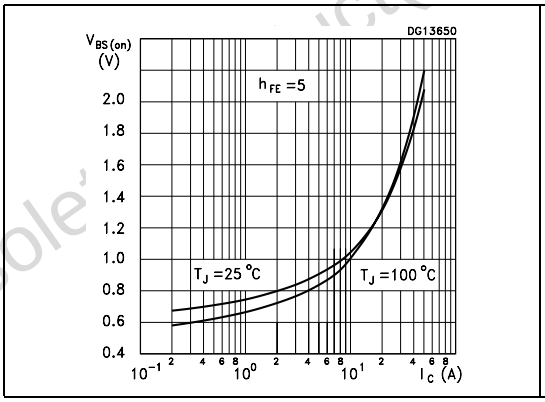


Figure 6. Base-source On voltage

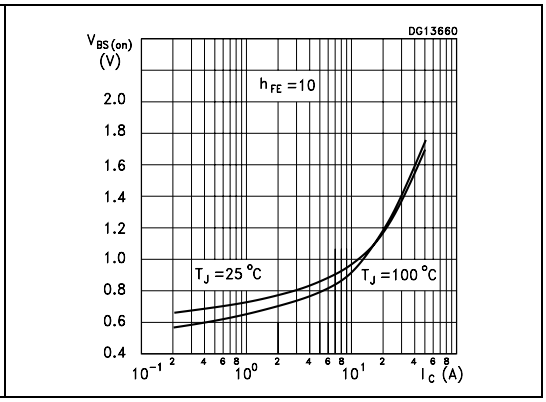


Figure 7. Reverse biased safe operting area

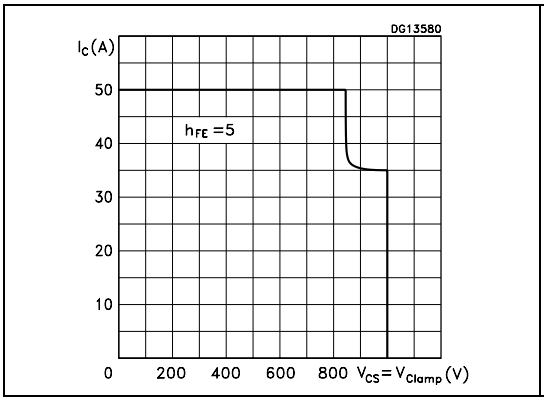


Figure 8. Gate threshold voltage vs temperature

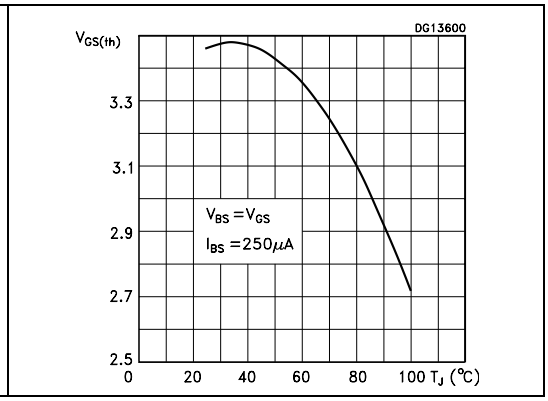


Figure 9. Dynamic collector-emitter saturation voltage

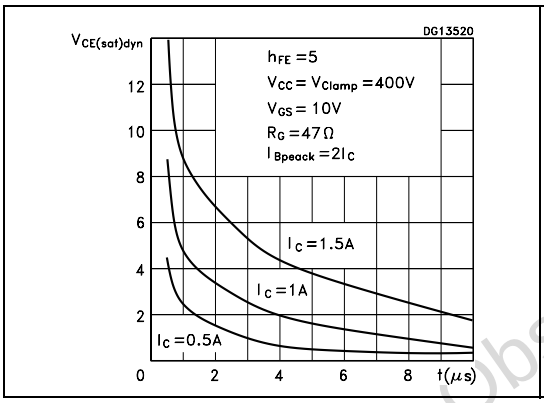


Figure 10. Inductive load switching time

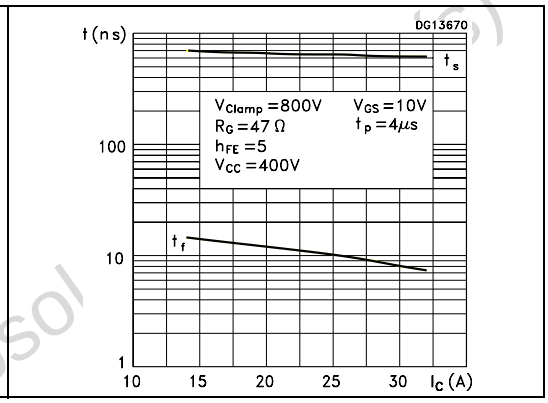
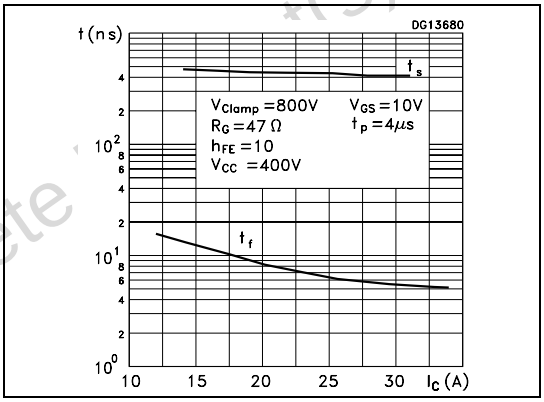


Figure 11. Inductive load switching time



2.2 Test circuits

Figure 12. Static $V_{CS(ON)}$ test circuit

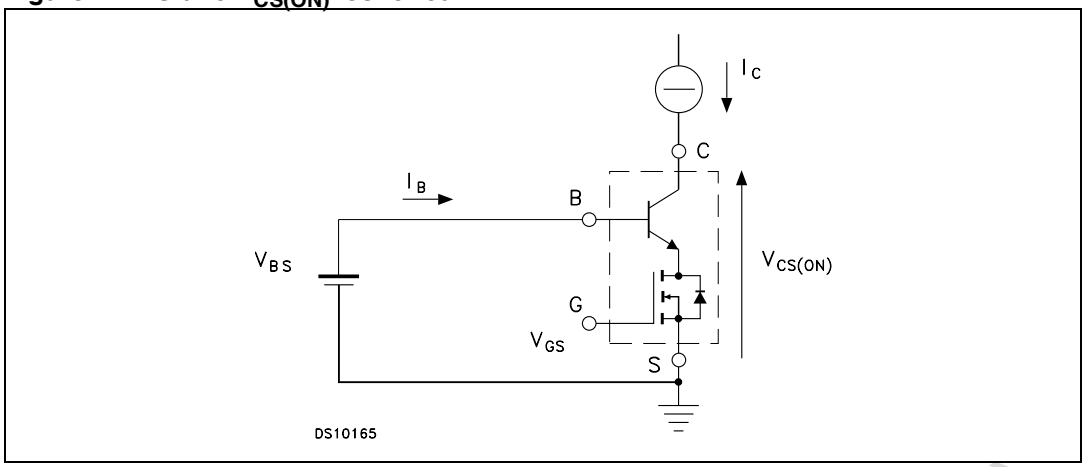


Figure 13. Inductive load switching and RBSOA test circuit

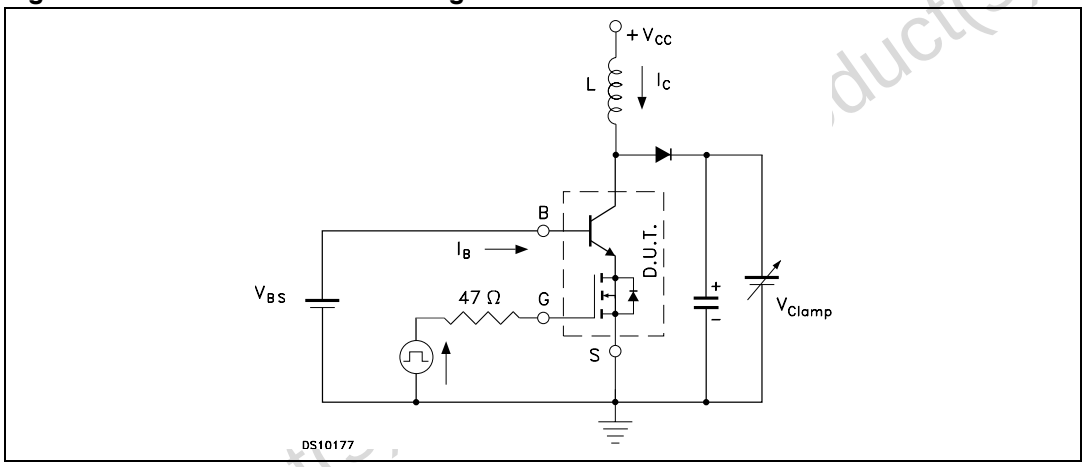
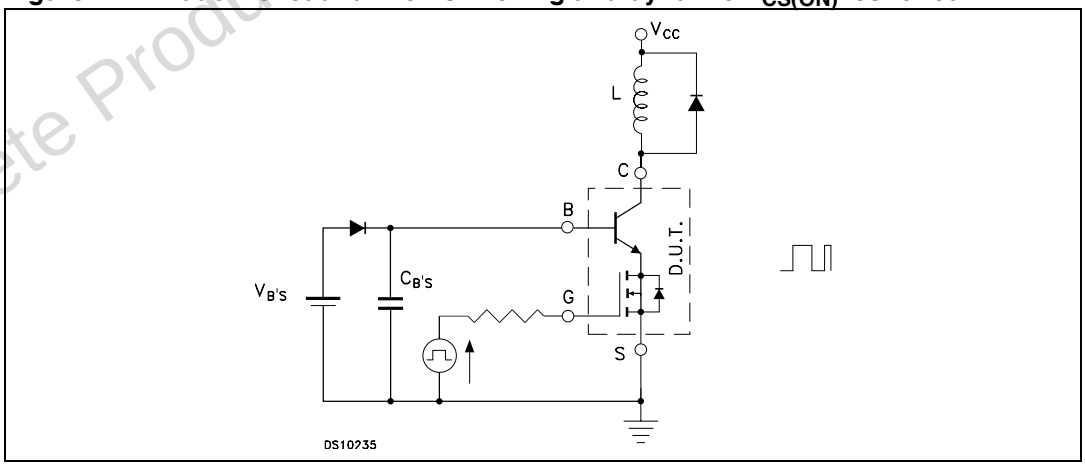


Figure 14. Inductive load turn-on switching and dynamic $V_{CS(ON)}$ test circuit

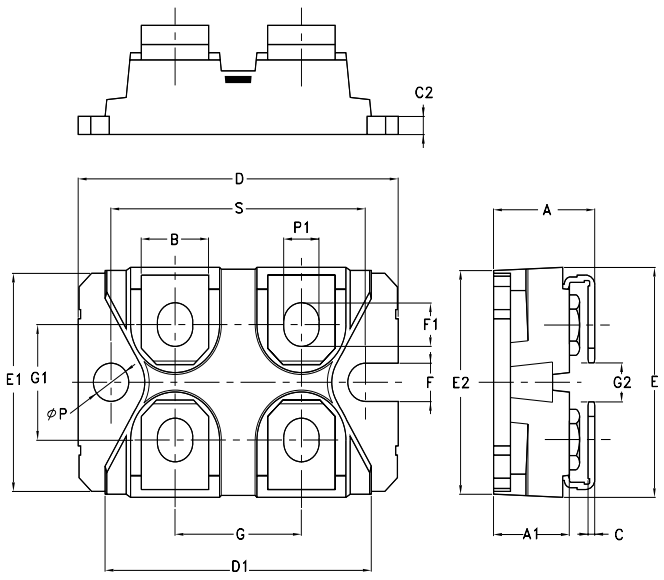


3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.465		0.480
A1	8.9		9.1	0.350		0.358
B	7.8		8.2	0.307		0.322
C	0.75		0.85	0.029		0.033
C2	1.95		2.05	0.076		0.080
D	37.8		38.2	1.488		1.503
D1	31.5		31.7	1.240		1.248
E	25.15		25.5	0.990		1.003
E1	23.85		24.15	0.938		0.950
E2		24.8			0.976	
G	14.9		15.1	0.586		0.594
G1	12.6		12.8	0.496		0.503
G2	3.5		4.3	0.137		1.169
F	4.1		4.3	0.161		0.169
F1	4.6		5	0.181		0.196
P	4		4.3	0.157		0.169
P1	4		4.4	0.157		0.173
S	30.1		30.3	1.185		1.193



P093A

4 Revision history

Table 4. Revision history

Date	Revision	Changes
06-Oct-2004	1	Initial release.
22-Jan-2007	2	The document has been reformatted

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