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AN2495
Application note

3-phase 80 W SMPS with very wide-range input voltage based on the L6565 and ESBT® STC04IE170HV

1 Introduction

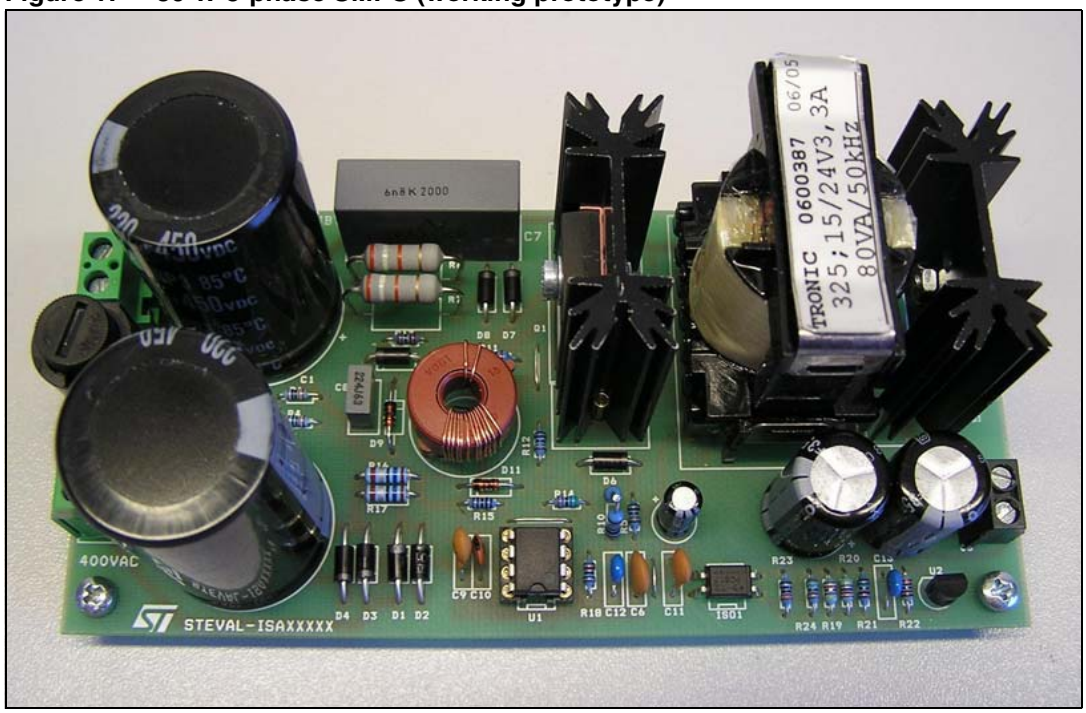
The purpose of this application note is to explain the design of an 80 W 3-phase auxiliary power supply for motor drives and welding applications. To reach a high level system in terms of both efficiency and cost, the L6565 PWM controller has been selected as well as the STC04IE170HV as the main switch. The combination of these STMicroelectronics™ parts provides a highly efficient solution for high DC input voltage, a typical requirement of any three-phase application. The L6565 driver is a variable frequency PWM driver suitable for a design flyback converter working in quasi-resonant mode. It also includes some very useful additional features.

The frequency response study reported in the this document is carried out using MATLAB.

All the design choices are thoroughly discussed to allow the user to adapt the project to specific needs. The input voltage can also be extended up to 1000 VDC as enough margin exists to do so. Finally, the experimental results are analyzed to better understand the benefits offered by the use of ESBT® in this application.

The document is associated with demonstration boards STEVAL-ISA019V1, STEVAL-ISA019V2 and STEVAL-ISA019V3 (*Figure 1*).

Figure 1. 80 W 3-phase SMPS (working prototype)



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2 Design specifications and L6565 brief description

Table 1 lists the converter specification data and the main parameters set for the demonstration board.

Table 1. Converter specification data and fixed parameters

Symbol	Description	Values
V_{inmin}	Rectified minimum input voltage	250
V_{inmax}	Rectified maximum input voltage	850
V_{out}	Output voltage 1	24 V/3.33 A
V_{aux}	Auxiliary output voltage	15 V/0.1 A
P_{out}	Maximum output power	80 W
h	Converter efficiency	> 80%
F	Minimum switching frequency	50 kHz
V_{spike}	Max. overvoltage limited by clamping circuit	200 V

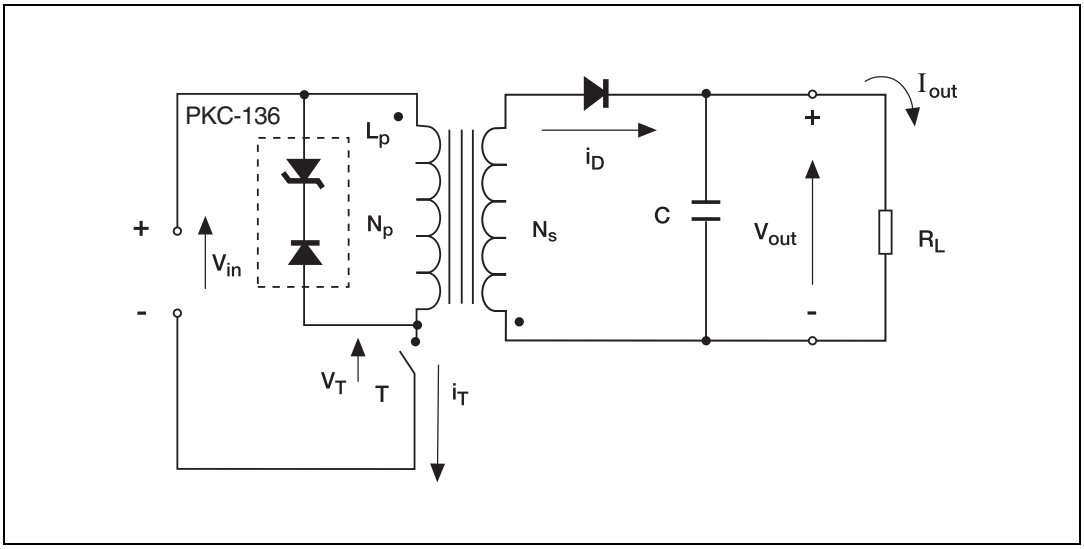
Figure 2 shows a simplified schematic diagram of a flyback converter.

The L6565 features a current mode control and is designed for flyback converters working in quasi-resonant mode and ZVS (zero voltage switching) at turn-on, or at least quasi ZVS, which means valley switching during turn-on. This condition allows the designer to reduce the power losses at turn-on as much as possible.

Since the input range is from 250 V up to 850 V, the ZVS is obtained only when $V_{in} = V_{inmin} = V_{fl} = 250$ V.

The L6565 has 8 pins. For a detailed explanation of each pin function, please refer to the L6565 datasheet.

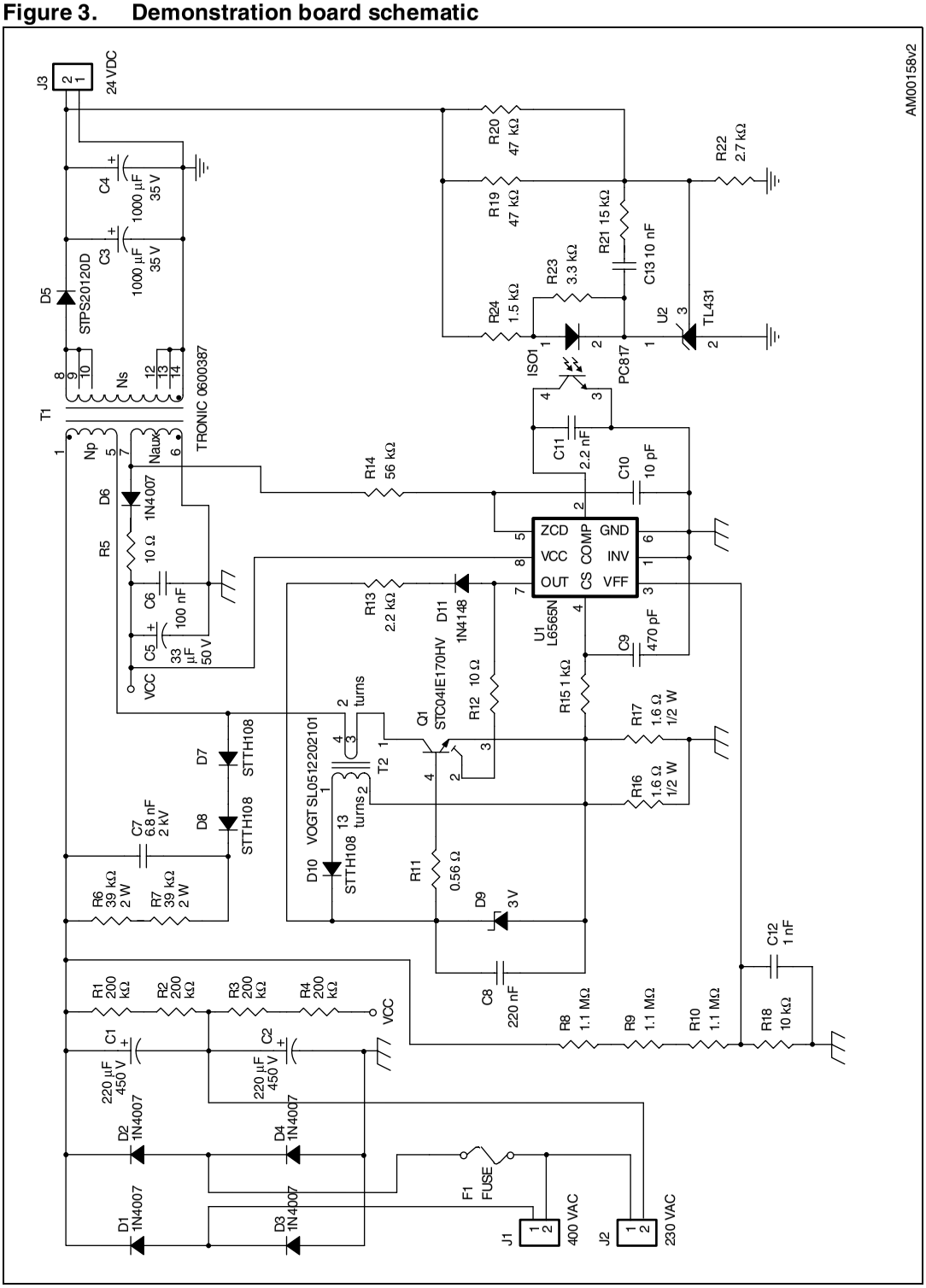
Figure 2. Flyback topology basic diagram



3 Flyback stage design

In *Figure 3* the complete schematic of the 80 W SMPS is shown.

Figure 3. Demonstration board schematic



As commonly known, the voltage stress on the device (power switch) is given by:

Equation 1

$$V_{off} = V_{inmax} - V_{fl} - V_{spike}$$

where V_{fl} = flyback voltage = (V_{out} + V_F, diode) *N_p/N_s and V_{spike} is the maximum overvoltage allowed by the clamping network. It has been set at 200 V. N_p is the number of turns on the primary side, while N_s is the number of turns on the main output secondary winding.

Taking into account a 200 V margin, the maximum flyback voltage that can be chosen is:

Equation 2

$$V_{fl} = BV - V_{inmax} - V_{spike} - V_{margin} = 1700 - 1000 - 200 - 250 = 250V$$

After calculating the flyback voltage, proceed with the next step in the converter design.

The turn ratio between primary and secondary side is calculated with the following equation:

Equation 3

$$\frac{N_p}{N_s} = \frac{V_{fl}}{V_{out} + V_{F,\ diode}} = \frac{250}{24 + 1} = 10$$

As a first approximation, since the turn-on of the device occurs immediately after the energy stored on the primary side inductance has been totally transferred to the secondary side:

Equation 4

$$V_{dcmin} T_{onmax} = V_{fl} T_{reset}$$

and

Equation 5

$$T_{onmax} + T_{reset} = T_S$$

where T_{onmax} is the maximum on time, T_{reset} is the time needed to demagnetize the transformer inductance and T_S is the switching time.

Combining the two previous equations, T_{onmax} is:

Equation 6

$$T_{onmax} = \frac{V_{fl} \bullet T_S}{V_{dcmin} + V_{fl}} \cong 10\mu s$$

The next step is to calculate the peak current. According to the converter specification in *Table 1*, output power of 80 W and desired efficiency (at least 80%), by using a formula that does not take into account the losses on the power switch, on the input bridge, and on the rectified network, we have:

Equation 7

$$P_{IN} = 1.25 P_{OUT} = \frac{\frac{1}{2} \bullet L_P I_P^{\ 2}}{T_S} = \frac{\frac{1}{2} V_{dcmin}^{\ 2} T_{onmax}^{\ 2}}{L_P T_S}$$

Hence:

Equation 8

$$L_P = \frac{V_{dcmin}^{2} T_{onmax}^{2}}{2.5 T_S P_{OUT}} = 1.56mH$$

Now we can calculate the peak current on primary.

Equation 9

$$I_P = \frac{V_{dcmin} T_{onmax}}{L_P} = 1.6A$$

3.1 Transformer design

3.1.1 Core size

The core size must be chosen according to the power that must be managed, to the primary inductance, and to the saturation current as well. An approximate but efficient formula could be used as a starting point. Eventually, the designer may choose a bigger core and repeat the following steps.

Equation 10

$$A_P = 10^3 \left[\frac{L_P I_{rms(primary)}}{\Delta T^{\frac{1}{2}} \bullet K_u \bullet B_{max}} \right]^{1.316} \quad [cm^4]$$

where:

- ΔT is the maximum temperature variation with respect to the ambient temperature
- K_U is the utilization factor of the window (say the portion of the window used for winding that generally ranges between 0.4 and 0.7)
- B_{max} is the maximum flux in the core.

From *Equation 10*, we can deduct that the final best choice is an ETD34.

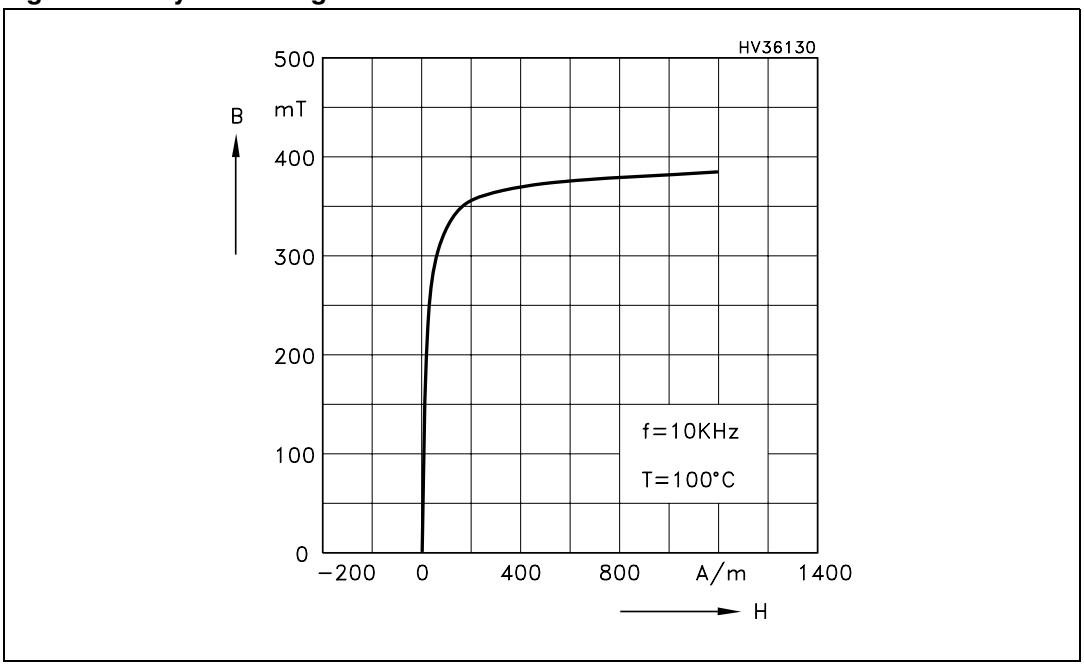
3.1.2 Transformer losses and air gap

From Faraday's law we can define the minimum primary winding turns to avoid saturation of the core. Looking at the saturation curve of the core, we can safely work up to 200 mT:

Equation 11

$$N_{pmin} = \frac{V_{in,\ min} \bullet T_{O(N,\ max)}}{\Delta B \bullet A_e} = \frac{250 \bullet 10\mu}{0.200 \bullet 97\mu} = 117$$

Figure 4. Dynamic magnetization curves



Concerning the gap, from the EPCOS datasheet, we can use the following approximate equation:

Equation 12

$$l_g = \text{gaplenght} = \left(\frac{A_L}{K_1}\right)^{\frac{1}{K_2}}$$

$K_1 = 153$, $K_2 = -0.713$, while A_L has to be calculated.

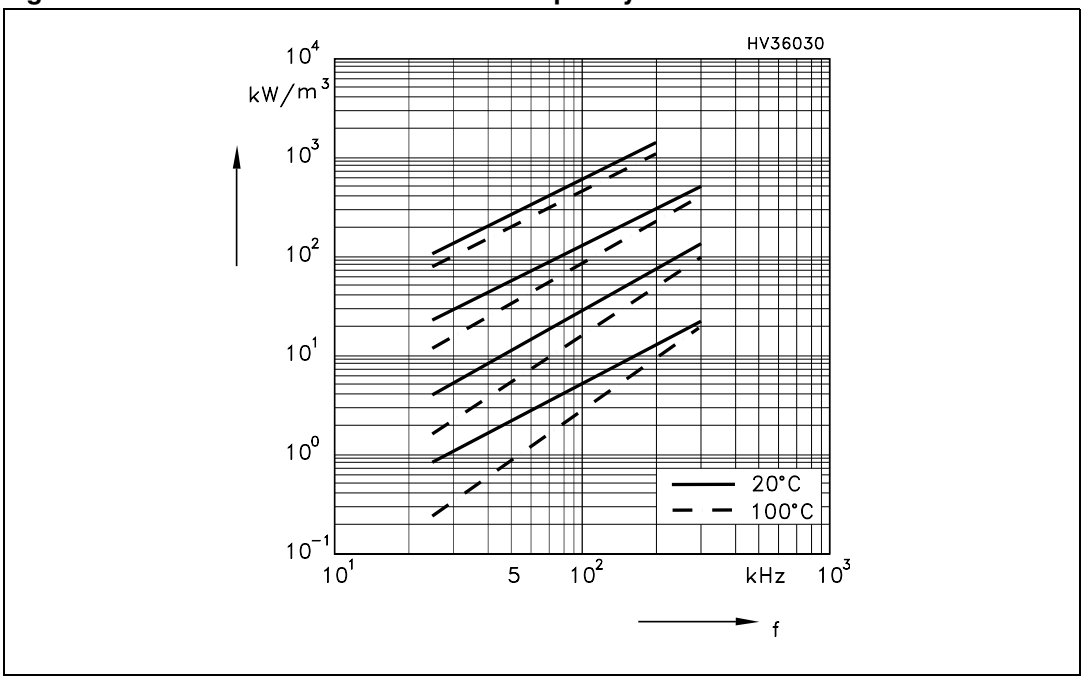
Knowing that $L_p = 1.56mH$ and $N_p = 120$,

Equation 13

$$A_L = \frac{L_P}{N^2_P} = \frac{1.56m}{120^2} = 108nH$$

Hence: $l_g = \text{gaplenght} = \left(\frac{108}{153}\right)^{\frac{1}{-0.713}} = 1.63mm$

Figure 5. Relative core losses versus frequency



From *Figure 5*, operating at 50 kHz with 220 mT flux excursion, the power dissipation density is about 300 mW/cm^3. Once again, referring to the EPCOS datasheet, the total volume of ETD 34 is 7.63 cm^3, therefore:

Equation 14

$$P_{core} = 0.3 \bullet 7.6 = 2.29W$$

Assuming a 95% efficiency for the transformer, only 4 W can be lost on it, of which about 2.3 is lost on the core while the residual 1.7 W is dissipated on the copper. Achieving this efficiency is detailed in the following *Section 3.1.3: Wire size*.

3.1.3 Wire size

To chose the right wire size we must know the rms current on both the primary and secondary sides. Since $I_{peak,\ primary}$ = 1.6 A and $I_{peak,\ secondary}$ = 16 A

Equation 15

$$I_{rms,\ primary} = 0.65A \quad \text{and} \quad I_{rms,\ secondary} = 6.53A$$

By imposing a 1 W loss on the primary side wire, the maximum series resistance can be calculated as follows:

From Joule's law we can calculate the resistance of both the primary and secondary windings.

Equation 16

$$R_P = \frac{P_{CU,\ pri}}{I_{PRMS}^2} \Rightarrow R_P = 2.36\Omega \qquad R_S = \frac{P_{CU,\ sec}}{I_{SRMS}^2} \Rightarrow R_S = 0.016\Omega$$

From that, knowing the copper resistivity at 100 °C ($\rho_{100} = 2.303\ 10^{-6}\ \Omega$ cm), and the average wind length L_t (L_t = 5.6 cm), we can easily calculate the wire sections (in cm^2).

Equation 17

$$A_{PCU} = \frac{\rho_{100} N_p L_t}{R_P} = 6.54 \bullet 10^{-4} \qquad [cm^2] \Rightarrow d_p = 0.028[cm]$$

Equation 18

$$A_{SCU} = \frac{\rho_{100} N_S L_t}{R_S} = 0.0096 \qquad [cm^2] \Rightarrow d_s = 0.011[cm]$$

Table 2 provides the skin effect resistance ratios due to Eddy currents for different frequencies.

Table 2. Skin effect AC-DC resistance ratios for square-wave currents

		25 kHz			50 kHz			100 kHz			200 kHz		
Wire no.	Diameter d, mils	Skin depth S, mils	d/S	R_{ac}/R_{dc}	Skin depth S, mils	d/S	R_{ac}/R_{dc}	Skin depth S, mils	d/S	R_{ac}/R_{dc}	Skin depth S, mils	d/S	R_{ac}/R_{dc}
12	81.6	17.9	4.56	1.45	12.7	6.43	1.55	8.97	9.10	2.55	6.34	12.87	3.50
14	64.7	17.9	3.61	1.30	12.7	5.08	1.54	8.97	7.21	2.00	6.34	10.21	2.90
16	51.3	17.9	2.87	1.10	12.7	4.04	1.25	8.97	5.72	1.70	6.34	8.09	2.30
18	40.7	17.9	2.27	1.05	12.7	3.20	1.15	8.97	4.54	1.40	6.34	6.42	1.85
20	32.3	17.9	1.80	1.00	12.7	2.54	1.05	8.97	3.60	1.25	6.34	5.09	1.54
22	25.6	17.9	1.43	1.00	12.7	2.02	1.00	8.97	2.85	1.10	6.34	4.04	1.30
24	20.3	17.9	1.13	1.00	12.7	1.60	1.00	8.97	2.26	1.04	6.34	3.20	1.15
26	16.1	17.9	0.90	1.00	12.7	1.27	1.00	8.97	1.79	1.00	6.34	2.54	1.05
28	12.7	17.9	0.71	1.00	12.7	1.00	1.00	8.97	1.42	1.00	6.34	2.00	1.00
30	10.1	17.9	0.56	1.00	12.7	0.80	1.00	8.97	1.13	1.00	6.34	1.59	1.00
32	8.1	17.9	0.45	1.00	12.7	0.84	1.00	8.97	0.90	1.00	6.34	1.28	1.00
34	6.4	17.9	0.36	1.00	12.7	0.50	1.00	8.97	0.71	1.00	6.34	1.01	1.00

Note: To completely avoid the skin effect, the maximum diameter allowed is 20.3 mils, which is equal to 0.5 mm.

For practical considerations, to better optimize the utilization of the transformer window, and comply with *Equation 15* to *Equation 18* and *Table 2*, it can be determined that:

Equation 19

$$d_s = 0.05[cm]3inparallel$$

The specifications of the transformer according to the above calculations are listed below.

Application specifications

Safety information - IEC EN60950

- V_{inmin} = 250 V DC
- V_{inmax} = 850 V DC
- P_{outmax} = 80 W
- V_{out} = 24 V (power output 80 W)
- I_{outmax} = 3.33 A
- V_{aux} = 15 V (to drive the IC < 1 W)
- F_{swmin} = 50 kHz (max. load, min. V_{in})
- $V_{flyback}$ = 250 V
- $I_{peak(primary)}$ = 1.6 A
- $I_{rms(primary)}$ = 0.65 A
- $I_{peak(secondary)}$ = 16 A
- $I_{rms(secondary)}$ = 6.5 A
- $L_{p\ (primary\ inductance)}$ = 1.56 mH
- N_p/N_s = 10
- N_p/N_{aux} = 17

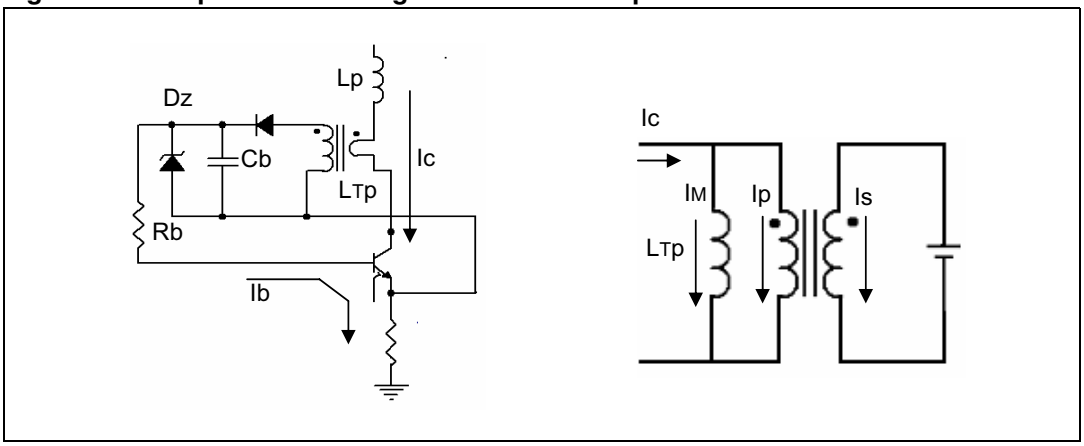
Wires and ferrite used

- N_p = 120 d = 0.28 mm
- N_s = 12 d = 0.5 mm 3 in parallel
- N_{aux} = 7 d = 0.28 or smaller
- The core used is an ETD 34, N67 material from EPCOS or equivalent.
- Air gap = 1.8 mm

4 Base driving circuit design

In practical applications such as SMPS where the load is variable, the collector current is variable as well. As a consequence it is very important to provide a base current to the device which is related to the collector. In this way it is possible to avoid device over-saturation at low load and to optimize the performance in terms of power dissipation. The best and simplest way to do this is the proportional driving method provided by the current transformer in *Figure 6*. At the same time, it is very useful to provide a short pulse to the base to make the turn-on as fast as possible and to reduce the dynamic saturation phenomenon. The pulse is achieved by using the capacitor and the Zener diode in *Figure 6*.

Figure 6. Proportional driving schematic and equivalent circuit



The I_C/I_B ratio is fixed once the current transformer turn ratio has been chosen. From the ESBT STC04DE170 datasheet, and especially looking at the storage time characterization, it is clear that a turn ratio equal to 5 is a good value to ensure the right saturation of the ESBT at I_C = 2 A, so that in the current transformer we can first fix:

Equation 20

$$\frac{N_P}{N_S} = \frac{1}{5}$$

The core magnetic permeability of current transformer must be as high as possible to minimize the magnetization current I_M (which is not transferred to the secondary side but only drives the core into saturation). On the contrary, a too high permeability core may lead the core into saturation even with a very small magnetization current. To avoid saturation, it is necessary to increase the number of primary turns and the size of the core as well. If a core with a very small magnetic permeability is chosen, it is possible to reduce the number of primary turns and the core size. If the permeability is too small, we may not have current on the secondary side because almost all the collector current becomes magnetization current. As a compromise, a ferrite material with a relative permeability in the range 4500-7000 is the best choice.

After selecting the ferrite ring diameter, the minimum primary turns is determined to avoid core saturation from the preliminarily fixed turn ratio N with 0.2. By applying Faraday's law and imposing the maximum flux B_{max} equal to $B_{sat}/2$:

Equation 21

$$V_1 = N_{TP} \bullet \frac{d\varphi}{dt} \cong N_{TP} \bullet A_e \bullet \frac{\Delta B}{\Delta T} \Rightarrow N_{TP} = 2 \bullet \frac{V_1 \bullet T_{onmax}}{A_e \bullet B_{sat}}$$

where B_{sat} is the saturation flux of the core which depends on the magnetic permeability.

During the conduction time, the junction base-emitter of the ESBT can be seen as a forward-biased diode. To complete the secondary side load loop, the voltage drop on both diode D and resistor RB must be added in series with the base of the ESBT. The equivalent secondary side voltage source is given by:

Equation 22

$$V_S = V_{BEon} - V_D - V_{RB} \cong 2.5V$$

Since the magnetization inductance cannot be neglected, only I_P, a fraction of the total collector current, is transferred to the secondary. As a result, the magnetization current has to be first as low as possible. Meanwhile, the value of the magnetization inductance must be taken into account for the proper calculation of transformer primary turns and turns ratio. The magnetization voltage drop, that is, the voltage at the primary of the current transformer, can now be easily calculated:

Equation 23

$$V_1 = V_S \bullet \frac{N_{1T}}{N_{2T}} = 2.5 \bullet \frac{1}{5} = 0.5(V)$$

The magnetization current will be:

Equation 24

$$I_{Mmax} = \frac{V_1 T_{ONmax}}{L_{TP}}$$

The number of primary turns should be increased if I_{Mmax} is relatively high. The core must have a window area large enough to hold all primary and secondary windings. Otherwise it is necessary to choose a bigger core size. Once both core material and size are fixed, the turn ratio must be adjusted to get the desiderated I_C/I_B ratio according to *Equation 25* below:

Equation 25

$$N_{eff} = \frac{I_P}{I_B} = \frac{I_{Cmax} - I_{Mmax}}{\frac{I_C}{5}}$$

where I_{Mmax} is the maximum magnetization current.

The insulation between primary and secondary should be considered since the voltage on the primary side during the off time can surpass 1500 V.

The next step is to select the Zener diode, the capacitor C_b, and the resistor R_b. The turn-on performance of the ESBT is related to the initial base peak current and its duration t_{peak}, which is given approximately by *Equation 26*:

Equation 26

$$t_{peak} = 3R_bC_b$$

A suitable value for R_b is 0.56 Ω It can eliminate the ringing on the base current after the peak, and at the same time, it generates negligible power dissipation.

The value t_{peak} can be determined once the minimum ON time is set based on the operating frequency. Bear in mind that in practical applications, it should never be lower than 200 ns. The value of C_b can be counted since the values of t_{peak} and R_b are known.

I_{peak} must be limited to avoid extra saturation of the device. The Zener diode D_z controls this and clamps the voltage across the small capacitor C_b. The Zener diode must be chosen according to the following empirical formulas and inside the range of V_{Zmin} and V_{Zmax}:

Equation 27

$$V_{Zmax} = 2(I_{peak}R_b + 1) \qquad V_{Zmin} = 2(I_{peak}R_b)$$

The base peak current is higher with higher clamp voltage (D_z) or smaller capacitance (C_b), which in turn will lead to shorter duration of the peak time.

The higher and longer the base peak current is, the lower the power dissipation during turn-on. The designer must limit the I_b peak both in terms of amplitude and time duration. Otherwise, at low load a very high saturation level may result. If the device is oversaturated, the storage time is too long with higher power dissipation during turn-off. Moreover, a long storage time can also lead to output oscillation, especially at high input voltage. To overcome these problems, it is recommended to set the peak duration to 1/3 the minimum duty cycle.

Following all the equations mentioned in this section applied to the present work gives:

Equation 28

$$N_{TP} = 2 \bullet \frac{V_1 \bullet T_{onmax}}{A_e \bullet B_{sat}} \approx 2$$

where A_e is the magnetic area, considering a ring core with 12.5 mm diameter, and the saturation field B_{sat} is 400 mT.

From the first approximated assumption NS should be 10. From bench verification it is very simple to verify that the turn ratio to get the best trade-off between conduction and turn-off losses is 6.

Of course, this verification and final decision has been taken after setting all the other components in the driving network and exactly:

Equation 29

$$t_{peak} = 3R_bC_c = 400ns = C_b = 238nF = C_b = 220nF \text{ (closet commercial value)}$$

Finally, the Zener diode has been set to 3 V.

5 Output circuit design

To choose the output capacitor, the series resistance of the electrolytic capacitor must be defined.

It is well known that the main cause of the output ripple is the series resistance of the electrolytic capacitor, known as ESR, while the capacitive ripple is absolutely negligible.

Therefore, with a known secondary side peak current of 16 A and imposing a resistive ripple equal to 2% (0.48 V), we have:

Equation 30

$$ESR < \frac{V_{ripple}}{I_{SP}} = \frac{0.48}{16} = 0.03\Omega$$

Using very low ESR output capacitances, from the catalogue we get the equation $ESR*C = 32e^{-6}s$ from which:

Equation 31

$$C_{out} > \frac{32 \bullet 10^{-6}}{ESR} = 1066\mu F$$

To obtain some margin and better thermal spread, the final choice is to use two 680 µF capacitors in parallel.

From Kirchoff's voltage law we can calculate the maximum voltage stress on the output diode:

Equation 32

$$V_{off-diode} = V_{out} + \frac{N_S}{N_P} \bullet V_{inmax} = 109V$$

Finally, adding a 10% margin, the STPS20120D has been selected.

6 Startup network design

To allow the circuit to start as soon as the line voltage is applied, it is necessary to pre-charge both C_5 and C_8 capacitances.

A resistor connected to the DC bus directly makes the pre-charge of C_5 electrolytic capacitance. The circuit must start at a minimum DC input voltage of 250 V. The current required by the L6565 driver during the startup time determines the (R_1+ R_2+ R_3+ R_4) value. Considering that the L6565 driver needs a 0.07 mA maximum startup current, we obtain:

Equation 33

$$(R_1 + R_2 + R_3 + R_4) < \frac{V_{inmin}}{I_{SU}} = \frac{250V}{0.07mA} \cong 3.6M\Omega$$

Startup resistance must be lower than 3.6 MΩ to reach the best trade-off between power dissipation and time-to-start. As a consequence, before choosing the startup resistor, we must determine the C_5 capacitance value, which is set according to another requirement. C_5 must be able to supply the L6565 driver until the steady state behavior of the converter is established. The time from bench verification is 20 ms maximum. Given a L6565 minimum hysteresis-voltage (difference between startup threshold and undervoltage threshold) of 3.7 V, the voltage across C5 must decrease less than 3.7 V during the startup period. From the L6565 datasheet we know that maximum quiescent current after turn-on is 3.5 mA, so C5 must be chosen such that:

Equation 34

$$\Delta V = \frac{I_Q \bullet \Delta t}{C_5} < 3.7V \Rightarrow C_5 > \frac{3.5mA \bullet 20ms}{3.7V} \cong 19\mu F$$

C_5 = 33 µF is a good choice to guarantee a good margin.

Finally, we can set the startup resistance value to reduce time-to-start and simultaneously optimize standby power dissipation. The L6565 has a maximum startup threshold of 14.5 V, therefore the maximum time-to-start is approximately:

Equation 35

$$\text{Time - to - start} = \frac{C_5 \bullet 14.5V}{\left(\frac{V_{inmin}}{(R_1 + R_2 + R_3 + R_4)}\right) - I_{SU}} \leq 2sec \Rightarrow (R_1 + R_2 + R_3 + R_4) \leq 808k\Omega$$

A good choice is to put in series four 200 kΩ resistors (R_1 = R_2 = R_3 = R_4 = 200 kΩ), which dissipate less than 1 W of standby power.

The pre-charge of C_8 base capacitance is carries out by connecting it to the OUT pin of the L6565 through a diode in series with a 2.2 kΩ resistor.

7 Frequency response and loop compensation

The transfer function in the complex frequency domain of the discontinuous current mode (DCM) flyback converter with L6565 driver is given by:

Equation 36

$$G_1(s) = \frac{V_{out(s)}}{V_{comp(s)}} = \frac{n \bullet R_{out} \bullet (1 - D_{max})}{2 \bullet R_S \bullet (1 + D_{max})} \bullet \frac{(1 + s \bullet C_{out} \bullet ESR)\left(1 - s \bullet \frac{L_p D_{max}}{n^2 R_{out}(1 - D_{max})^2}\right)}{1 + s \bullet \frac{C_{out} R_{out}}{1 + D_{max}}}$$

The parameters and values are listed in *Table 3*.

Table 3. Transfer function main parameters

Parameter	Description	Value
n	Primary/secondary turn-ratio	10
R_S	Sensing resistor	0.8 Ω
D_{max}	Maximum duty-cycle	0.5
ESR	Electrolytic series resistance	16 mΩ
$R_{out} = V_{out}/I_{out}$	Output load	7.2 Ω
C_{out}	Output capacitance	2 mF
L_p	Primary inductance	1.56 mH

It is worth noting that the transfer function has one pole and one zero on the left half plane and an additional zero on the right half plane. The RHP zero is very difficult, if not impossible, to compensate and therefore must be kept well beyond the closed-loop bandwidth. As a result, the transient response of such a system will not be extremely fast.

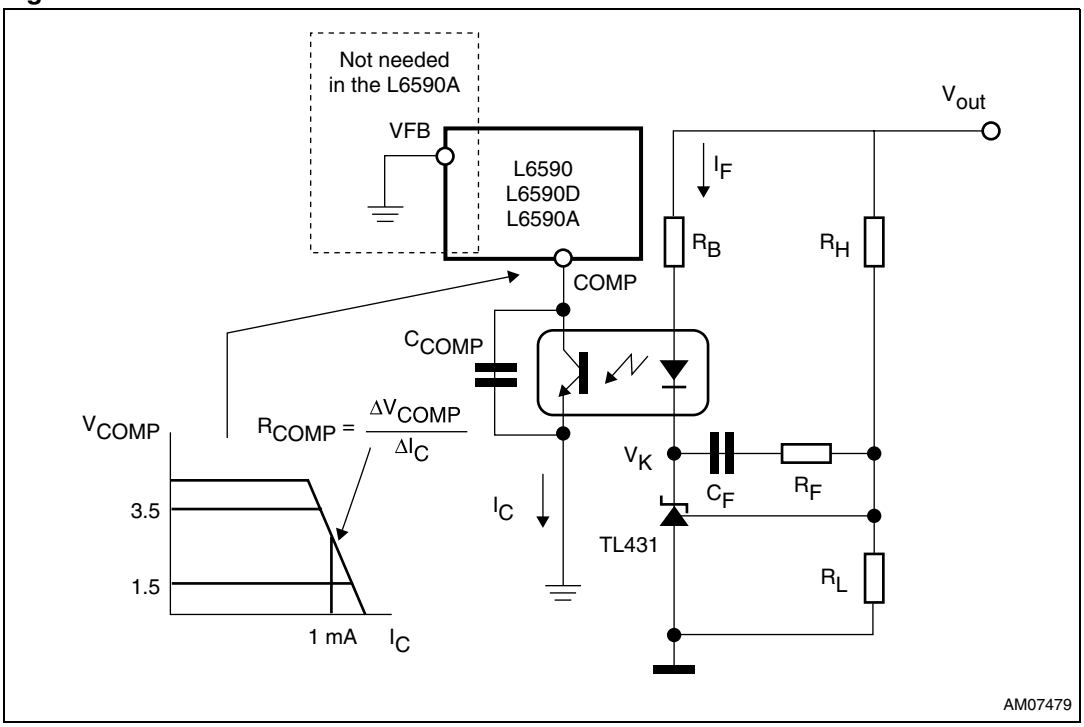
Poles and zeros are given in *Equation 37* and *Equation 38*:

Equation 37

$$f_p = 25Hz; f_{Z1} = 3.5 \bullet 10^5 Hz; f_{Z2} = 5 \bullet 10^3 Hz$$

A good line and load regulation implies a high DC gain, thus the open loop gain should have a pole at the origin. Normally in this case we need a feedback network like the one in *Figure 7*.

Figure 7. Converter feedback network



Its transfer function, which comprises a pole at the origin and a zero-pole pair, is given by:

Equation 38

$$G_2(s) = \frac{v_{comp}(s)}{V_{out}(s)} = \frac{CTR_{max} \bullet R_{COMP}}{R_B R_H C_F} \bullet \frac{1}{s} \bullet \frac{1 + s(R_H + R_F)C_F}{1 + sR_{COMP}C_{comp}}$$

The task of the control loop design is then to determine the transfer function $G_2(s)$ to ensure that the resulting closed-loop system is stable and performs well in terms of dynamic response, and line and load regulation. It is well known that the characteristics of the closed-loop system can be inferred from its open loop transfer function properties, that is $G(s) = G_1(s) \cdot G_2(s)$.

Frequency response requirements are summarized below:

1. Optimum dynamic performance requires a large gain bandwidth, that is the open loop cross-over frequency f_C to be typically chosen equal to $f_{sw}/5$ (f_c = 10 kHz).
2. Phase margin φ_m comprised between 45° and 90° is used as a design guideline. This ensures fast transient response with very little ringing. Sometimes this is not enough and so phase shift should be lower than 180° at any frequency below f_C, because a phase shift over 180° would result in a conditionally stable system.
3. Good load and line regulation implies a high DC gain (this requirement is ensured by the feedback network, whose transfer function has a pole at the origin).

First choose a typical value for $R_L = R_{22} = 2.7\ k\Omega$

From the L6565 datasheet we know that I_{comp} = 5 mA (source current) and R_{comp} = 15 kΩ and can obtain:

Equation 39

$$R_B = R_{24} < \frac{V_{out} - (V_{ref} - V_{diode})}{I_{comp}} = \frac{24V - 3.5V}{5mA} = 4.1k\Omega$$

R_{24} = 1.5 kΩ is a good choice. It is good practice to put a 3.3 kΩ resistor (R_{23} = 3.3 kΩ) in parallel to the photodiode.

The resistive partition must be set with high precision according to the following equation:

Equation 40

$$R_{high} = R_{22} \bullet \frac{V_{out} - V_{ref}}{V_{ref}} = 23.2k\Omega$$

There is no next close commercial value so it is a good idea to put two 47 kΩ resistors (R_{19} = R_{20} = 47 kΩ) in series.

Now C_{11} (C_{comp}), C_{13} (C_F) and R_{21} (R_F) must be set in order to satisfy frequency response requirements.

A good choice is to set the pole of $G_2(s)$ so as to cancel the low frequency zero of $G_1(s)$:

Equation 41

$$\frac{1}{2\pi \bullet R_{comp} \bullet C_{comp}} = 5kHz \Rightarrow C_{11} = C_{comp} \cong 2.12nF$$

The next close commercial value for C_{11} = 2.2 nF has been chosen.

Similarly C_{13} and R_{21} have been determined by setting the corresponding zero close to the pole of $G_1(s)$ and imposing the open loop gain to cross the 0 dB axis only once at f = f_c = 10 kHz:

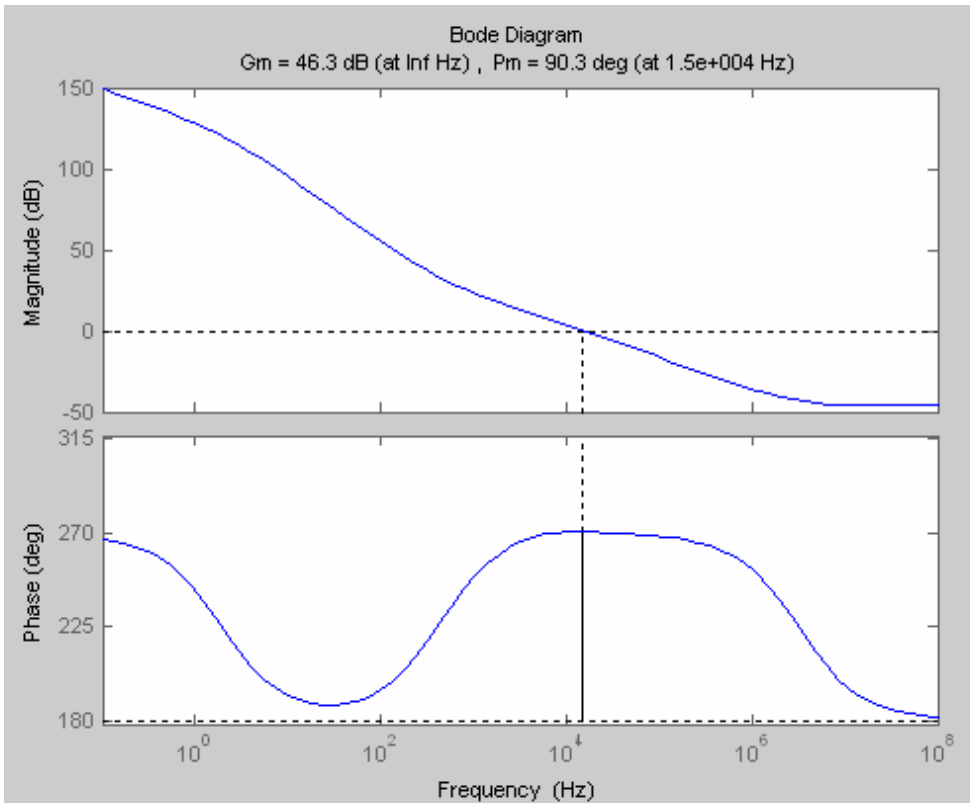
Equation 42

$$\begin{cases} \frac{1}{2\pi \bullet (R_H + R_F) \bullet C_F} = 400Hz \Rightarrow C_{13} = 10nF \\ |G(j\omega)|_{\omega = 2\pi \bullet 10^{-4} rad/sec} = 1 \Rightarrow R_{21} \cong 15k \end{cases}$$

In such a way we ideally get a phase margin of 90 degrees and an adequate closed-loop bandwidth.

Figure 8 shows Bode plots of the stabilized open loop transfer function.

Figure 8. Stabilized open loop transfer function $G(s) = G_1(s) \cdot G_2(s)$ (Bode plots)

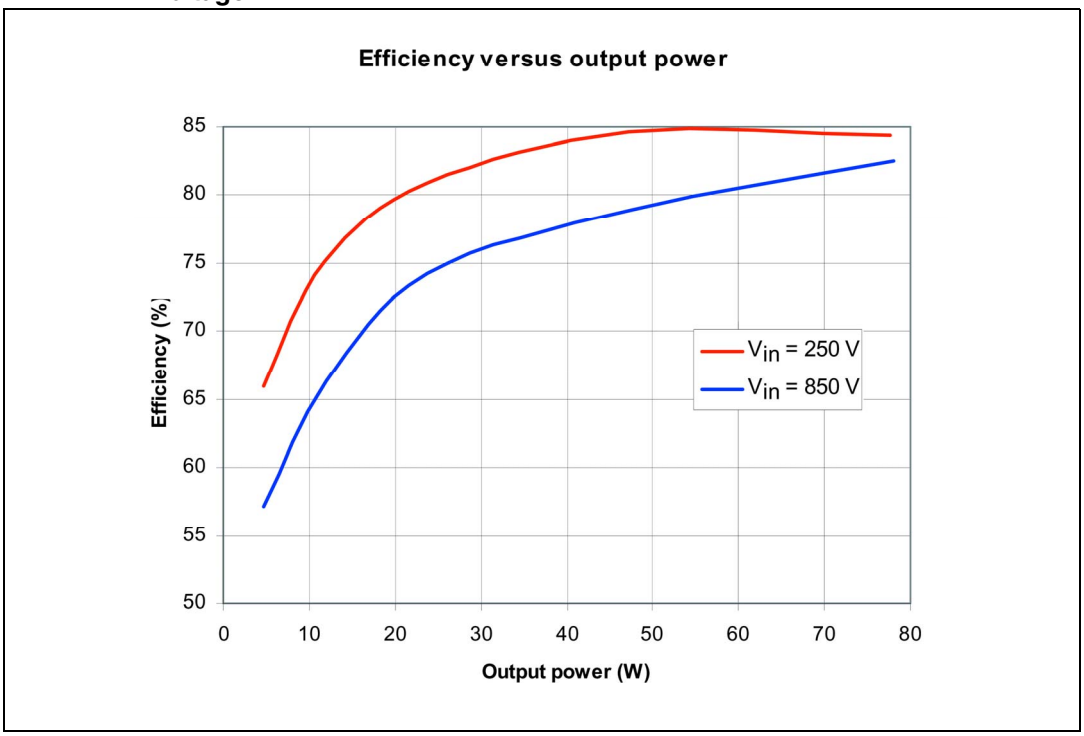


As expected, all requirements have been satisfied by properly choosing the feedback network. Gain bandwidth is quite large, phase margin is around 90°, and system stability margin is improved.

8 Efficiency, waveforms and experimental results

Overall efficiency variation versus output power is illustrated in *Figure 9* for two different values of input voltage.

Figure 9. Overall efficiency versus output power for two different values of input voltage



It is worth noting that with low input voltage (red curve), total efficiency is over 80%, and at medium and high load working conditions, reaching almost 85%. Efficiency decreases with input voltage. However, it is above 75% at loads higher than 30% even with maximum input voltage.

Theoretical assumptions made so far have been validated with the use of a demonstration board. A complete description of this board has been carried out and the most meaningful waveforms in any working condition are shown in *Figure 10* through *Figure 15*.

Figure 10, *Figure 11* and *Figure 12* show the prototype steady state behavior, by indicating the gate voltage (blue waveform), the base current (violet waveform) and the collector voltage (sky blue waveform) at maximum load for different input voltages.

Figure 10. Minimum input voltage-maximum load (250 V - 80 W) in steady state

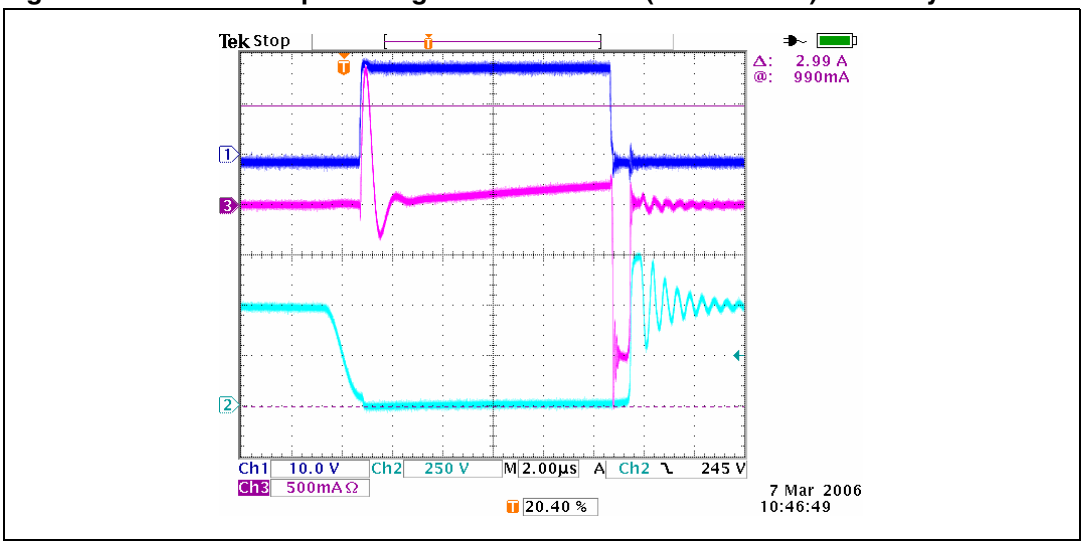


Figure 11. Medium input voltage-maximum load (500 V - 80 W) in steady state

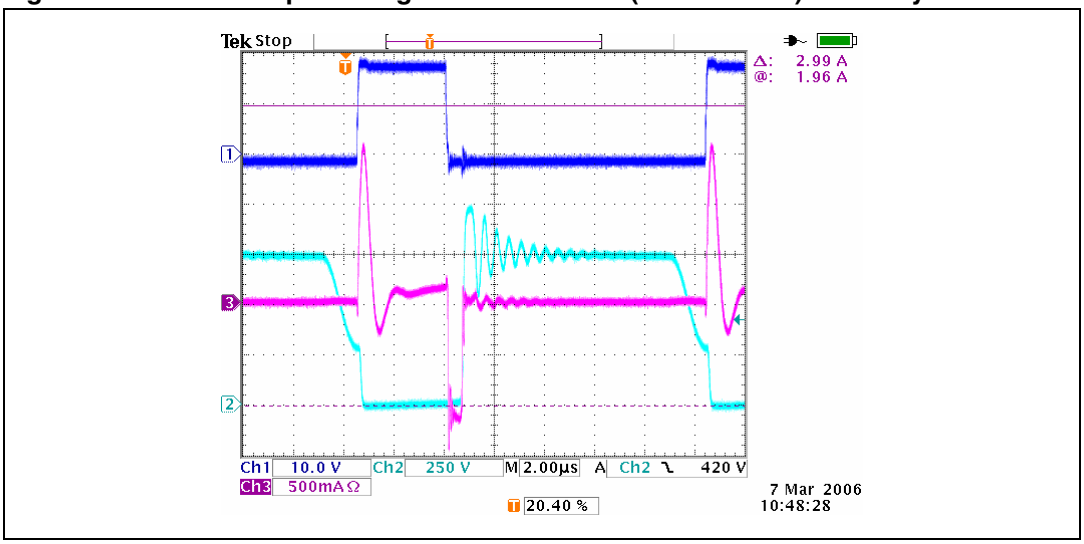
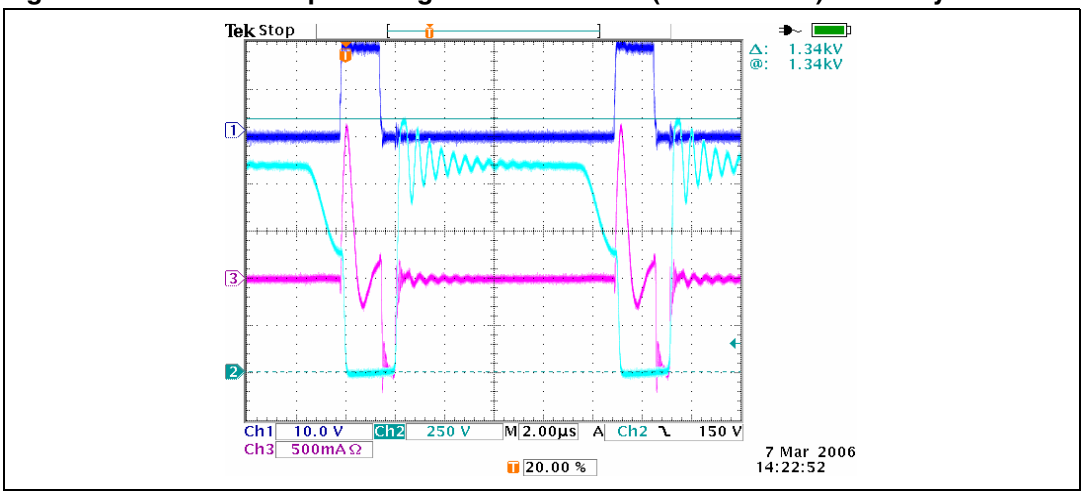


Figure 12. Maximum input voltage-maximum load (850 V - 80 W) in steady state



Waveforms in *Figure 13*, *Figure 14*, and *Figure 15* describe the function of the converter at both low and high load conditions with the same input rectified voltage.

Figure 13. Very low load condition (750 V - 5 W)

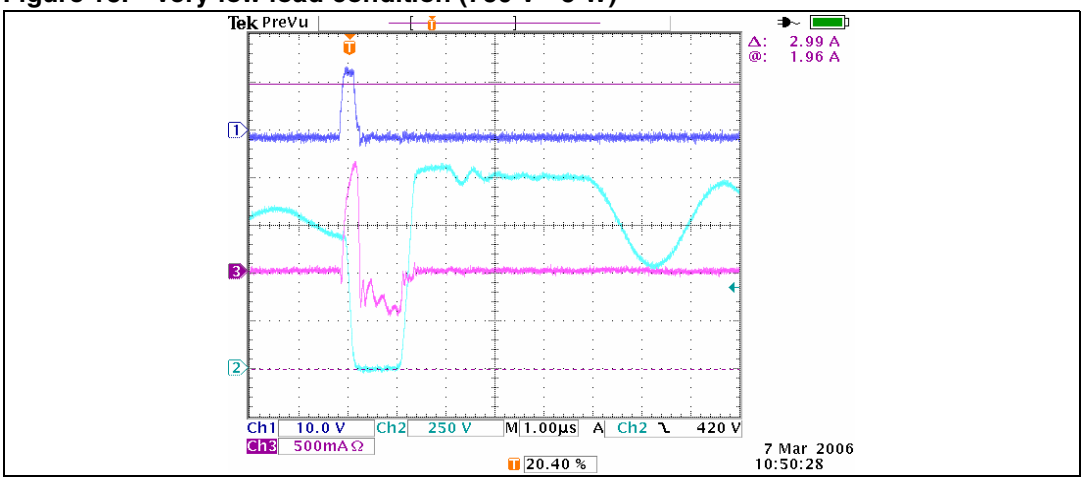


Figure 14. Low load condition (750 V - 24 W)

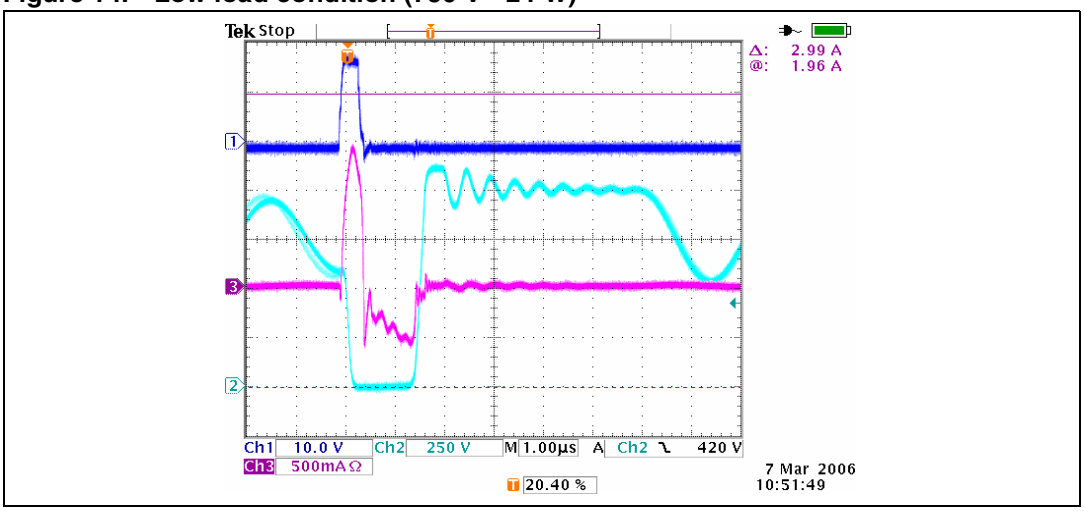
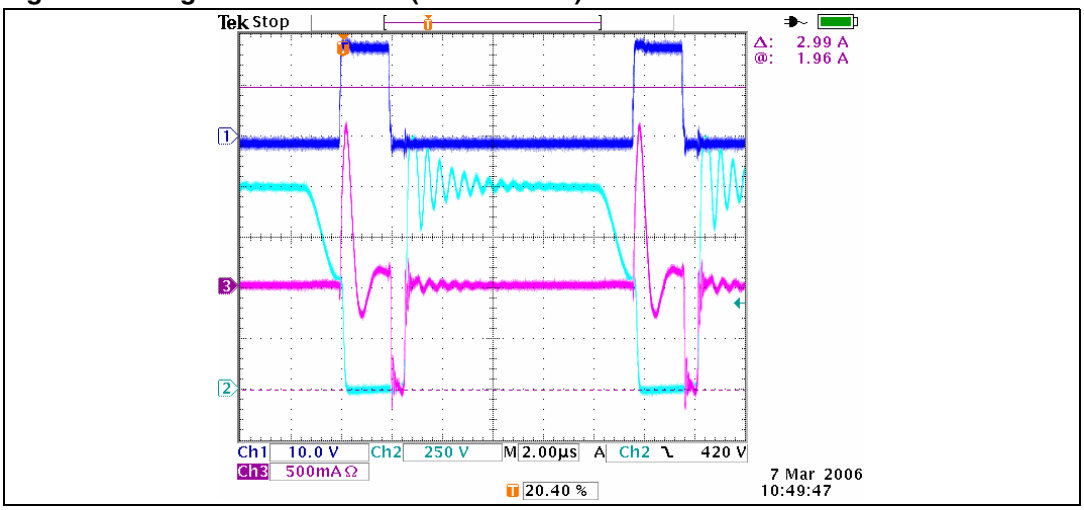


Figure 15. High load condition (750 V - 80 W)



The waveform in *Figure 16* illustrates the function of the proportional base driving network. In this graph, collector current is the violet line, while the base current line is light green.

Figure 16. Proportional base driving circuit relevant waveform