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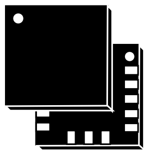
iNEMO inertial module: 3D accelerometer and 3D gyroscope

Datasheet - production data



LGA-16L (3x3x0.86 mm)

Features

- Analog supply voltage: 1.71 V to 3.6 V
- Independent IOs supply (1.71 V)
- “Always on” eco power mode down to 1.8 mA
- 3 independent acceleration channels and 3 angular rate channels
- ±2/±4/±8/±16 *g* full scale
- ±245/±500/±2000 dps full scale
- SPI/I^2C serial interface
- Embedded temperature sensor
- Embedded FIFO
- ECOPACK®, RoHS and “Green” compliant

Applications

- GPS navigation systems
- Impact recognition and logging
- Gaming and virtual reality input devices
- Motion-activated functions
- Intelligent power saving for handheld devices
- Vibration monitoring and compensation
- Free-fall detection
- 6D orientation detection

Description

The LSM6DS0 is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope. ST’s family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM6DS0 has a full-scale acceleration range of ±2/±4/±8/±16 *g* and an angular rate range of ±245/±500/±2000 dps. The LSM6DS0 has two operating modes in that the accelerometer and gyroscope sensors can be either activated at the same ODR or the accelerometer can be enabled while the gyroscope is in power-down.

The LSM6DS0 is available in a plastic land grid array (LGA) package.

Table 1. Device summary

Part number	Temp. range [°C]	Package	Packing
LSM6DS0	-40 to +85	LGA-16L (3x3x0.86 mm)	Tray
LSM6DS0TR	-40 to +85		Tape and reel

Contents

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1 Pin description

Figure 1. Pin connections

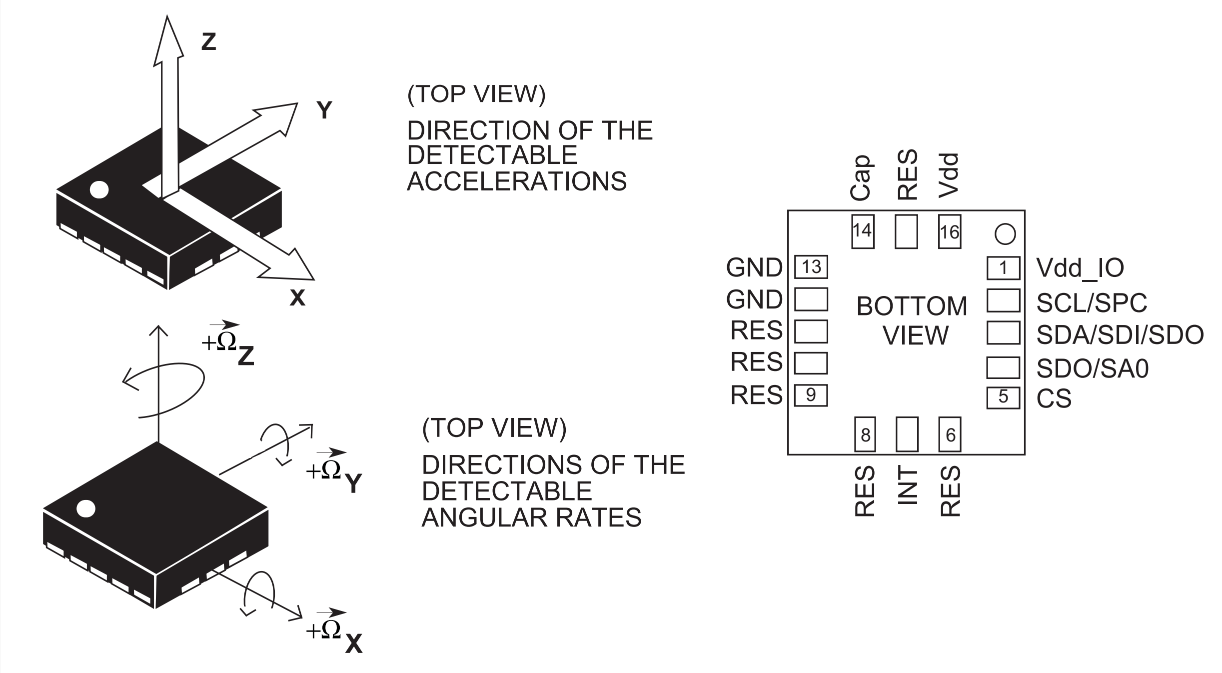


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO(1)	Power supply for I/O pins
2	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
3	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO SA0	SPI serial data output (SDO) I^2C least significant bit of the device address (SA0)
5	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
6	RES	Leave unconnected
7	INT	Programmable interrupt
8	RES	Connect to GND
9	RES	Connect to GND
10	RES	Connect to GND
11	RES	Connect to Vdd or GND
12	GND	0 V supply
13	GND	0 V supply
14	Cap	Connect to GND with ceramic capacitor(2)
15	RES	Connect to Vdd or GND
16	Vdd(3)	Power supply

1. Recommended 100 nF filter capacitor.
2. 10 nF (±10%), 16 V. 1 nF minimum value has to be guaranteed under 11 V bias condition.
3. Recommended 100 nF plus 10 µF capacitors.

2 Module specifications

2.1 Mechanical characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted[a]

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range			±2		*g*
				±4		
				±8		
				±16		
G_FS	Angular rate measurement range			±245		dps
				±500		
				±2000		
LA_So	Linear acceleration sensitivity	FS = ±2 *g*		0.061		mg/LSb
		FS = ±4 *g*		0.122		
		FS = ±8 *g*		0.244		
		FS = ±16 *g*		0.732		
G_So	Angular rate sensitivity	FS = ±245 dps		8.75		mdps/LSb
		FS = ±500 dps		17.50		
		FS = ±2000 dps		70		
LA_TyOff	Linear acceleration typical zero-*g* level offset accuracy[2]	FS = ±8 *g*		±90		m*g*
G_TyOff	Angular rate typical zero-rate level[3]	FS = ±2000 dps		±30		dps
LA_ODR	Linear acceleration output data rate	Gyro ON		952 476 238 119 59.5 14.9		Hz
		Gyro OFF		952 476 238 119 50 10		Hz

a. The product is factory calibrated at 2.2 V. The operational power supply range is from 1.71 V to 3.6 V.

Table 3. Mechanical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
G_ODR	Angular digital output data rate			952 476 238 119 59.5 14.9		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Typical zero-g level offset value after soldering.
3. Typical zero-rate level offset value after MSL3 preconditioning.

2.2 Electrical characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
Vdd	Supply voltage		1.71		3.6	V
Vdd_IO	Power supply for I/O		1.71		Vdd + 0.1	V
LA_Idd	Accelerometer current consumption in normal mode	ODR = 10 Hz		60		µA
		ODR = 50 Hz		160		
		ODR ≥ 119 Hz		330		
G_Idd	Gyroscope current consumption in normal mode			4.0		mA
Top	Operating temperature range		-40		+85	°C
Trise	Time for power supply rising[2]		0.01		100	ms
Twait	Time delay between Vdd_IO and Vdd [2]		0		10	ms

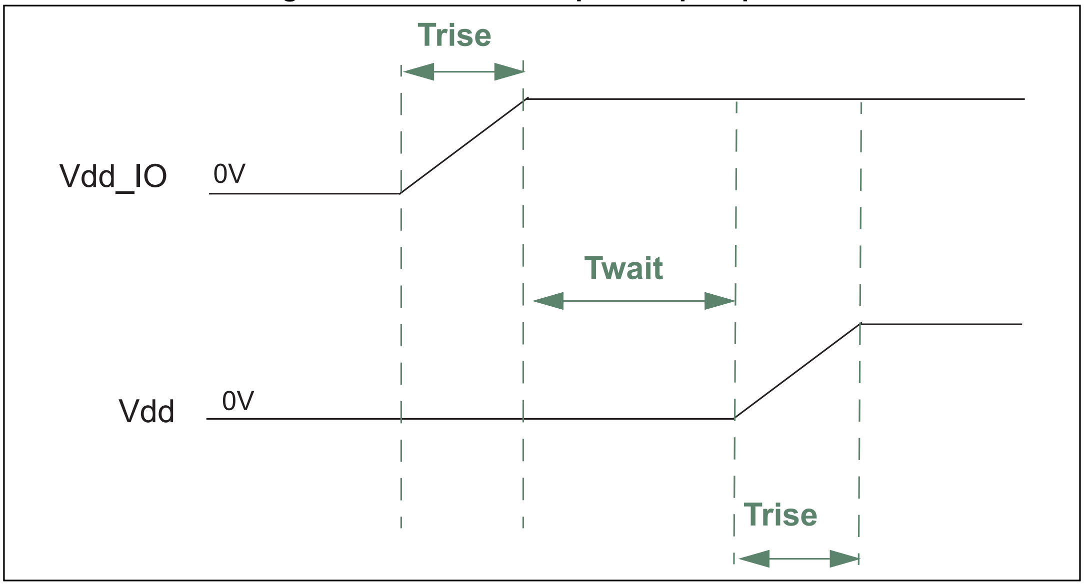
1. Typical specifications are not guaranteed.
2. Please refer to *Section 2.2.1: Recommended power-up sequence* for more details.

2.2.1 Recommended power-up sequence

For the power-up sequence please refer to the following figure, where:

- Trise is the time for the power supply to rise from 10% to 90% of its final value
- Twait is the time delay between the end of the Vdd_IO ramp (90% of its final value) and the start of the Vdd ramp

Figure 2. Recommended power-up sequence



2.3 Temperature sensor characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted [b]

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
TODR	Temperature refresh rate	Gyro off[2]		50		Hz
		Gyro on		59.5		
TSen	Temperature sensitivity[3]			16		LSB/°C
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. When the accelerometer ODR is set to 10 Hz and the gyroscope part is turned off, the TODR value is 10 Hz.
3. The output of the temperature sensor is 0 (typ.) at 25°C

b. The product is factory calibrated at 2.2 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

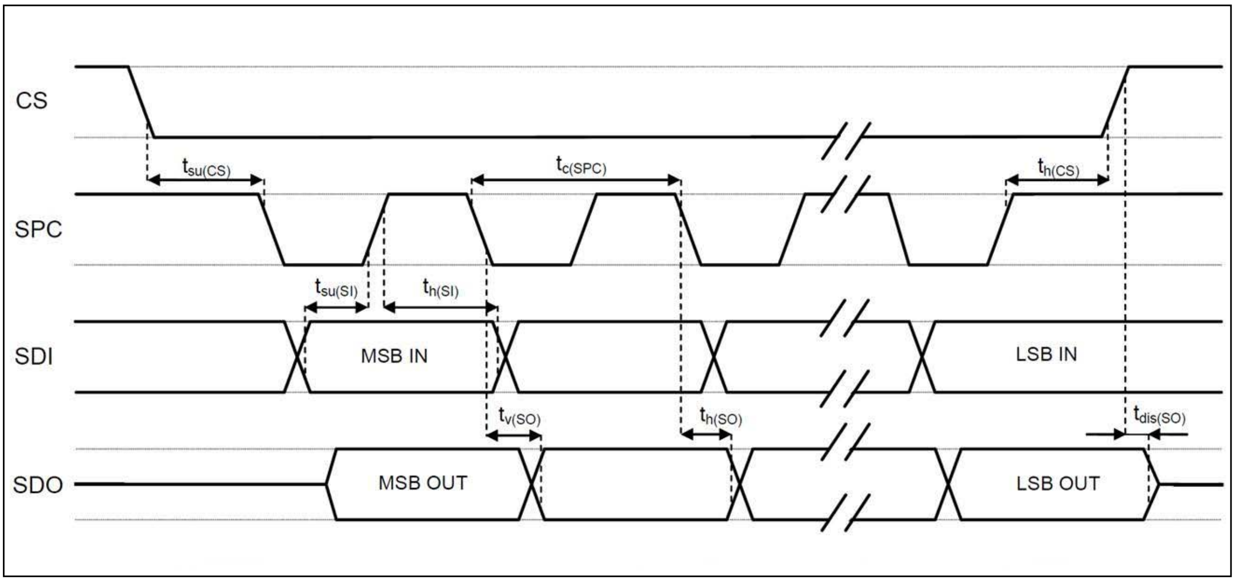
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value[1] Min	Value[1] Max	Unit
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I^2C - inter-IC control interface

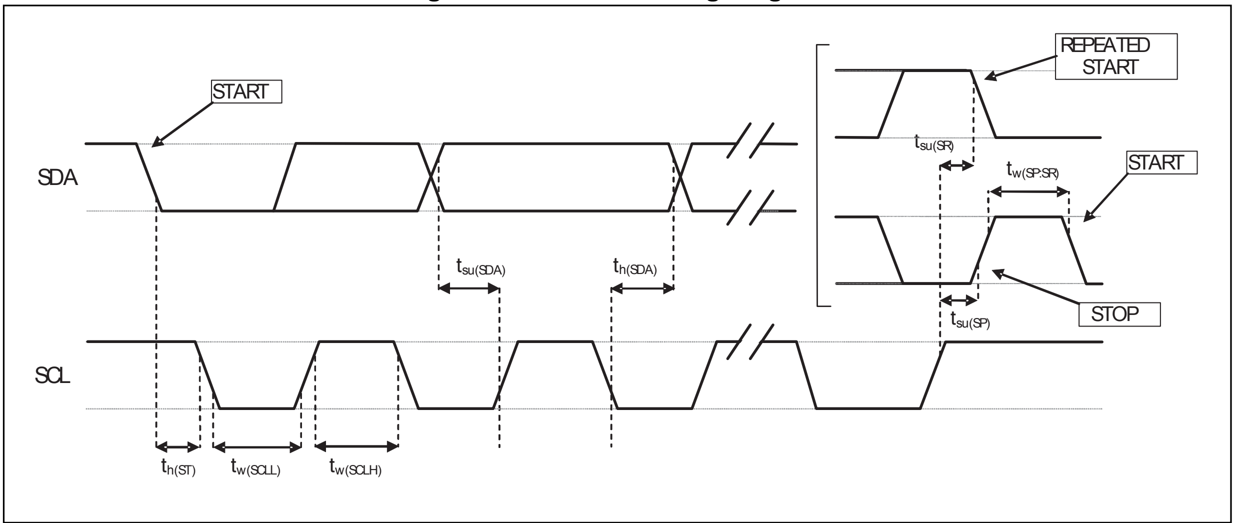
Subject to general operating conditions for Vdd and Top.

Table 7. I^2C slave timing values

Symbol	Parameter	I^2C Standard mode(1)		I^2C Fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		µs
$t_{su(SP)}$	STOP condition setup time	4		0.6		µs
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		µs

1. Data based on standard I^2C protocol requirement, not tested in production.

Figure 4. I^2C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration *g* for 0.1 ms	10,000	*g*
ESD	Electrostatic discharge protection (HBM)	2	kV
Vin	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.6 Terminology

2.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the considered axis. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

2.6.2 Zero-*g* and zero rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X-axis and Y-axis, whereas the Z-axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in *Table 3*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

The zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

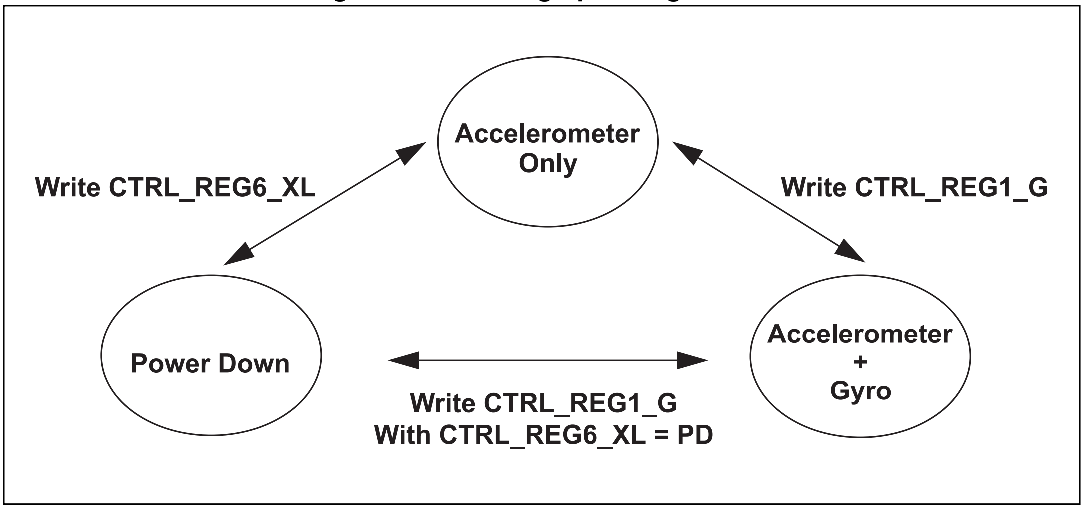
3 Functionality

3.1 Operating modes

The LSM6DS0 has two operating modes available: only accelerometer active and gyroscope in power-down or both accelerometer and gyroscope sensors active at the same ODR. Switching from one mode to the other requires one write operation: writing to *CTRL_REG6_XL (20h)*, the accelerometer operates in normal mode and the gyroscope is powered down, writing to *CTRL_REG1_G (10h)* both the accelerometer and gyroscope are activated at the same ODR.

Figure 5 depicts both modes of operation from power down.

Figure 5. Switching operating modes



3.2 Gyroscope power modes

In the LSM6DS0, the gyroscope can be configured in three different operating modes: power-down, low-power and normal mode.

Low-power mode is available for lower ODR (14.9, 59.5, 119 Hz) while for greater ODR (238, 476, 952 Hz) the device is automatically in normal mode. *Table 9* summarizes the ODR configuration (ODR_G[2:0] bits set in *CTRL_REG1_G (10h)*) and the corresponding power modes.

To enable low-power mode, the LP_mode bit in *CTRL_REG3_G (12h)* has to be set to ‘1’.

Low-power mode allows reaching low-power consumption while maintaining the device always on, refer to *Table 10*.

Table 9. Gyroscope operating modes

ODR_G [2:0]	ODR [Hz]	Power mode(1)
000	Power-down	Power-down
001	14.9	Low-power/Normal mode
010	59.5	Low-power/Normal mode
011	119	Low-power/Normal mode
100	238	Normal mode
101	476	Normal mode
110	952	Normal mode

1. Gyroscope low-power mode is available for G_FS = ±2000 dps.

Table 10. Operating mode current consumption

ODR [Hz]	Power mode	Current consumption(1) [mA]
14.9	Low-power	1.8
59.5	Low-power	2.3
119	Low-power	2.9
238	Normal mode	4.3
476	Normal mode	4.3
952	Normal mode	4.3

1. Typical values of gyroscope and accelerometer current consumption are based on characterization data

Table 11. Accelerometer turn-on time

ODR [Hz]	BW = 400 Hz(1)	BW = 200 Hz(1)	BW = 100 Hz(1)	BW = 50 Hz(1)
14.9	0	0	0	0
59.5	0	0	0	0
119	1	1	1	2
238	1	1	2	4
476	1	2	4	7
952	2	4	7	14

1. The table contains the number of samples to be discarded after switching between power-down mode and normal mode.

Table 12. Gyroscope turn-on time

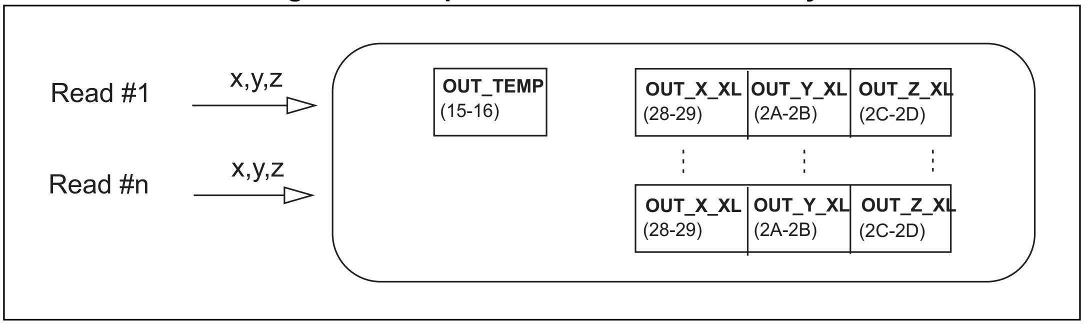
ODR [Hz]	LPF1 only(1)	LPF1 and LPF2(1)
14.9	2	LPF2 not available
59.5 or 119	3	13
238	4	14
476	5	15
952	8	18

1. The table contains the number of samples to be discarded after switching between low-power mode and normal mode.

3.3 Multiple reads (burst)

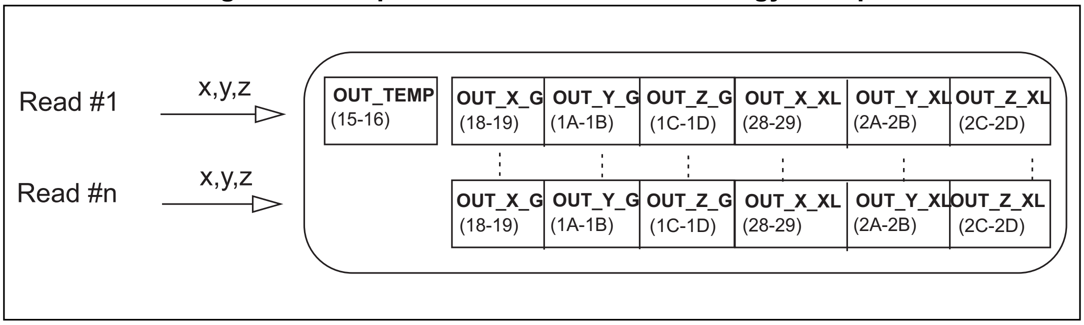
When only the accelerometer is activated and the gyroscope is in power down, starting from *OUT_X_XL (28h - 29h)* multiple reads can be performed. Once *OUT_Z_XL (2Ch - 2Dh)* is read, the system automatically restarts from *OUT_X_XL (28h - 29h)* (see *Figure 6*).

Figure 6. Multiple reads: accelerometer only



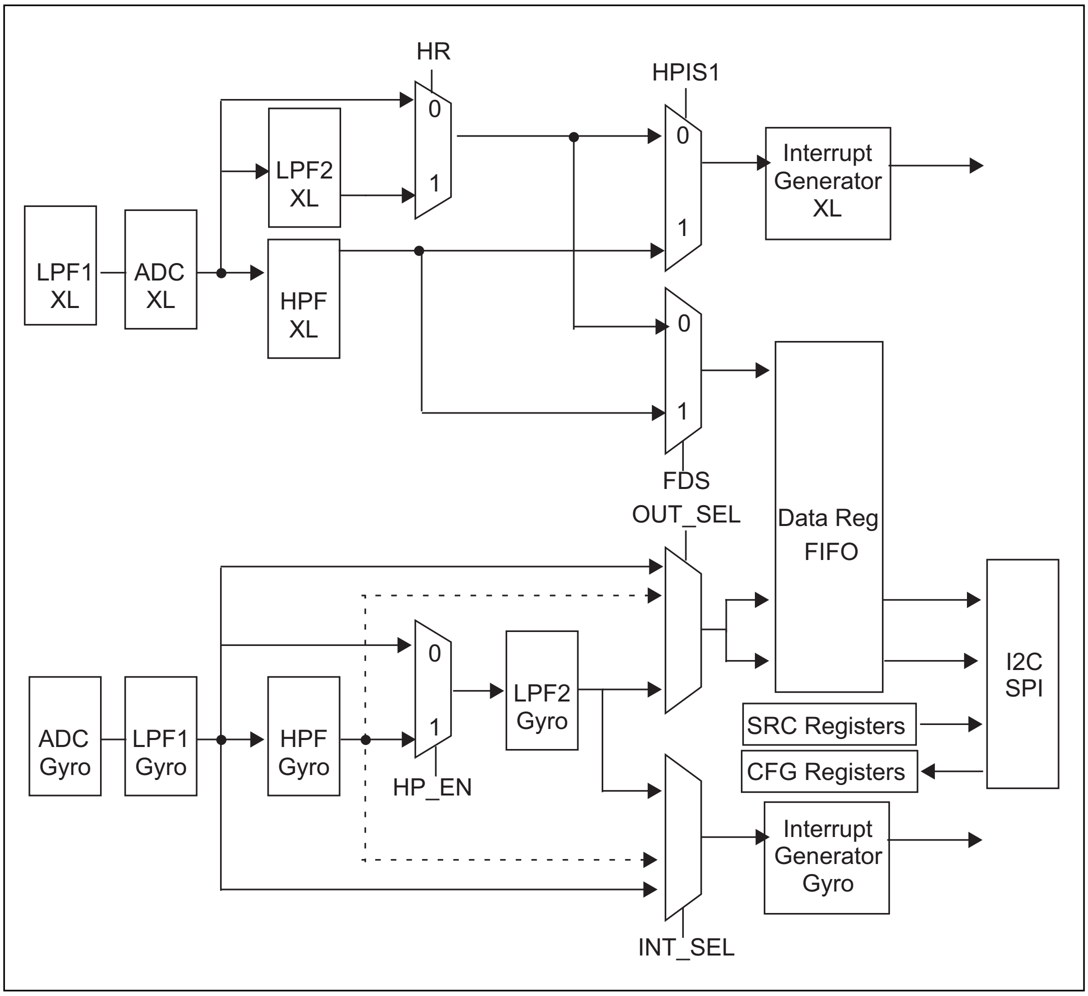
When both accelerometer and gyroscope sensors are activated at the same ODR, starting from *OUT_X_G (18h - 19h)* multiple reads can be performed. Once *OUT_Z_XL (2Ch - 2Dh)* is read, the system automatically restarts from *OUT_X_G (18h - 19h)* (see *Figure 7*).

Figure 7. Multiple reads: accelerometer and gyroscope



3.4 Digital block diagram

Figure 8. Digital block diagram



3.5 FIFO

The LSM6DS0 embeds 32 slots of 16-bit data FIFO for each of the gyroscope's three output channels, yaw, pitch and roll, and 16-bit data FIFO for each of the accelerometer's three output channels, X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly to five different modes: Bypass mode, FIFO-mode, Continuous mode, Continuous-to-FIFO mode and Bypass-to-Continuous. Each mode is selected by the FMODE [2:0] bits in the *FIFO_CTRL (2Eh)* register. Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_SRC (2Fh)* register and can be set to generate dedicated interrupts on the INT pin using the *INT_CTRL (0Ch)* register.

FIFO_SRC (2Fh)(FTH) goes to '1' when the number of unread samples (*FIFO_SRC (2Fh)* (FSS5:0)) is greater than or equal to FTH [4:0] in *FIFO_CTRL (2Eh)*. If *FIFO_CTRL (2Eh)* (FTH[4:0]) is equal to 0, *FIFO_SRC (2Fh)*(FTH) goes to '0'.

FIFO_SRC (2Fh)(OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO_SRC (2Fh)(FSS [5:0]) contains stored data levels of unread samples. When FSS [5:0] is equal to '000000', FIFO is empty. When FSS [5:0] is equal to '100000', FIFO is full and the unread samples are 32.

The FIFO feature is enabled by writing '1' in *CTRL_REG9 (23h)* (FIFO_EN).

To guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

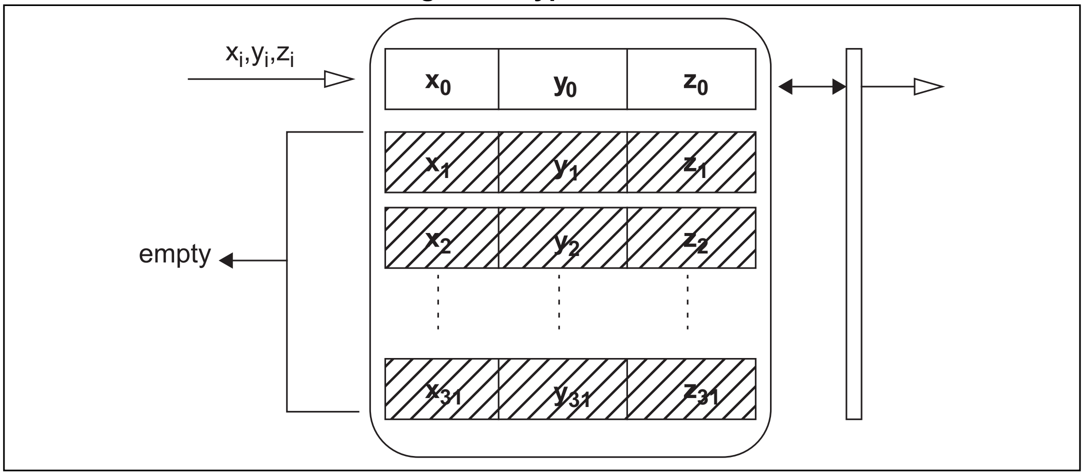
3.5.1 Bypass mode

In Bypass mode (*FIFO_CTRL (2Eh)*(FMODE [2:0]= 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

As described in *Figure 9*, for each channel only the first address is used. When new data is available the old data is overwritten.

Figure 9. Bypass mode



3.5.2 FIFO mode

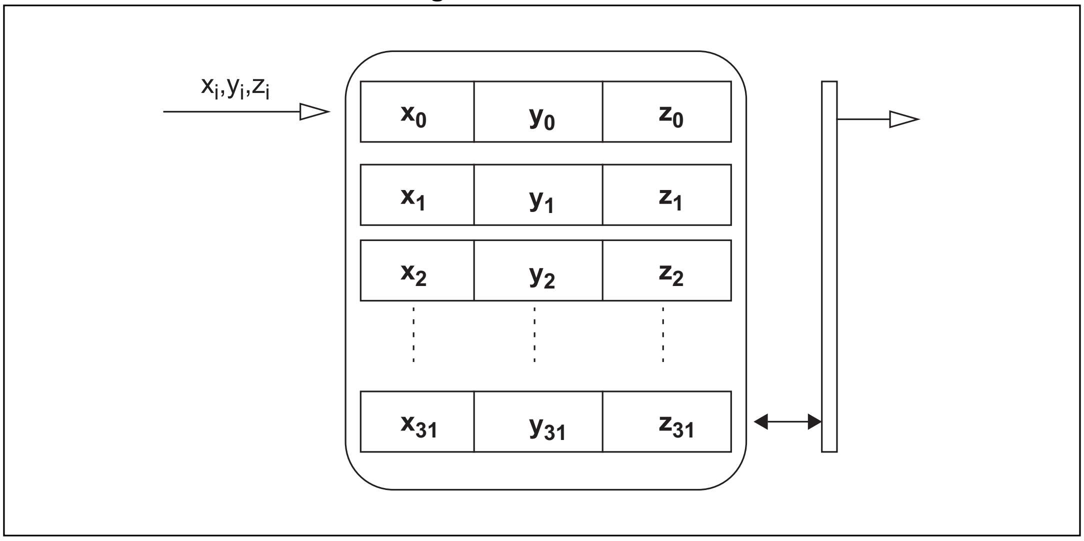
In FIFO mode (*FIFO_CTRL (2Eh)* (FMODE [2:0] = 001) data from the output channels are stored in the FIFO until it is overwritten.

To reset FIFO content, Bypass mode should be selected by writing *FIFO_CTRL (2Eh)* (FMODE [2:0]) to '000'. After this reset command, it is possible to restart FIFO mode, writing *FIFO_CTRL (2Eh)* (FMODE [2:0]) to '001'.

The FIFO buffer memorizes 32 levels of data, but the depth of the FIFO can be resized by setting the STOP_ON_FTH bit in *CTRL_REG9 (23h)*. If the STOP_ON_FTH bit is set to '1', FIFO depth is limited to *FIFO_CTRL (2Eh)*(FTH [4:0]) + 1 data.

A FIFO threshold interrupt can be enabled (INT_OVR bit in *INT_CTRL (0Ch)*) in order to be raised when the FIFO is filled to the level specified by the FTH[4:0] bits of *FIFO_CTRL (2Eh)*. When a FIFO threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

Figure 10. FIFO mode



3.5.3 Continuous mode

Continuous mode (*FIFO_CTRL (2Eh)* (FMODE[2:0] = 110) provides a continuous FIFO update: as new data arrives the older is discarded.

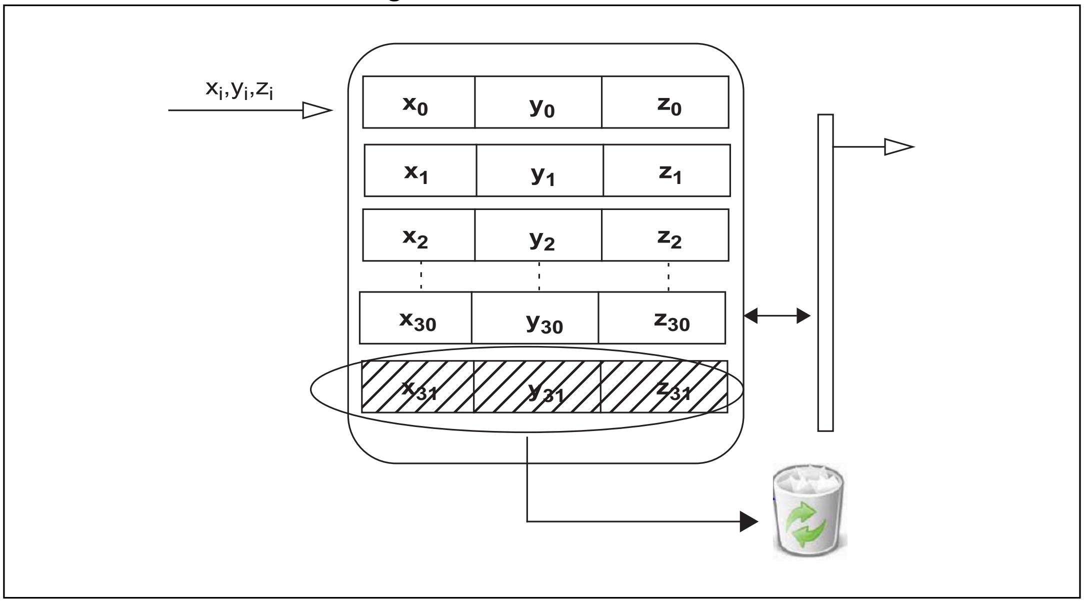
A FIFO threshold flag *FIFO_SRC (2Fh)*(FTH) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO_CTRL (2Eh)*(FTH4:0).

It is possible to route *FIFO_SRC (2Fh)*(FTH) to the INT pin by writing the INT_FTH bit to '1' in register *INT_CTRL (0Ch)*.

A full-flag interrupt can be enabled (*INT_CTRL (0Ch)* (INT_ FSS5)= '1') when the FIFO becomes saturated and in order to read the contents all at once. If an overrun occurs, the oldest sample in FIFO is overwritten and the OVRN flag in *FIFO_SRC (2Fh)* is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in *FIFO_SRC (2Fh)* (FSS[5:0]).

Figure 11. Continuous mode



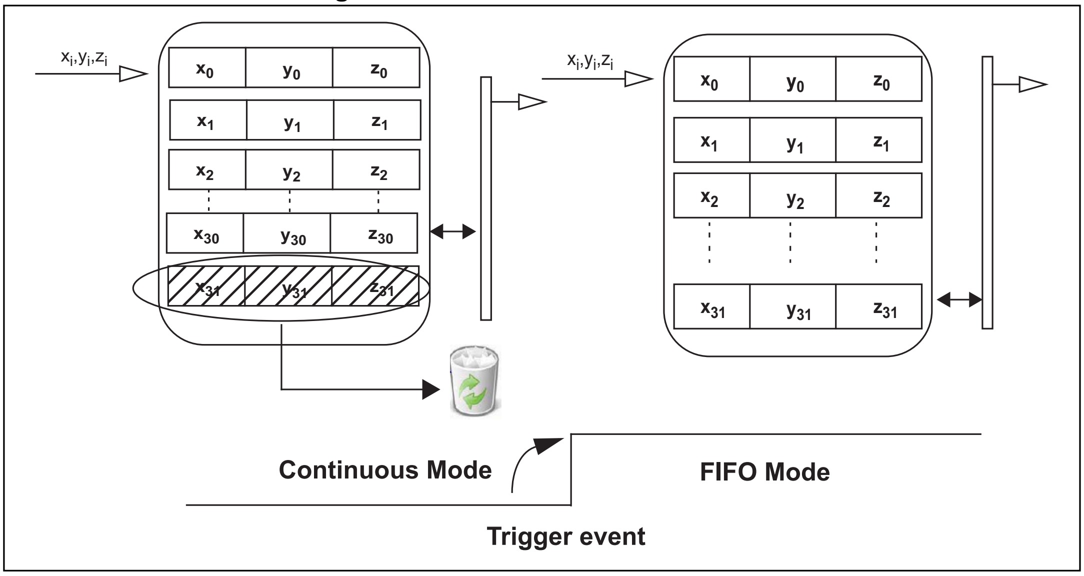
3.5.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode (*FIFO_CTRL (2Eh)*(FMODE [2:0] = 011), FIFO behavior changes according to the *INT_GEN_SRC_XL (26h)*(IA_XL) bit. When the *INT_GEN_SRC_XL (26h)*(IA_XL) bit is equal to '1', FIFO operates in FIFO mode. When the *INT_GEN_SRC_XL (26h)*(IA_XL) bit is equal to '0', FIFO operates in Continuous mode.

The interrupt generator should be set to the desired configuration by means of *INT_GEN_CFG_XL (06h)*, *INT_GEN_THS_X_XL (07h)*, *INT_GEN_THS_Y_XL (08h)* and *INT_GEN_THS_Z_XL (09h)*.

The *CTRL_REG4 (1Eh)*(LIR_XL) bit should be set to '1' in order to have latched interrupt.

Figure 12. Continuous-to-FIFO mode



3.5.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO_CTRL (2Eh)*(FMODE[2:0] = '100'), data measurement storage inside FIFO operates in Continuous mode when *INT_GEN_SRC_XL (26h)*(IA_XL) is equal to '1', otherwise FIFO content is reset (Bypass mode).

The interrupt generator should be set to the desired configuration by means of *INT_GEN_CFG_XL (06h)*, *INT_GEN_THS_X_XL (07h)*, *INT_GEN_THS_Y_XL (08h)* and *INT_GEN_THS_Z_XL (09h)*.

The *CTRL_REG4 (1Eh)*(LIR_XL) bit should be set to '1' in order to have latched interrupt.

Figure 13. Bypass-to-Continuous mode