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N-channel 80 V, 3.5 mΩ typ., 64 A STripFET™ F7 Power MOSFET in a TO-220FP package

Datasheet - production data

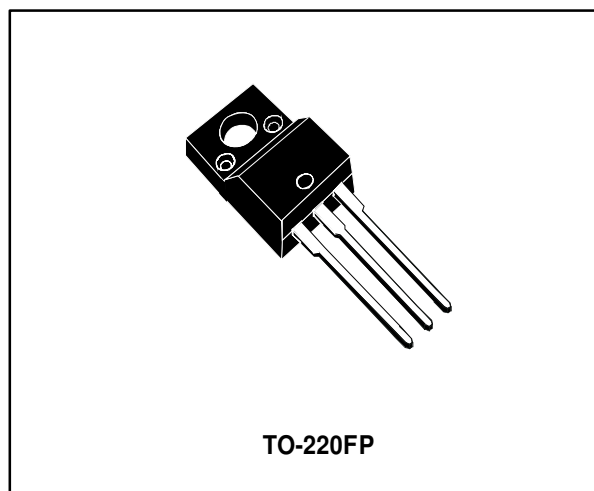
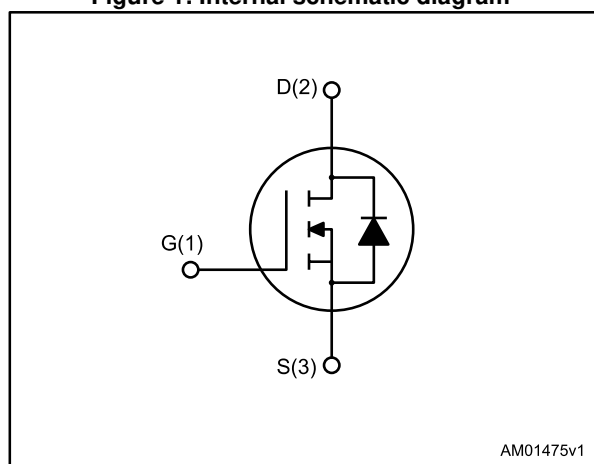


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STF140N8F7	80 V	4.3 mΩ	64 A	35 W

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STF140N8F7	140N8F7	TO-220FP	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	64 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	45 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	256	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	35	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	515	mJ
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ }^\circ\text{C}$)	2.5	kV
T_j	Operating junction temperature	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature		

Notes:

⁽¹⁾Limited by package.

⁽²⁾Pulse width is limited by safe operating area.

⁽³⁾Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 18.5\text{ A}$, $V_{DD} = 50\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	4.29	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C/W}$

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 250 μA	80			V
I _{DSS}	Zero gate voltage Drain current	V _{GS} = 0, V _{DS} = 80 V			1	μA
		V _{GS} = 0, V _{DS} = 80 V, T _J = 125 °C			10	μA
I _{GSS}	Gate-source leakage current	V _{DS} = 0, V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.5		4.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 32 A		3.5	4.3	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{GS} = 0, V _{DS} = 40 V, f = 1 MHz	-	6340	-	pF
C _{OSS}	Output capacitance		-	1195	-	pF
C _{rSS}	Reverse transfer capacitance		-	105	-	pF
Q _g	Total gate charge	V _{DD} = 40 V, I _D = 64 A, V _{GS} = 10 V	-	96	-	nC
Q _{gs}	Gate-source charge		-	30	-	nC
Q _{gd}	Gate-drain charge		-	26	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 40 V, I _D = 45 A R _G = 4.7 Ω, V _{GS} = 10 V	-	26	-	ns
t _r	Rise time		-	51	-	ns
t _{d(off)}	Turn-off-delay time		-	82	-	ns
t _f	Fall time		-	44	-	ns

Table 7: Source drain diode

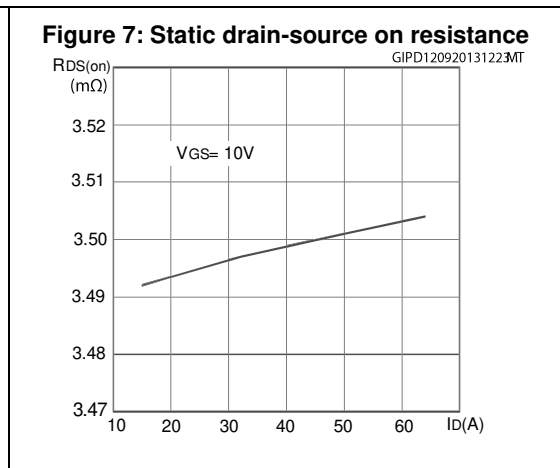
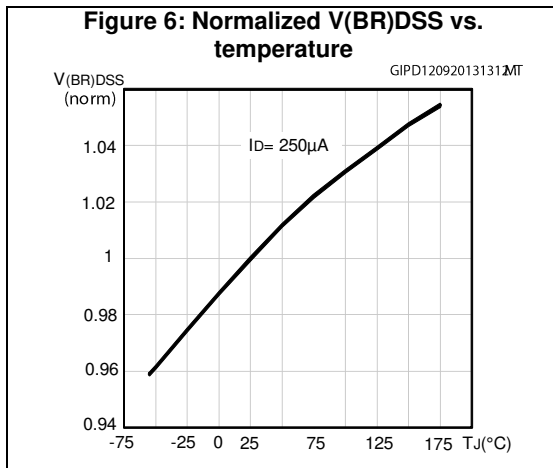
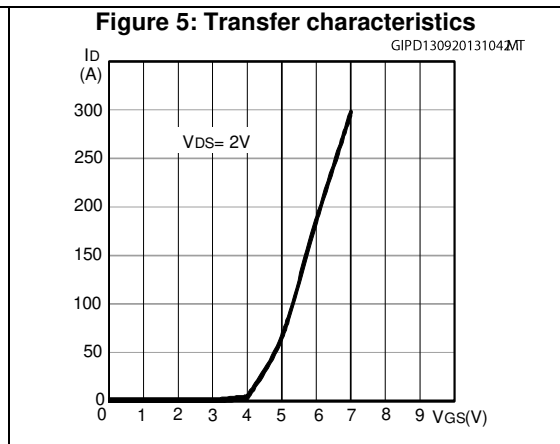
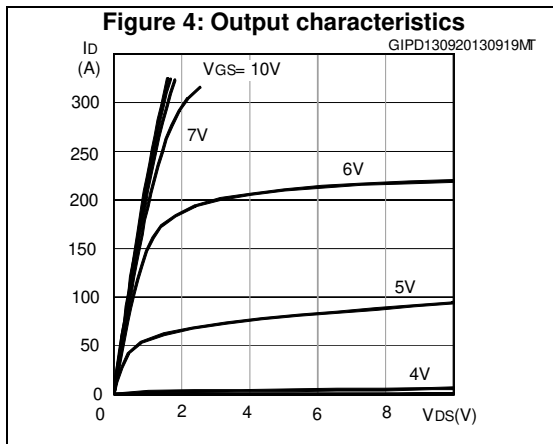
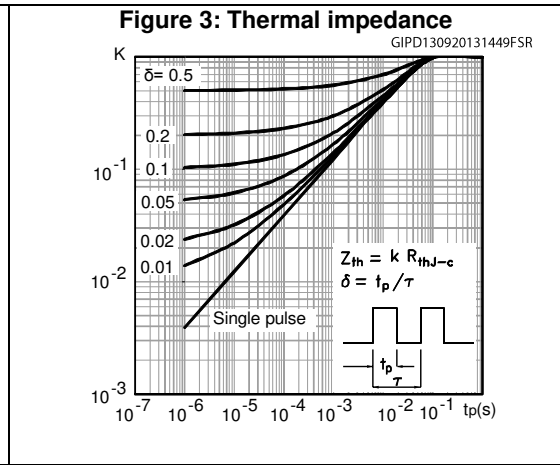
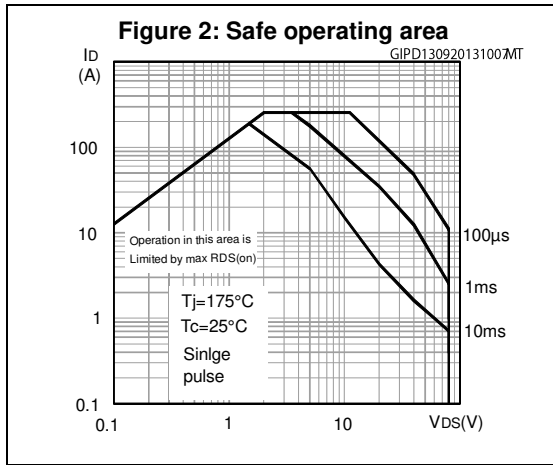
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SD}	Source-drain current		-		64	A
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		256	A
V _{SD} ⁽²⁾	Forward on voltage	V _{GS} = 0, I _{SD} = 64 A	-		1.2	V
t _{rr}	Reverse recovery time	I _{SD} = 64 A, di/dt = 100 A/μs, V _{DD} = 60 V, T _J = 150 °C	-	58		ns
Q _{rr}	Reverse recovery charge		-	92		nC
I _{RRM}	Reverse recovery current		-	3.2		A

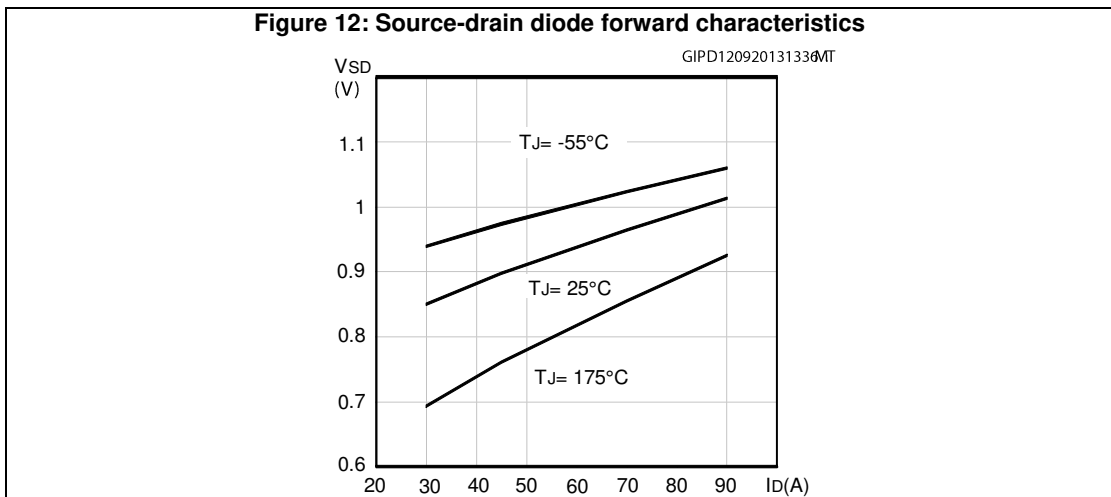
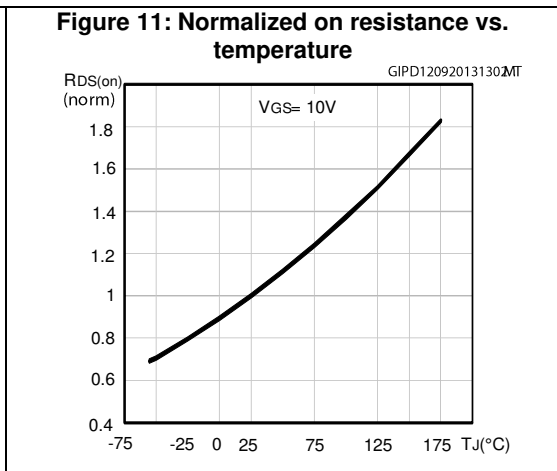
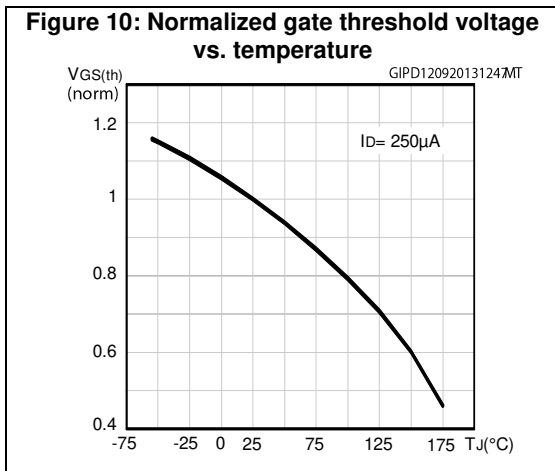
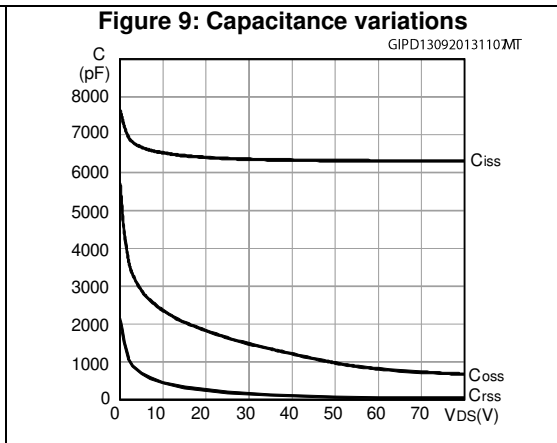
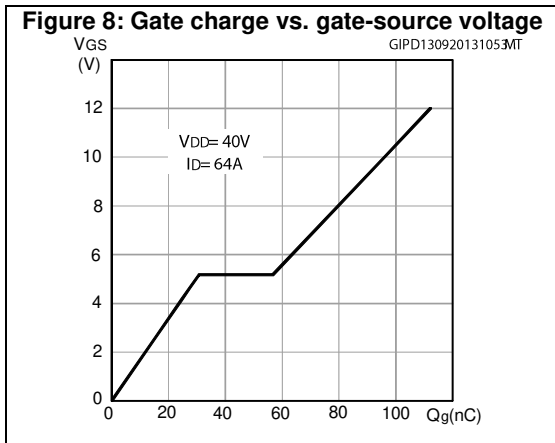
Notes:

⁽¹⁾Pulse width is limited by safe operating area

⁽²⁾Pulse test: pulse duration = 300 μs, duty cycle 1.5%

2.1 Electrical characteristics (curves)





3 Test circuits

Figure 13: Switching times test circuit for resistive load

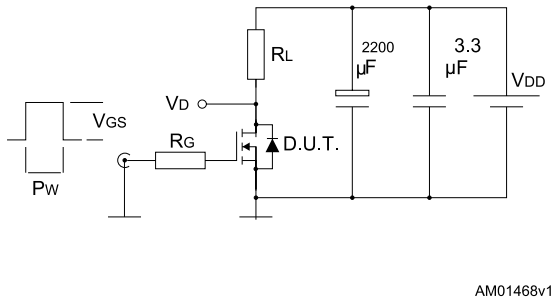


Figure 14: Gate charge test circuit

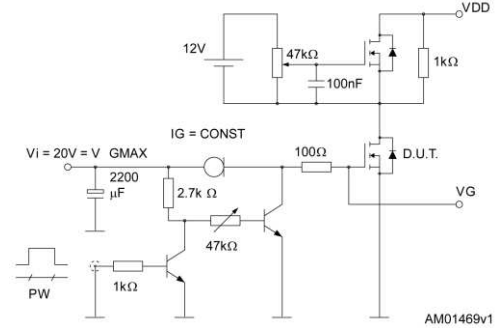


Figure 15: Test circuit for inductive load switching and diode recovery times

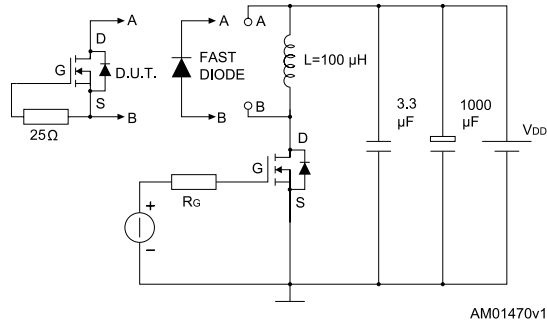


Figure 16: Unclamped inductive load test circuit

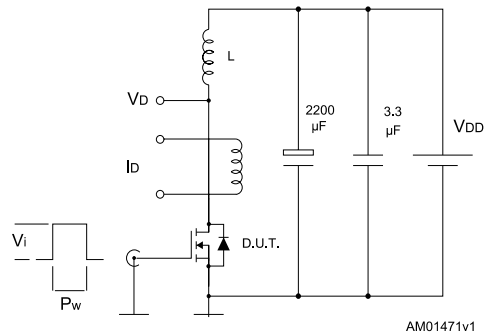


Figure 17: Unclamped inductive waveform

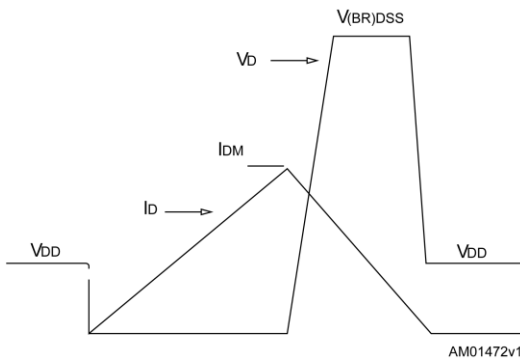
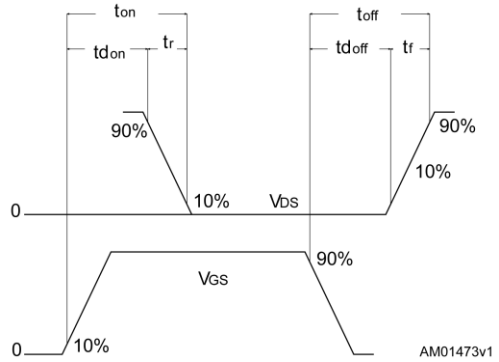


Figure 18: Switching time waveform

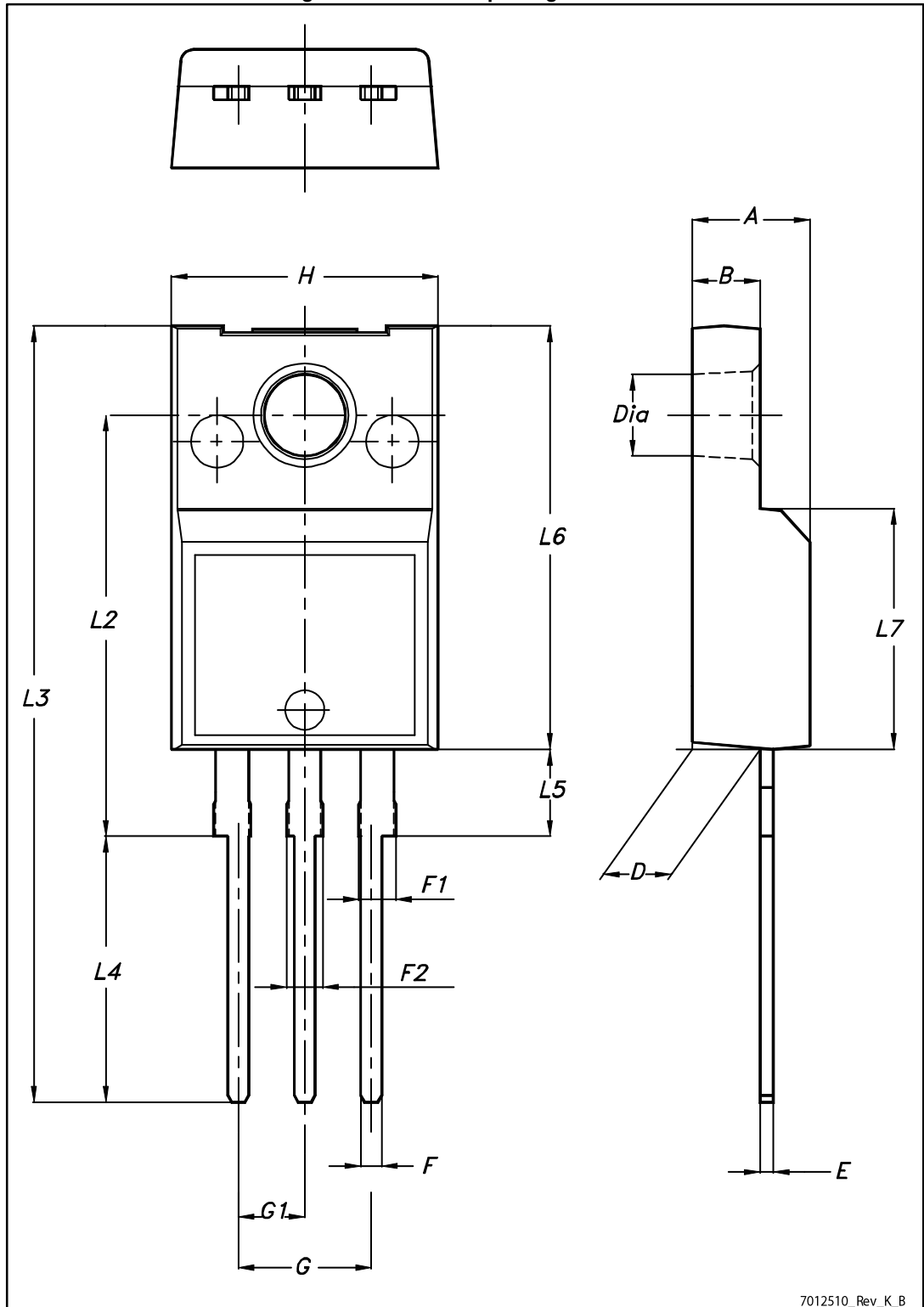


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 19: TO-220FP package outline



7012510_Rev_K_B

Table 8: TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
18-Sep-2013	1	First release.
22-Aug-2014	2	<ul style="list-style-type: none">• The part numbers STH140N8F7-2 and STP140N8F7 have been moved to a separate datasheet.• Modified: not found• Minor text changes
10-Oct-2014	3	<ul style="list-style-type: none">• Updated <i>Figure 3: "Thermal impedance"</i>

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