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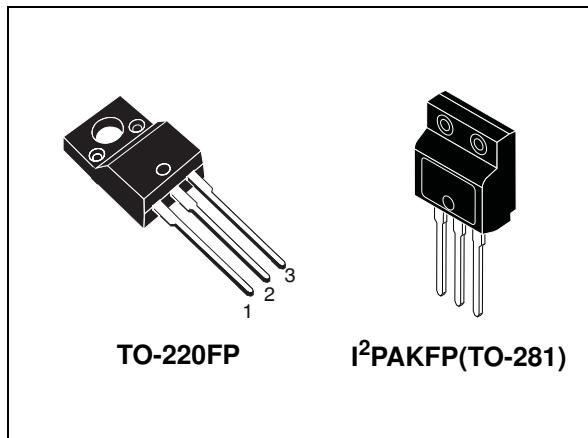
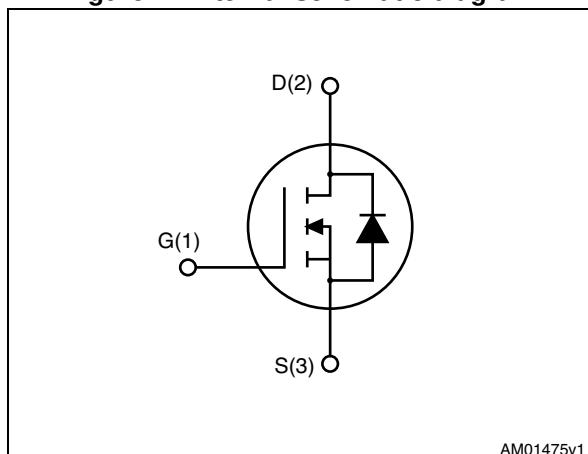


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**Figure 1. Internal schematic diagram**


## Features

| Order codes | $V_{DS} @ T_{Jmax}$ | $R_{DS(on)} \text{ max}$ | $I_D$ |
|-------------|---------------------|--------------------------|-------|
| STF34N65M5  | 710 V               | 0.11 $\Omega$            | 28 A  |
| STFI34N65M5 |                     |                          |       |

- Worldwide best  $R_{DS(on)}$  \* area
- Higher  $V_{DSS}$  rating and high dv/dt capability
- Excellent switching performance
- 100% avalanche tested

## Applications

- Switching applications

## Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

**Table 1. Device summary**

| Order codes | Marking | Packages                      | Packaging |
|-------------|---------|-------------------------------|-----------|
| STF34N65M5  | 34N65M5 | TO-220FP                      | Tube      |
| STFI34N65M5 |         | I <sup>2</sup> PAKFP (TO-281) |           |

## Contents

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# 1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol         | Parameter  | Value               | Unit             |
|----------------|--|---------------------|------------------|
| $V_{GS}$       | Gate-source voltage  | $\pm 25$            | V                |
| $I_D$          | Drain current (continuous) at $T_C = 25^\circ\text{C}$   | 28 <sup>(1)</sup>   | A                |
| $I_D$          | Drain current (continuous) at $T_C = 100^\circ\text{C}$  | 17.7 <sup>(1)</sup> | A                |
| $I_{DM}^{(1)}$ | Drain current (pulsed)   | 112 <sup>(1)</sup>  | A                |
| $P_{TOT}$      | Total dissipation at $T_C = 25^\circ\text{C}$  | 35                  | W                |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope  | 15                  | V/ns             |
| $dv/dt^{(3)}$  | MOSFET dv/dt ruggedness  | 50                  | V/ns             |
| $V_{ISO}$      | Insulation withstand voltage (RMS) from all three leads to external heat sink<br>( $t = 1\text{ s}$ ; $T_C = 25^\circ\text{C}$ ) | 2500                | V                |
| $T_{stg}$      | Storage temperature  | -55 to 150          | $^\circ\text{C}$ |
| $T_j$          | Max. operating junction temperature  | 150                 | $^\circ\text{C}$ |

1. Limited by maximum junction temperature.
2.  $I_{SD} \leq 28\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS}$  peak <  $V_{(BR)DSS}$ ,  $V_{DD}=400\text{ V}$ .
3.  $V_{DS} \leq 480\text{ V}$

Table 3. Thermal data

| Symbol         | Parameter                               | Value | Unit                      |
|----------------|---|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case max    | 3.57  | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$  | Thermal resistance junction-ambient max | 62.5  | $^\circ\text{C}/\text{W}$ |

Table 4. Avalanche characteristics

| Symbol   | Parameter   | Value | Unit |
|----------|---|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive<br>(pulse width limited by $T_{jmax}$ )       | 7     | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$ , $I_d=I_{AR}$ ; $V_{dd}=50$ ) | 510   | mJ   |

## 2 Electrical characteristics

( $T_C = 25^\circ\text{C}$  unless otherwise specified)

Table 5. On /off states

| Symbol                      | Parameter  | Test conditions  | Min. | Typ. | Max.      | Unit                           |
|-----------------------------|--|--|------|------|-----------|--------------------------------|
| $V_{(\text{BR})\text{DSS}}$ | Drain-source breakdown voltage                   | $I_D = 1 \text{ mA}$ , $V_{GS} = 0$  | 650  |      |           | V                              |
| $I_{DSS}$                   | Zero gate voltage drain current ( $V_{GS} = 0$ ) | $V_{DS} = 650 \text{ V}$<br>$V_{DS} = 650 \text{ V}$ , $T_C = 125^\circ\text{C}$ |      |      | 1<br>100  | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$                   | Gate-body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 25 \text{ V}$  |      |      | $\pm 100$ | nA                             |
| $V_{GS(\text{th})}$         | Gate threshold voltage                           | $V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$                                      | 3    | 4    | 5         | V                              |
| $R_{DS(\text{on})}$         | Static drain-source on-resistance                | $V_{GS} = 10 \text{ V}$ , $I_D = 14 \text{ A}$                                   |      | 0.09 | 0.11      | $\Omega$                       |

Table 6. Dynamic

| Symbol                   | Parameter                             | Test conditions   | Min. | Typ. | Max. | Unit     |
|--------------------------|---------------------------------------|---|------|------|------|----------|
| $C_{iss}$                | Input capacitance                     | $V_{DS} = 100 \text{ V}$ , $f = 1 \text{ MHz}$ ,<br>$V_{GS} = 0$                                | -    | 2700 | -    | pF       |
| $C_{oss}$                | Output capacitance                    |   | -    | 75   | -    | pF       |
| $C_{rss}$                | Reverse transfer capacitance          |   | -    | 6.3  | -    | pF       |
| $C_{o(\text{tr})}^{(1)}$ | Equivalent capacitance time related   | $V_{DS} = 0 \text{ to } 520 \text{ V}$ , $V_{GS} = 0$   | -    | 220  | -    | pF       |
| $C_{o(\text{er})}^{(2)}$ | Equivalent capacitance energy related |   | -    | 63   | -    | pF       |
| $R_G$                    | Intrinsic gate resistance             | $f = 1 \text{ MHz}$ open drain  | -    | 1.95 | -    | $\Omega$ |
| $Q_g$                    | Total gate charge                     | $V_{DD} = 520 \text{ V}$ , $I_D = 14 \text{ A}$ ,<br>$V_{GS} = 10 \text{ V}$<br>(see Figure 16) | -    | 62.5 | -    | nC       |
| $Q_{gs}$                 | Gate-source charge                    |   | -    | 17   | -    | nC       |
| $Q_{gd}$                 | Gate-drain charge                     |   | -    | 28   | -    | nC       |

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 7. Switching times

| Symbol            | Parameter          | Test conditions  | Min. | Typ. | Max. | Unit |
|-------------------|--------------------|--|------|------|------|------|
| $t_d(v)$          | Voltage delay time | $V_{DD} = 400 \text{ V}$ , $I_D = 18 \text{ A}$ ,<br>$R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$<br>(see <a href="#">Figure 17</a> and<br><a href="#">Figure 20</a> ) | -    | 59   | -    | ns   |
| $t_r(v)$          | Voltage rise time  |  | -    | 8.7  | -    | ns   |
| $t_f(i)$          | Current fall time  |  | -    | 7.5  | -    | ns   |
| $t_c(\text{off})$ | Crossing time      |  | -    | 12   | -    | ns   |

Table 8. Source drain diode

| Symbol          | Parameter                     | Test conditions  | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|--|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |  | -    |      | 28   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |  | -    |      | 112  | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 28 \text{ A}$ , $V_{GS} = 0$   | -    |      | 1.5  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 28 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$<br>$V_{DD} = 100 \text{ V}$ (see <a href="#">Figure 20</a> )   | -    | 350  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |  | -    | 5.6  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |  | -    | 32   |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 28 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$<br>$V_{DD} = 100 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$<br>(see <a href="#">Figure 20</a> ) | -    | 422  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |  | -    | 7.4  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |  | -    | 35   |      | A             |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

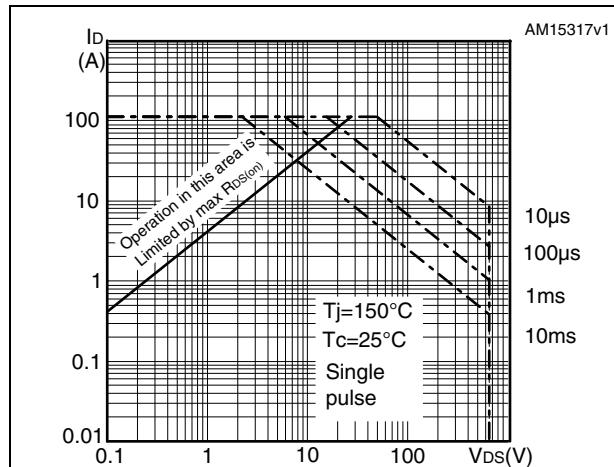


Figure 3. Thermal impedance

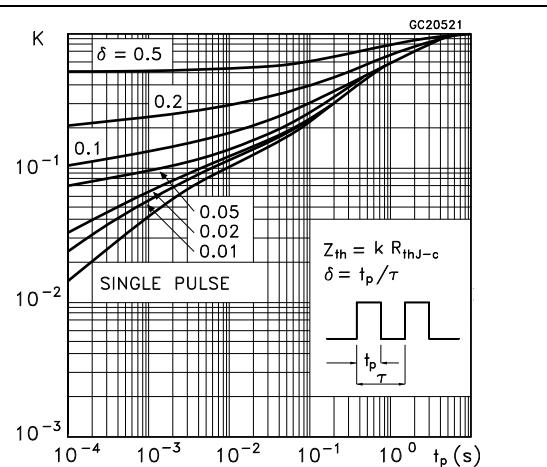


Figure 4. Output characteristics

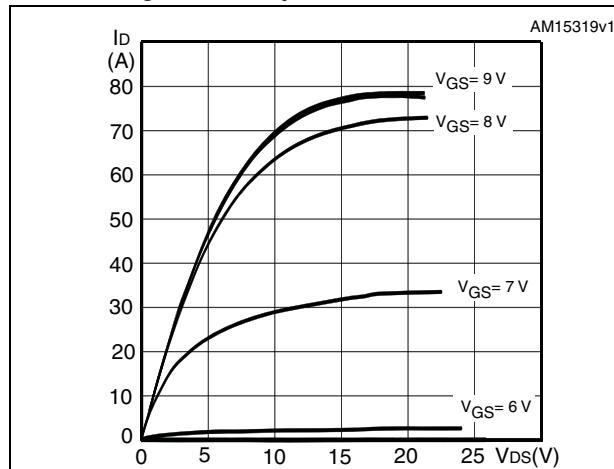


Figure 5. Transfer characteristics

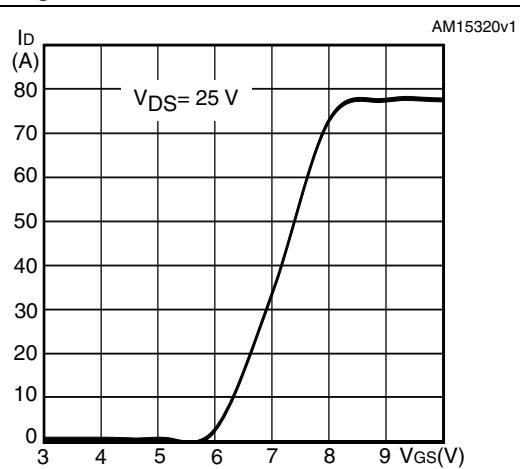


Figure 6. Gate charge vs gate-source voltage

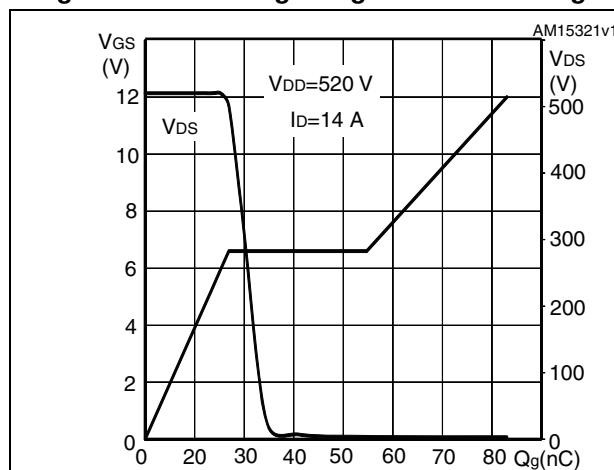


Figure 7. Static drain-source on-resistance

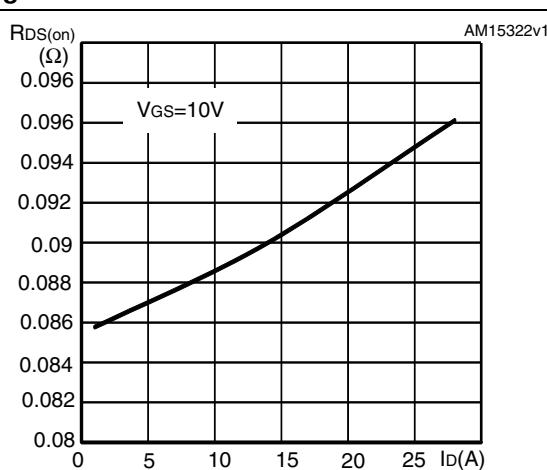


Figure 8. Capacitance variations

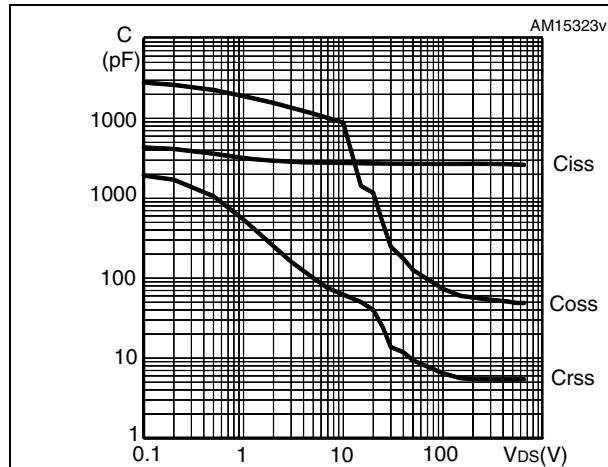


Figure 9. Output capacitance stored energy

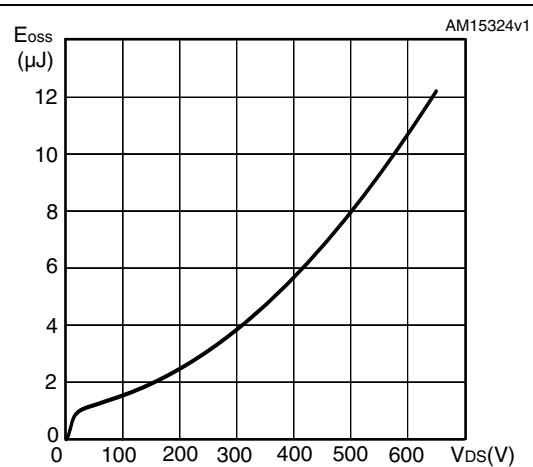


Figure 10. Normalized gate threshold voltage vs temperature

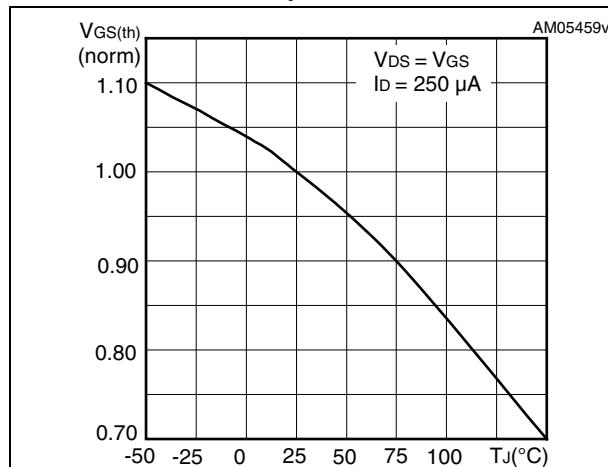


Figure 11. Normalized on-resistance vs temperature

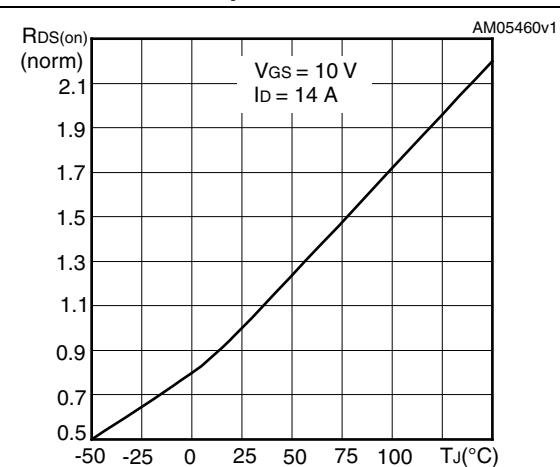


Figure 12. Source-drain diode forward characteristics

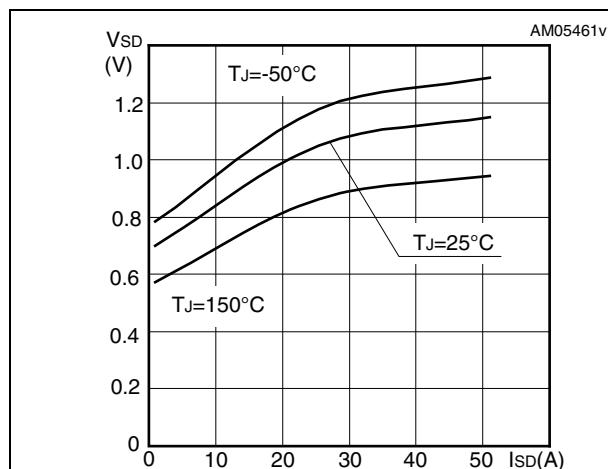
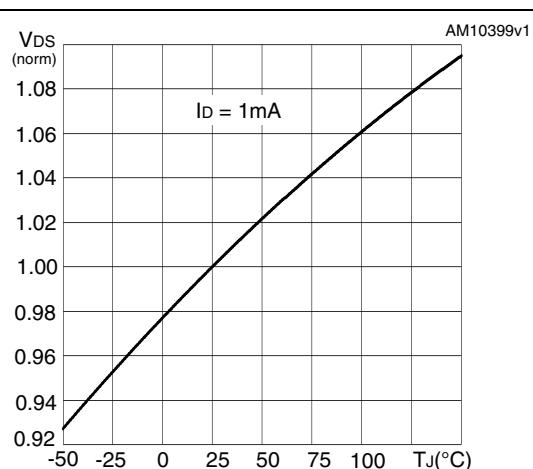
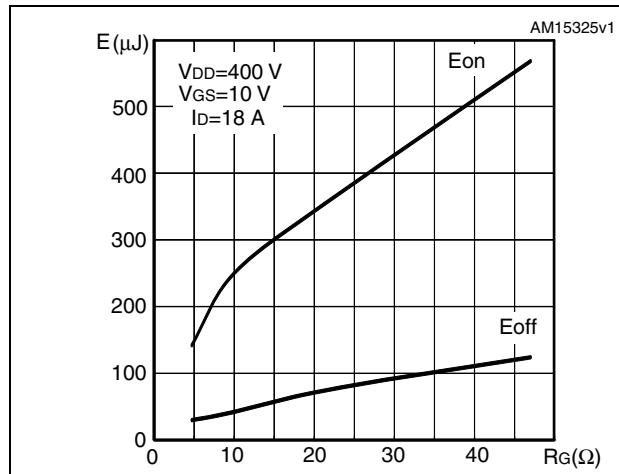


Figure 13. Normalized VDS vs temperature



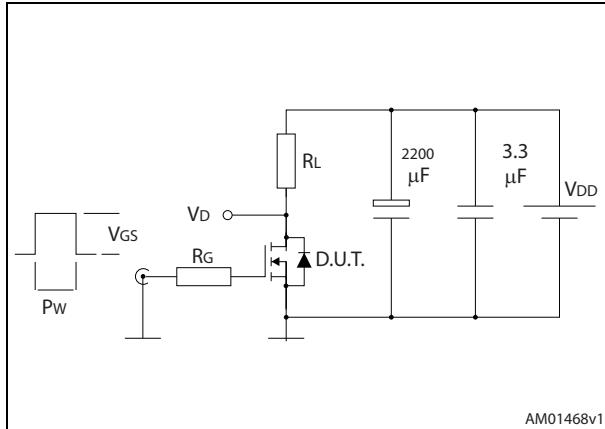
**Figure 14. Switching losses vs gate resistance (1)**



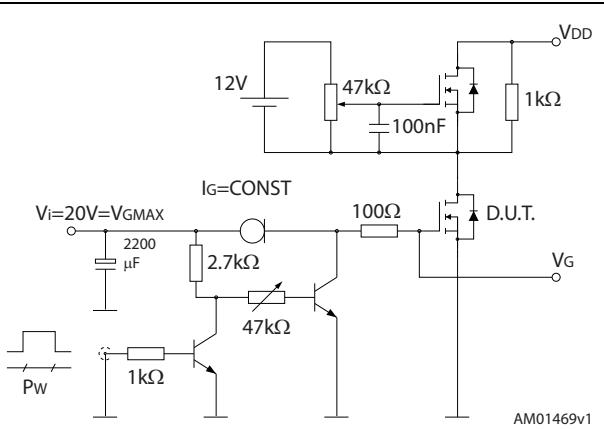
1.  $E_{on}$  including reverse recovery of a SiC diode

### 3 Test circuits

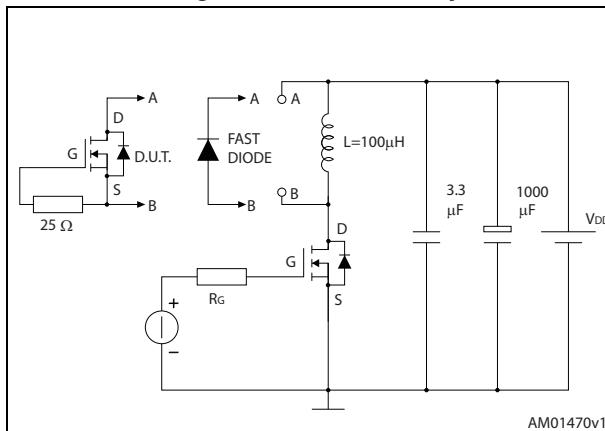
**Figure 15. Switching times test circuit for resistive load**



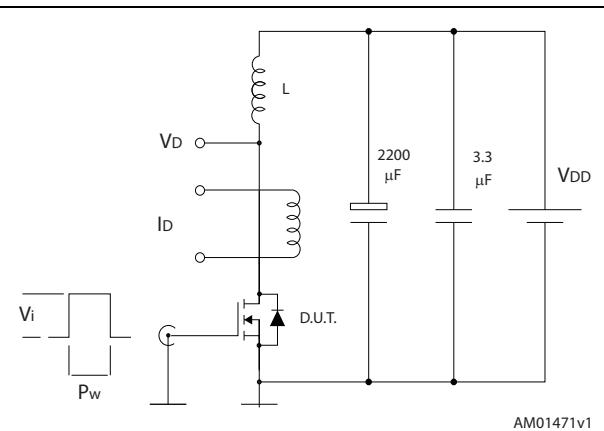
**Figure 16. Gate charge test circuit**



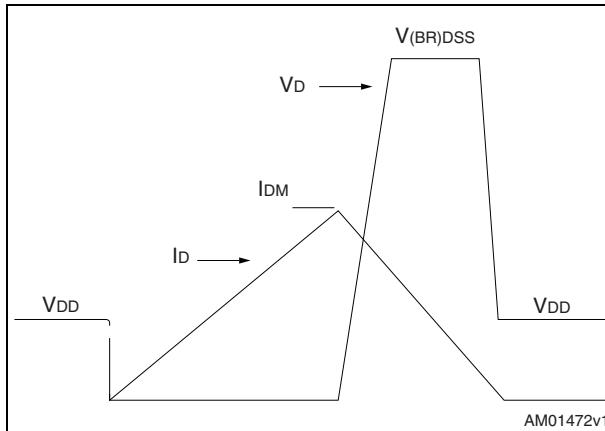
**Figure 17. Test circuit for inductive load switching and diode recovery times**



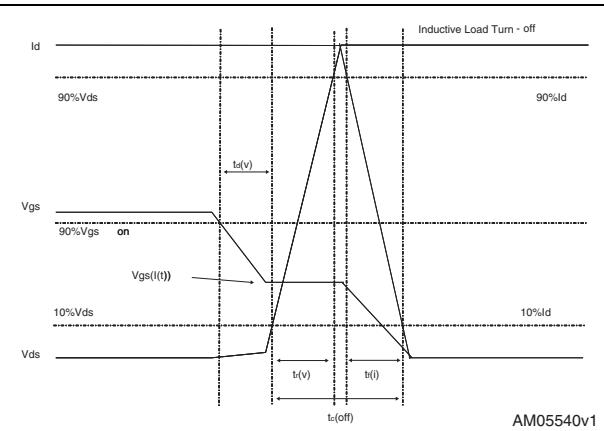
**Figure 18. Unclamped inductive load test circuit**



**Figure 19. Unclamped inductive waveform**



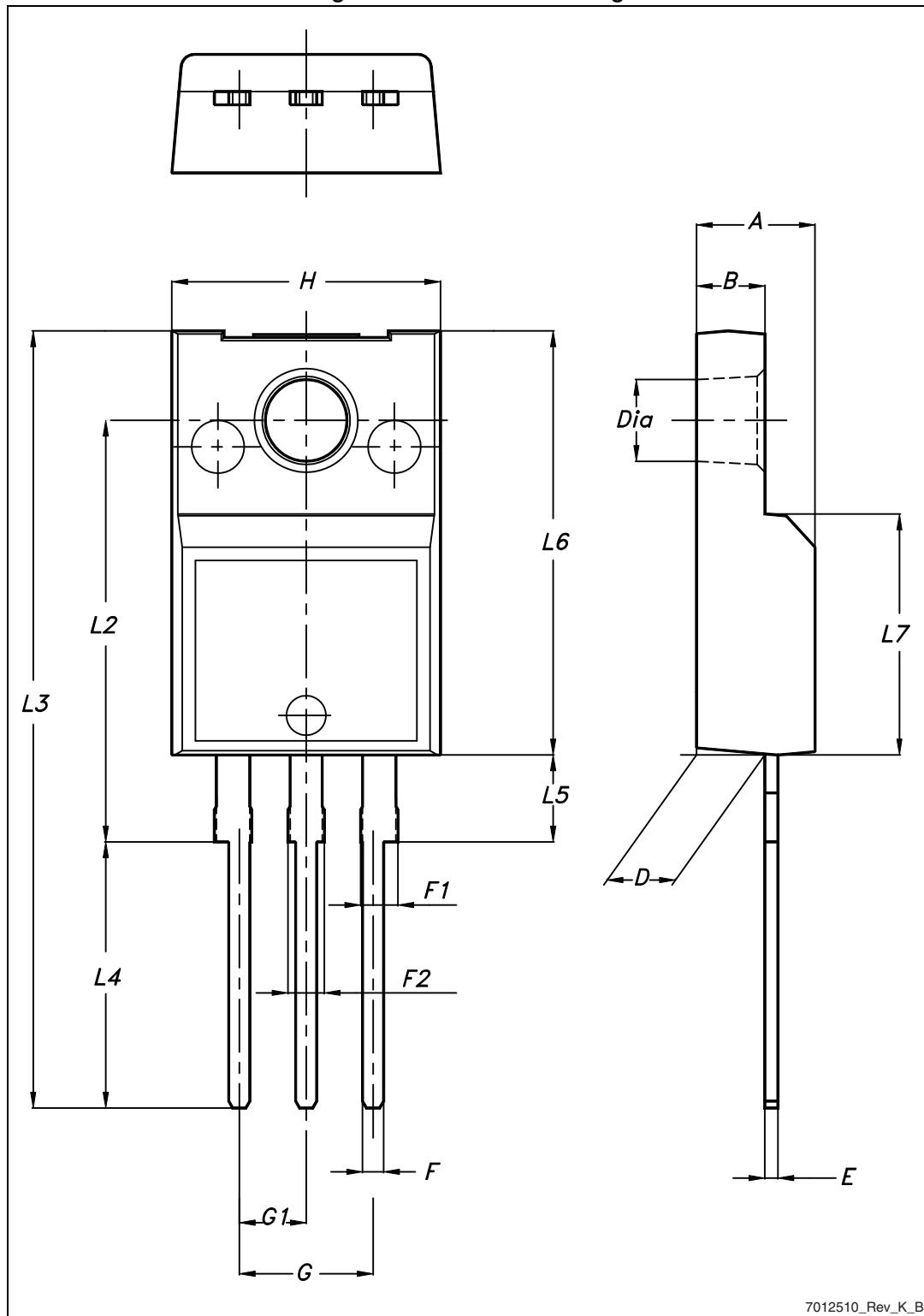
**Figure 20. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).  
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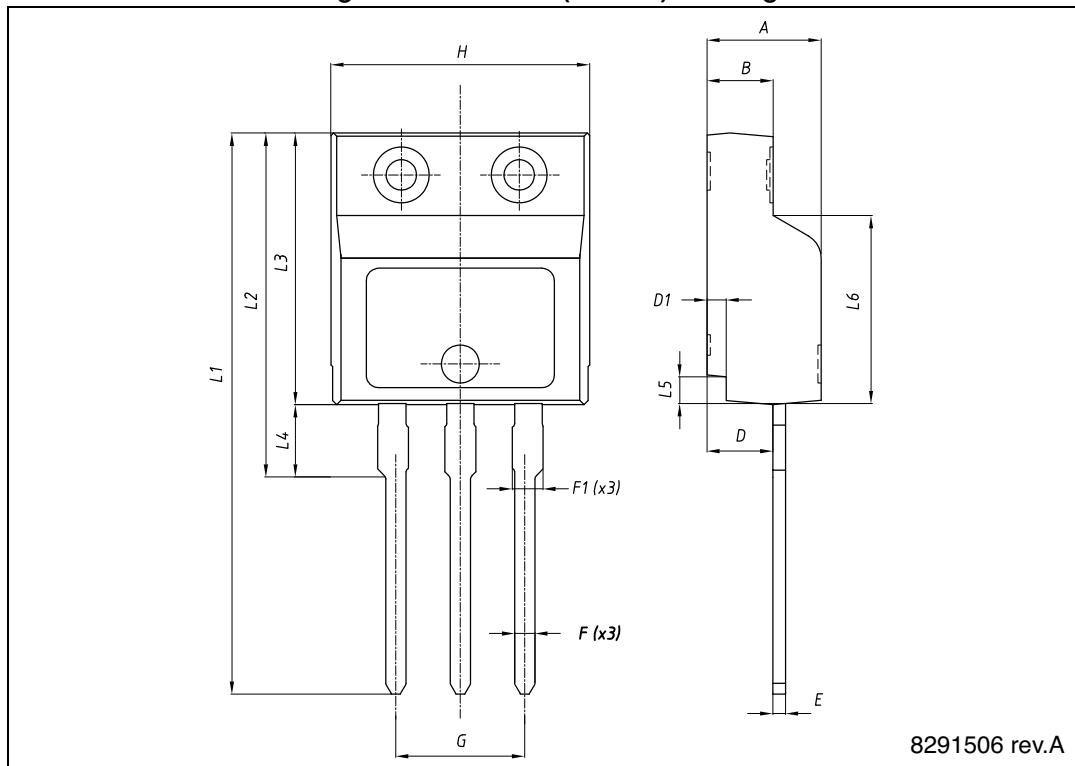
Figure 21. TO-220FP drawing



7012510\_Rev\_K\_B

Table 9. TO-220FP mechanical data

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 4.4  |      | 4.6  |
| B    | 2.5  |      | 2.7  |
| D    | 2.5  |      | 2.75 |
| E    | 0.45 |      | 0.7  |
| F    | 0.75 |      | 1    |
| F1   | 1.15 |      | 1.70 |
| F2   | 1.15 |      | 1.70 |
| G    | 4.95 |      | 5.2  |
| G1   | 2.4  |      | 2.7  |
| H    | 10   |      | 10.4 |
| L2   |      | 16   |      |
| L3   | 28.6 |      | 30.6 |
| L4   | 9.8  |      | 10.6 |
| L5   | 2.9  |      | 3.6  |
| L6   | 15.9 |      | 16.4 |
| L7   | 9    |      | 9.3  |
| Dia  | 3    |      | 3.2  |

Figure 22. I<sup>2</sup>PAKFP (TO-281) drawingTable 10. I<sup>2</sup>PAKFP (TO-281) mechanical data

| Dim. | mm    |      |       |
|------|-------|------|-------|
|      | Min.  | Typ. | Max.  |
| A    | 4.40  |      | 4.60  |
| B    | 2.50  |      | 2.70  |
| D    | 2.50  |      | 2.75  |
| D1   | 0.65  |      | 0.85  |
| E    | 0.45  |      | 0.70  |
| F    | 0.75  |      | 1.00  |
| F1   |       |      | 1.20  |
| G    | 4.95  | -    | 5.20  |
| H    | 10.00 |      | 10.40 |
| L1   | 21.00 |      | 23.00 |
| L2   | 13.20 |      | 14.10 |
| L3   | 10.55 |      | 10.85 |
| L4   | 2.70  |      | 3.20  |
| L5   | 0.85  |      | 1.25  |
| L6   | 7.30  |      | 7.50  |

## 5 Revision history

Table 11. Document revision history

| Date        | Revision | Changes   |
|-------------|----------|---|
| 14-Jan-2014 | 1        | First release. Part numbers previously included in datasheet<br>DocID022853 |

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