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STFPC320

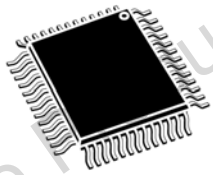
Front panel controller/driver with standby power management and real-time clock

Features

- IC front panel VFD controller driver
- Standby power management to the host
- 3.3 V (V_{DD}) and down to -30 V (V_{SS}) supply for the IC
- IR remote control decoder (Philips, NEC, Thomson, Sony, Matsushita)
- Multiple display modes (12 seg. and 16 digits to 20 seg and 8 digits)
- High voltage outputs (V_{DD} - 33.3 V max)
- No additional external resistors required for driver outputs (P-CH. open drain + pull-down resistor outputs)
- Key scanning (up to 12 x 2 matrix = 24 keys)
- LED ports (4 channels 20 mA max each)
- Serial I^2C interface (SCL, SDA) communication protocol b
- Operating speed: up to 400 kHz for I^2C
- Programmable hotkeys for IR remote control command and KEYSCAN command
- Low power consumption in standby mode
- Dimming circuit (8 steps)
- Real-time clock (accuracy ± 25 secs/month)
- Wake-up alarm
- Internal oscillator with external crystal for RTC
- Available in PQFP-52 package (0.65 mm pitch

Applications

- VCR, DVD and personal video recorders
- Home theatre with clock feature, STB and HTiB (home theater in a box)



PQFP-52

Description

The STFPC320 is designed to integrate the VFD driving, key-scan matrix, LED driving, infrared (IR) remote control decoding and real-time clock (RTC) into one integrated solution. All the functions are programmable using the I^2C bus.

Low power consumption is achieved during standby operation. The STFPC320 provides the standby power management to the main chipset.

The STFPC320 is housed in a 52-pin PQFP package. The pin assignments and application circuit are optimized for an easy PCB layout and cost saving advantages.

Table 1. Device summary

Order code	Operating temperature	Package	Packaging
STFPC320	-40°C to 85°C	PQFP-52	Tape and reel

Contents

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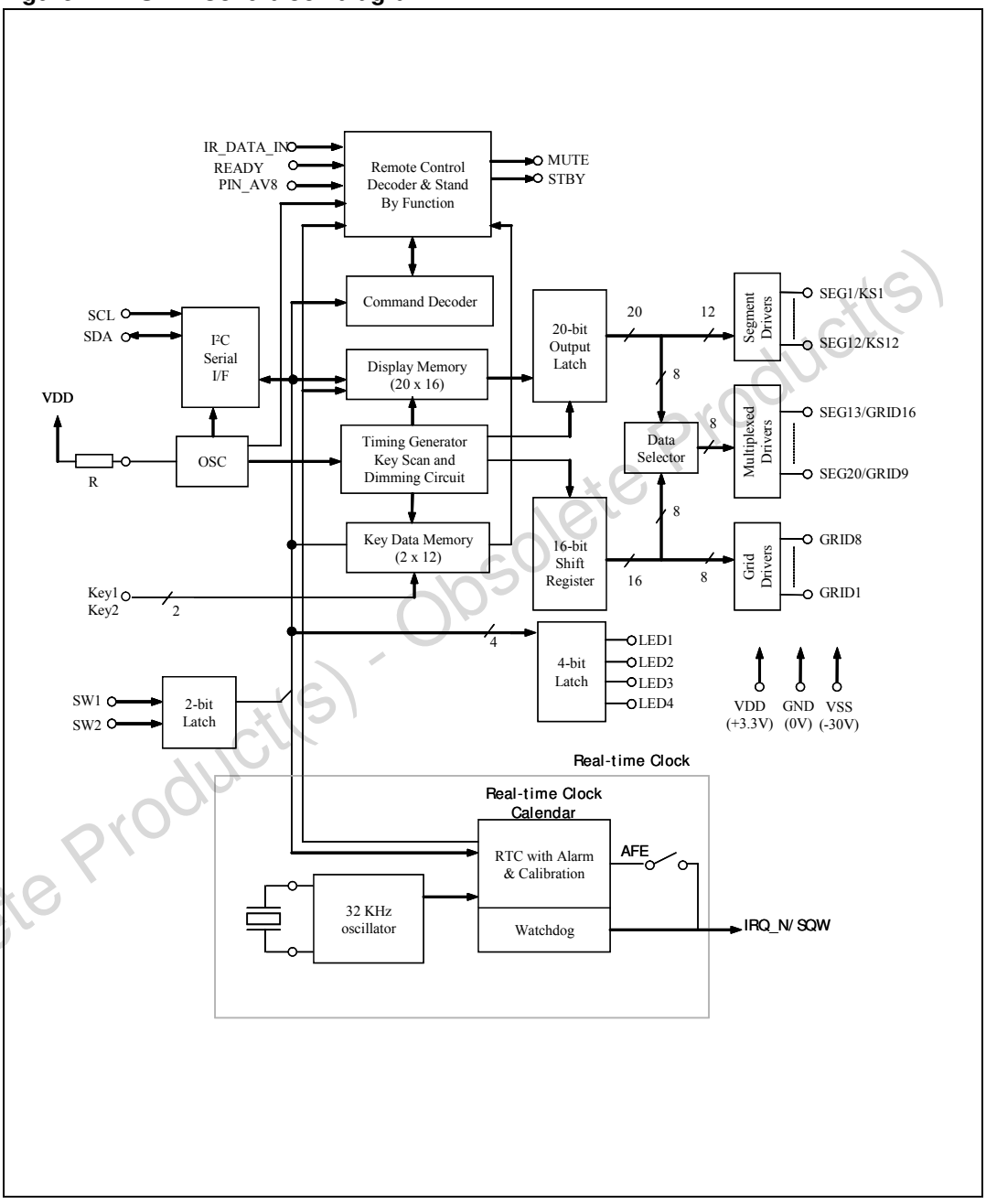
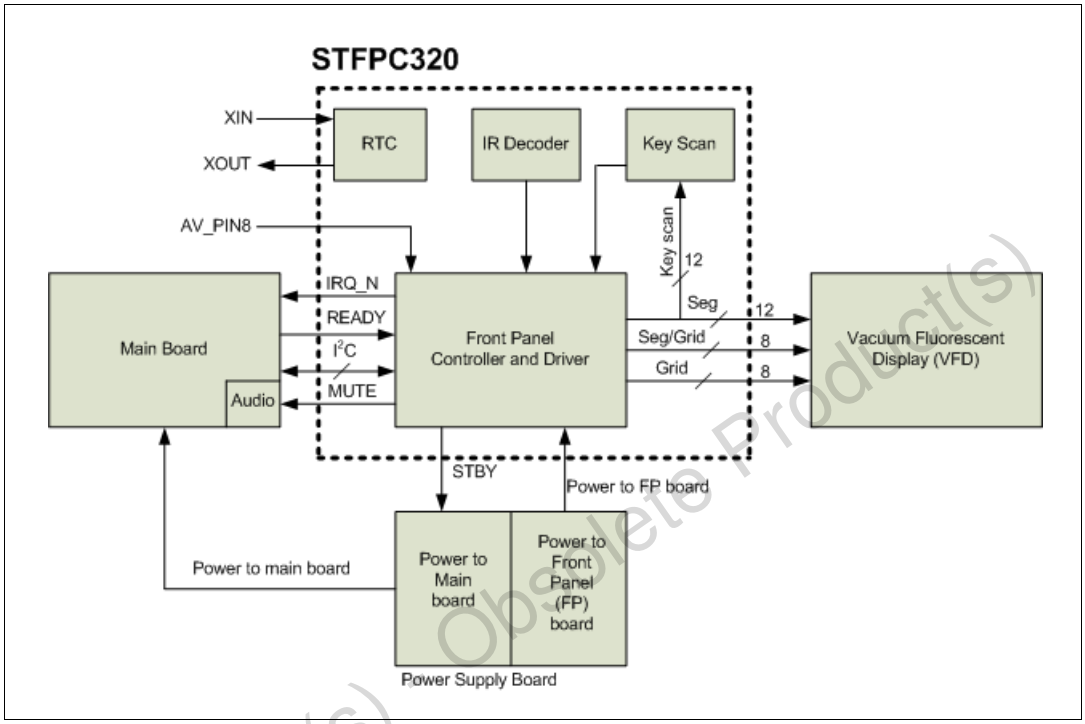
1 Device block diagram

Figure 1. STFPC320 block diagram



2 Functional diagram

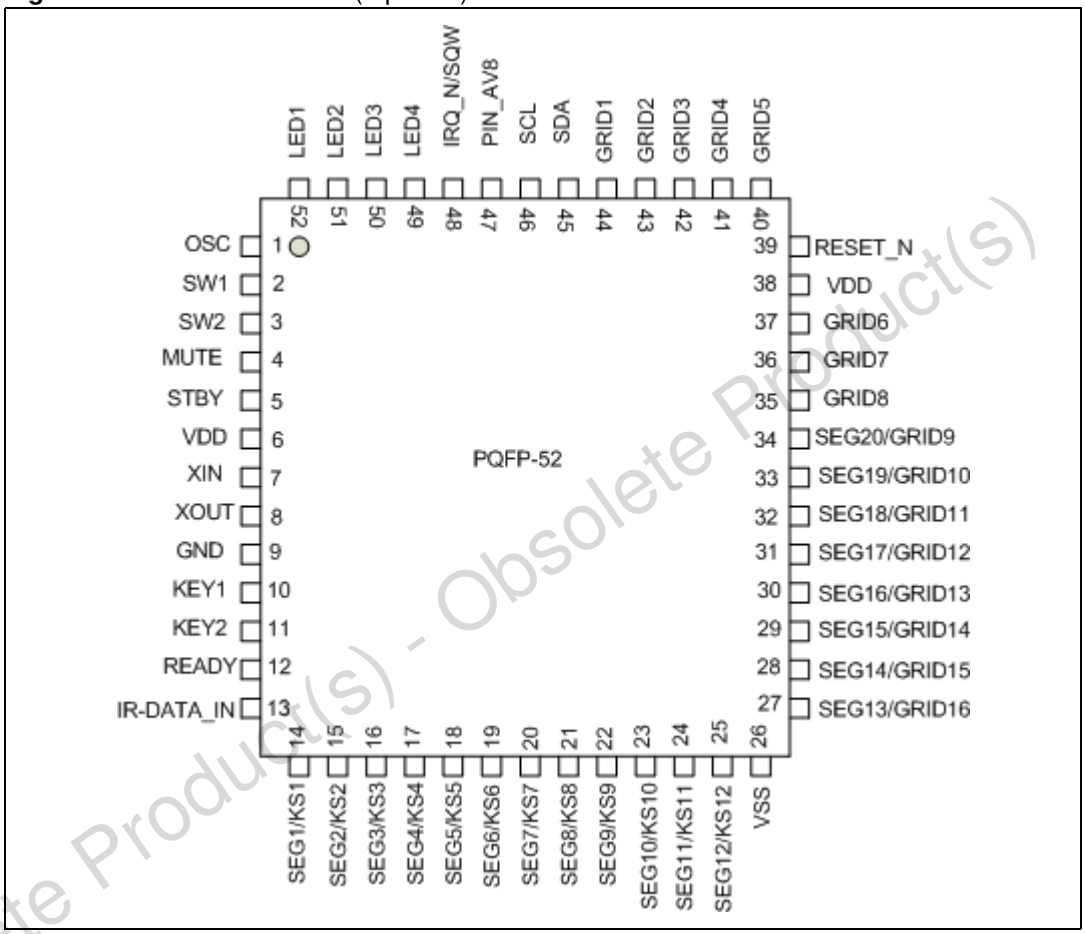
Figure 2. Functional diagram



3 Pin settings

3.1 Pin connection

Figure 3. Pin connection (top view)



Note: For a description of each pin behaviour, please refer to the STFPC320 Table 2: Pin description on page 12

3.2 Pin description

Table 2. Pin description

Pin N°	Name	Type	Description
1	OSC	IN	Connect to an external resistor of value 33 kΩ ± 1%
2	SW1	IN	General purpose switch input port.
3	SW2	IN	General purpose switch input port.
4	MUTE	OUT	High level means mute status for audio. Low level stands for normal working.
5	STBY	OUT	Pin to control power to the main board. High level means standby status. Low level stands for normal working. Active high.
6, 38	VDD	SUPPLY	3.3 V ± 10%. Core main supply voltage.
7	XIN	IN	Oscillator input pin. 32.768 KHz crystal.
8	XOUT	OUT	Oscillator output pin. 32.768 KHz crystal.
9	GND	SUPPLY	Connect this pin to system GND.
10,11	KEY1, KEY2	IN	Input data to these pins from external keyboard are latched at end of the display cycle (maximum keyboard size is 12 x 2).
12	READY	IN	High level on this pin means that main board chip has been working normally. Connect an external pull down resistor of 10kΩ on this pin.
13	IR_DATA_IN	IN	Remote control input. Connect to IR photodiode.
14 to 25	SEG1/KS1 to SEG12/KS12	OUT	Segment output pins (dual function as key source).
26	VSS	SUPPLY	VFD outputs high voltage pull-down level. VDD- 33.3 V max.
27 to 34	SEG13/GRID16 to SEG20/GRID9	OUT	These pins are selectable for segment or grid driving.
35-37	GRID8 to GRID6	OUT	Grid output pins.
39	RESET_N	IN	Active low reset input.
40-44	GRID5 to GRID1	OUT	Grid output pins.
45	SDA	IN/OUT	Serial data in/out. Connect to 3.3 V through an external pull-up resistor.
46	SCL	IN	Serial clock input. Connect to 3.3 V through an external pull-up resistor.
47	PIN_AV8	IN	A rising edge transition on this input will signal wake-up operation. This signal comes from the SCART interface. The micro processor can use this signal to start the recording or take other actions.
48	IRQ_N/SQW	OUT	Interrupt/square wave output (open drain). A pull up resistor of 10 kΩ must be connected on this pin.
49, 50, 51, 52	LED4, LED3, LED2, LED1	OUT	CMOS sink outputs (20 mA max).

4 Functional description

The STFPC320 integrates the supply standby management functionality, remote control decoder, a 28-bit VFD driver and a real-time clock (RTC). This device is meant to reduce the standby power consumption of the whole front panel application and also to reduce hardware/cost by integrating the above mentioned functions in a single chip.

By utilizing the standby function, the host processor and other ICs could be turned off, thus reducing the system power consumption. The STFPC320 is able to wake-up the system when programmed hotkeys are detected to signal that the full operation of the system is required. The hotkeys could be entered to the system through the front panel keys or through the infrared (IR) remote control. STFPC320 supports multiple remote control protocols decoding by setting the appropriate register.

The integrated 28-bit VFD driver can drive up to 16 digits of display. Controlling of the display is done through writing to a internal RAM. The 4 LED drivers allow indication of operation of the system. 2-wire serial interface (I^2C) completes the interfacing part between host processor and STFPC320.

The STFPC320 integrates a a low-power serial RTC with a built-in 32.768kHz oscillator (external crystal controlled). Eight bytes of the SRAM are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. An additional 12 bytes of SRAM provide status/ control of alarm, watchdog and square wave functions. Addresses and data are transferred serially via a two line, bidirectional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte.

Functions available to the user include a non-volatile, time-of-day clock/calendar, alarm interrupts, watchdog timer and programmable Square Wave output. The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24 hour BCD format. Corrections for 28, 29 (leap year - valid until year 2100), 30 and 31 day months are made automatically.

4.1 Reset

Reset is an active low input signal to the STFPC320. A negative pulse input on RESET_N pin resets the STFPC320. Electrical specifications of this pin are identical to that of the logic input pin.

Upon power-up, an internal power on reset circuit resets the whole chip. This occurs when V_{DD} is ramping up (at approximately 2.7 V) and the whole chip is initialized within 4 µs. This time is much lesser than the typical V_{DD} ramp-up time. It is recommended to tie the RESET_N pin permanently by a pull-up resistor to V_{DD} if reset to STFPC320 is not desired during normal operation. For an initialization on power-up, a power-on-reset in STFPC320 is sufficient to reset the entire STFPC320.

As soon as the 3.3 V supply to the chip is stable, the I^2C bus of the STFPC320 is ready for communication.

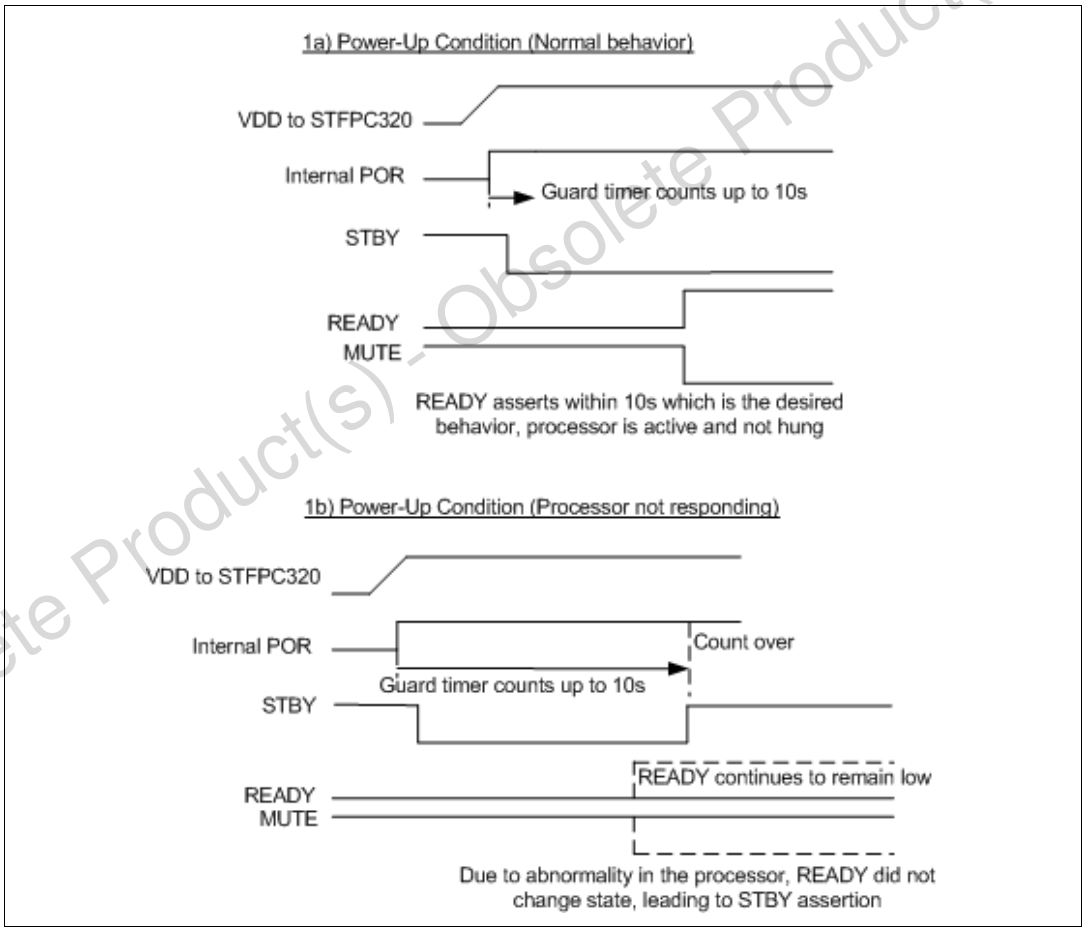
4.2 Cold boot up

When power is first applied to the system, the STFPC320 will be reset. It will then manage the power to the main board by bringing the STBY pin to a low level. This will wake-up the main processor which will assert the READY pin to a high level to indicate to STFPC320 of a proper boot-up sequence.

If the microprocessor does not assert the READY pin to a high within 10s, the STFPC320 will cut off the power to the Host by asserting the STBY pin. The high level on READY pin signifies that the processor is ready. After this, the processor can configure the STFPC320 by sending the various I^2C commands for configuration of display, RC protocol, RTC display mapping, hot-keys.

The power-up behavior in 2 conditions is shown in the *Figure 4*.

Figure 4. Power-up behaviour



Note: 1 Guard timer is turned off by default upon READY assertion.

2 If the guard timer is to be kept on during READY high condition, the guard timer registers must be set accordingly by proper commands through I^2C bus.

3 In this power-up condition, the guard timer is triggered by internal POR pulse.

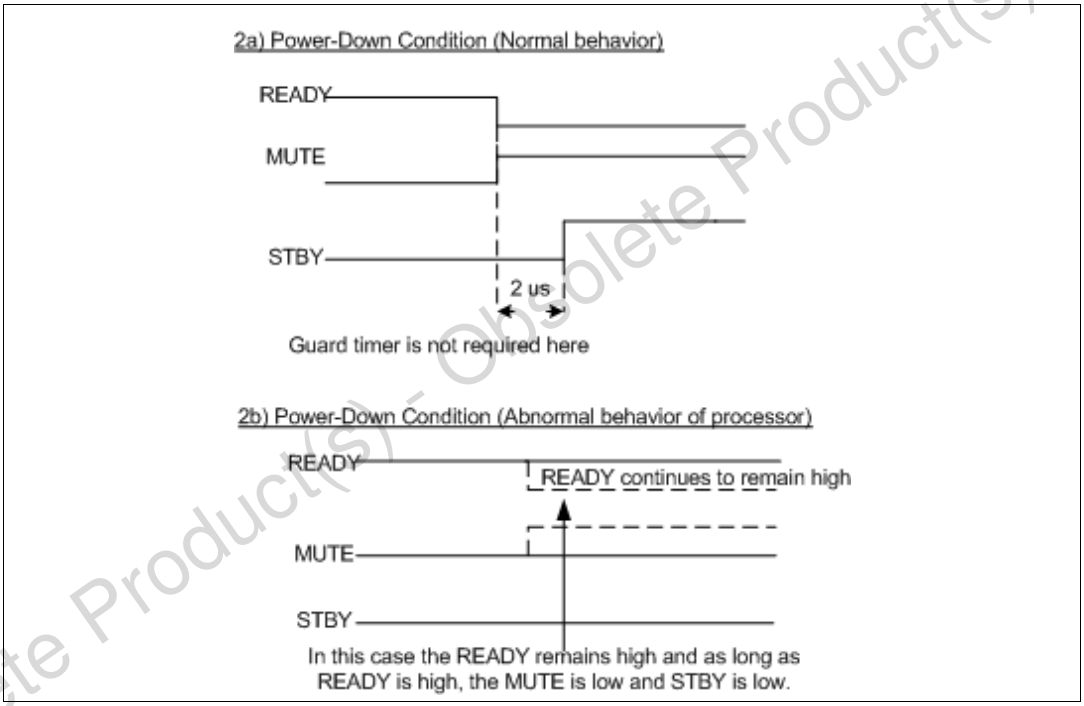
4 During power-up, the guard timer value is 10s.

4.3 Entering standby mode

The STFPC320 will control the power to the main board using the STBY pin. During normal operation, the STBY pin is at a low level which externally controls a power MOS switch to enable power to the main board. The STFPC320 asserts the STBY pin to a high when any one of the following conditions occur:

- Processor fails to respond by enabling the READY pin within 10 s upon first power-up (cold boot up)
- Guard timer counts down to 0 s
- Processor makes the READY pin to low (can happen in various conditions, such as user presses STBY key on front panel, STBY key on remote control, etc.)

Figure 5. Standby mode behaviour



Note: 1 Guard timer can be kept on during normal condition when READY is high (depending on the user).

2 In this condition, the guard timer can be disabled or enabled. If the guard timer is enabled, the timer needs to be cleared before the programmed count of the timer is reached. If the programmed count is reached, the STBY will be asserted.

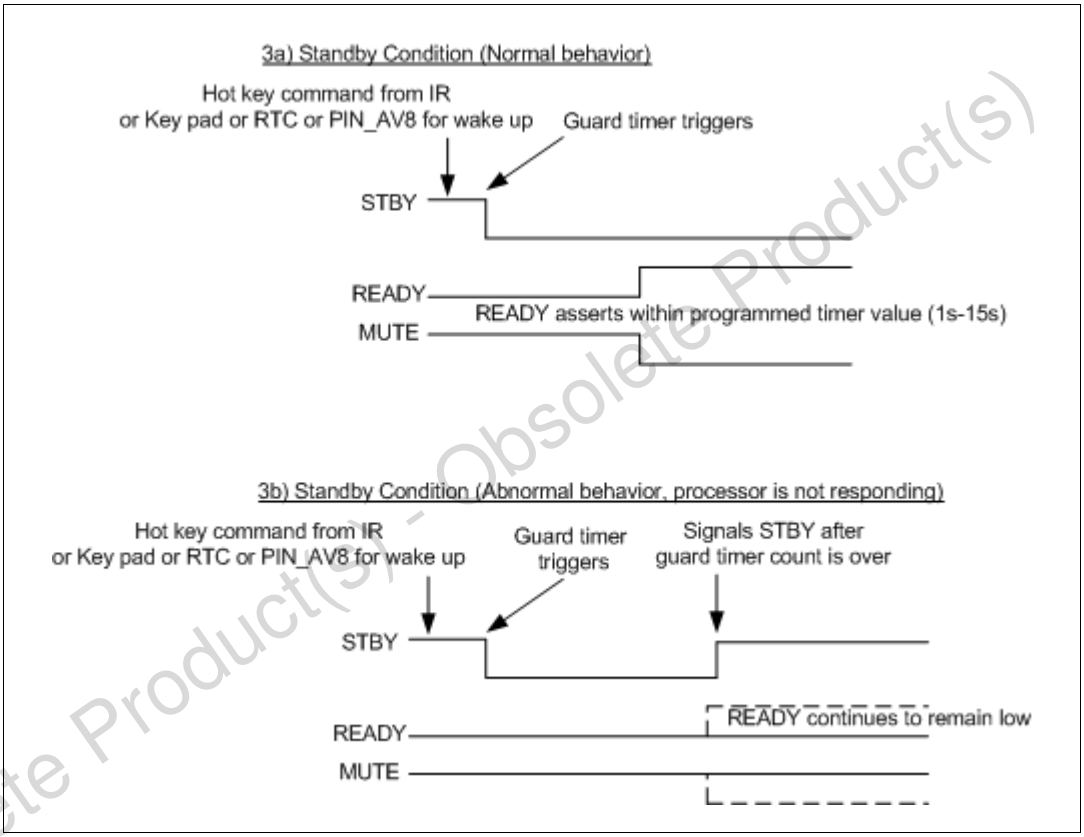
3 It is advisable not to enable the guard timer during normal operation.

4.4 Wake-up

The STFPC320 can wake-up from any one of the following sources:

- Front-panel keys
- Remote-control keys
- Real-time clock (RTC) in 3 conditions (alarm, watchdog timer, oscillator fail)
- External pin PIN_AV8 (only by a low-to-high transition on this pin)

Figure 6. Wake-up



Note: 1 When the hot-key is detected either from front-panel or remote control or RTC or from a low-to-high transition on PIN_AV8 pin during standby, the STBY pin de-asserts.

2 The de-assertion of the STBY triggers the guard timer.

3 The timer value is the programmed value by the user (1-15s). If the user did not change the value before entering standby, then it remains 10s.

4 Also note that the guard timer is off when the STFPC320 is in the standby mode.

Guard timer is thus triggered by a de-assertion of the STBY signal or by internal power on reset signal.

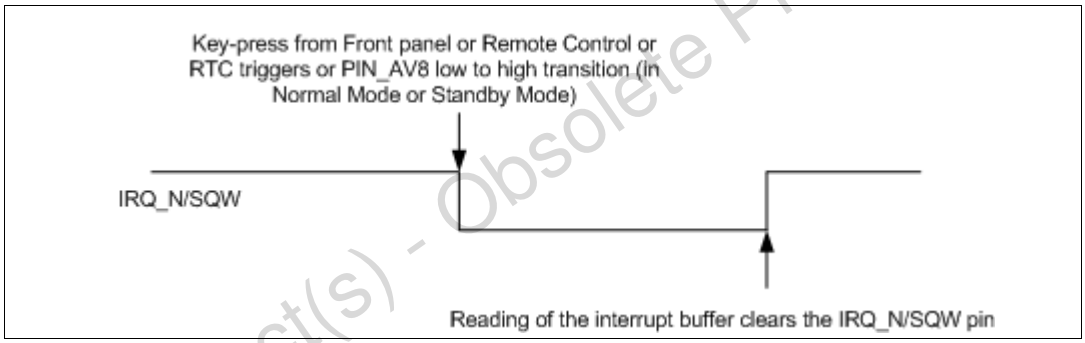
4.5 Interrupts/events handling by STFPC320

The STFPC320 interrupts the Host by pulling the IRQ_N/SQW pin to a low-level both in normal mode of operation and during wake-up. The interrupt is enabled by STFPC320 when any of the conditions occur:

- Front panel key press in normal operation or during system standby state
- Remote control key press in normal operation or during system standby state
- A low-to-high transition on the external pin, PIN_AV8
- Real-time clock triggers (alarm, watchdog timer, oscillator fail)

The IRQ_N/SQW is an active low level signal and is cleared only after the interrupt buffer is read. After reading the interrupt buffer, the Host will know the actual source of the interrupt. This allows the Host to exactly know the event which caused the interrupt (e.g STBY key on the front panel). The interrupt signal is used to inform the Host of any events detected by the STFPC320. Note that the IRQ_N/SQW pin is an open-drain pin which requires an external pull-up resistor.

Figure 7. Interrupts/events handling



4.6 Ready pin

The STFPC320 supports cutting-off power to the main board for standby operation for good power management. STBY will be set to high when the READY transitions from high to low. During a cold boot up or wakeup from standby, if the READY pin stays low, the STFPC320 will assert the STBY when the guard timer has finished counting down to 0.

When the READY drops to a low, MUTE goes high immediately and soon after (2 µs) the STBY is asserted.

In the normal mode of operation, when READY is a high, the STBY is asserted only when the guard timer is enabled and has finished counting down to 0. This is meant to put the system into standby as the READY pin was stuck at high and the guard timer register was not cleared before it finished counting down to 0. It is advised to disable the guard timer during normal operation.

4.7 Mute pin

The MUTE pin is set to logic high to mute the audio output before power is cut to the host processor. In wakeup mode, the MUTE pin is set to logic low to enable the audio output immediately after the high assertion of the READY pin. In general, MUTE follows READY pin with an inverted polarity. This pin is used to prevent pop-up sound during power-up and power-down states.

4.8 Keyscan matrix/front panel keys

The key scan matrix on the STFPC320 helps to pass command from the front panel to the host processor through the SDA pin on STFPC320. The STFPC320 can be programmed to wake-up the system from standby using any of the 24 keys pressed on the front panel. These wake-up keys are also referred to as hot-keys.

4.9 LED ports

4 LED displays are supported by the STFPC320. Turning on or off of the LED is done by issuing write command to the LED port. After reset, the LEDs are off. Note that the LED outputs sink the current, so the cathode of the diode must be connected to the LED pins of STFPC320.

4.10 Display

The display is divided into two sections, Normal and real-time clock (RTC).

4.10.1 Normal display

The VFD display is configurable for displays from 8 digits/20 segments to 16 digits/12 segments. The VFD display can be configured to be either in the normal VFD mode or in the RTC mode. In the normal VFD mode, the display shows whatever is written in the VFD display memory.

If the user desires to show normal display simultaneously with the RTC, then CPU must read the time of RTC display memory and then write all the data to be displayed to the normal display memory. After writing the values to the display memory, a display-on command will show both the normal and RTC display on the front panel.

On first power on, the default configuration is 16-digit, 12-segment mode (with display turned OFF).

4.10.2 RTC display

In RTC mode, the display can be configured to show the time in two modes, either by direct mapping of RTC to the display or by using the CPU. If CPU is used, the CPU reads the RTC value from RTC registers and then writes the time to be displayed in the RTC display memory.

4.11 Remote control decoder

Remote control (RC) decoder module decodes the signal coming from IR_DATA_IN. The list of IR remote control protocols recognized by STFPC320 is Philips RC-5, SONY, NEC, Thomson-RCA, Thomson-R2000 and Matsushita. The selection of remote control protocol to use is done by setting the RC Protocols register. The commands from RC is used to wake-up from standby and resume normal operation. All RC keys can be programmed to act like RC hotkeys. Upon receiving any one of the designated hotkeys, wake-up operation will begin.

4.12 PIN_AV8

External device (e.g. set-top box) could pull this pin high to wake-up the system. A low-to-high transition on this pin will signal the STPFC320 to wake-up and provide power to the system. This signal is considered high when it is in the range of 2.5 - 3.6 V (proper voltage division must be done externally so that the STFPC320 PIN_AV8 sees no more than 3.6 V). No action is taken on the high-to-low transition on PIN_AV8. Also when the pin is already a high, the current state of the system is maintained and it does not trigger anything.

4.13 Default state upon power-up

The *Table 3* below shows the default state of the STFPC320 upon power-up.

Table 3. Default state

S.No.	Functions	Default state
1	Display	OFF
2	Key-scan	ON
3	IR (Remote Control)	ON
4	Display mode	12 segment/16 digit
5	Display address	10H with Address increment mode
6	RC protocol	RC-5 (Raw format)
7	LED	OFF
8	Dimming	1/16 duty factor
9	Hot Keys (IR and FP)	Disabled
10	Guard timer	10s

4.14 Initial state

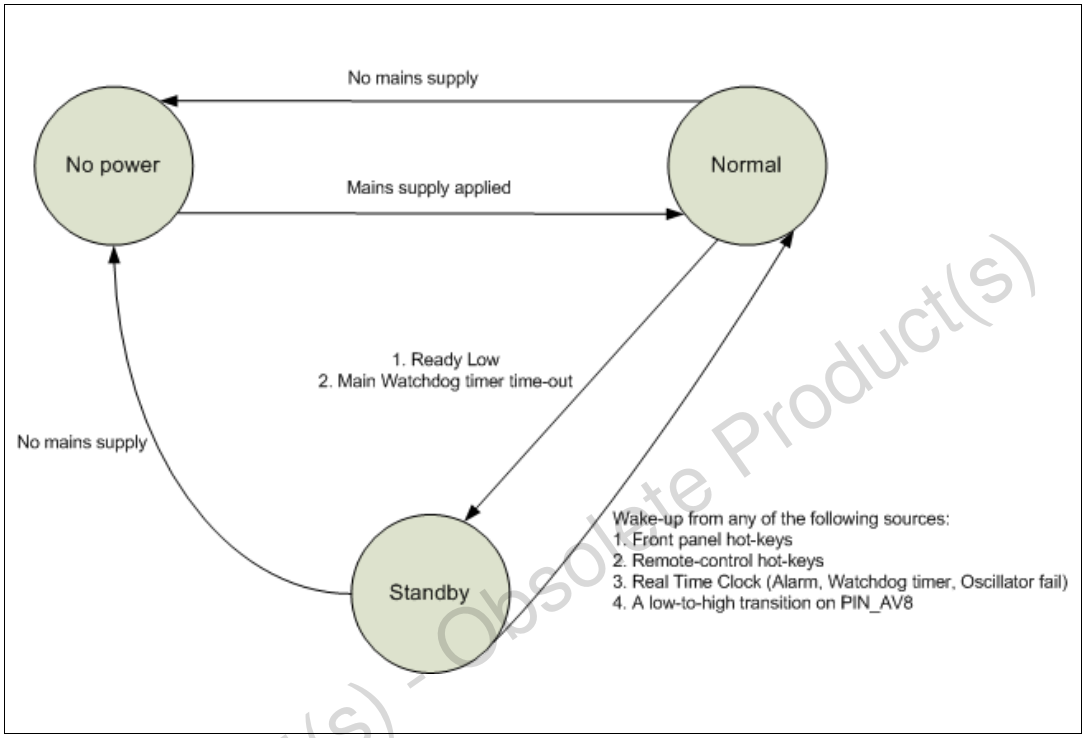
On power application, the 1/16-pulse width is set and the display shows the value configured in the VFD display RAM before entering the standby mode. Thus if HELLO is required to be shown on the VFD upon wake-up, then the user must write the corresponding digit and segments locations in the VFD display memory before going into the standby mode of operation. Note that the V_{SS} must be present in order to keep the VFD display active. The value of the display changes only after user configuration.

If the user wishes to display the RTC value during standby, then the user must configure the STFPC320 by sending the appropriate command. If the user does not configure the STFPC320 to display the RTC in standby, the VFD shows the same value as was written in the VFD display memory location.

Note that all the hot keys are disabled on power-up. Only the hotkeys (FP or RC) or RTC or the low to high transition on the PIN_AV8 pin can be detected to wake-up the system from standby condition.

5 Operating state diagram

Figure 8. Operating state diagram



6 Real-time clock (RTC) operation

6.1 Real-time clock

The RTC operates as a slave device through the slave address of the STFPC320 on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (Write: 0x52H and Read: 0x53H). The 16 bytes contained in the device can then be accessed sequentially in the following order:

1. Reserved
2. Seconds register
3. Minutes register
4. Hours register
5. Square wave/day register
6. Date register
7. Century/month register
8. Year register
9. Calibration register
10. Watchdog register

11 - 15. Alarm registers

16. Flags register

6.2 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bidirectional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage (typical voltage is 3.3 V) via a pull-up resistor (typical value is 10 K). The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is High.
- Changes in the data line, while the clock line is High, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

- **Bus not busy**: both data and clock lines remain High.
- **Start data transfer**: a change in the state of the data line, from high to Low, while the clock is High, defines the START condition.
- **Stop data transfer**: a change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.
- **Data Valid:** the state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.
  Each data transfer is initiated with a start condition and terminated with a stop

condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.
By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

- **Acknowledge:** each byte of eight bits is followed by one Acknowledge Bit. This Acknowledge Bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the master transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line High to enable the master to generate the STOP condition.

Figure 9. Serial bus data transfer sequence

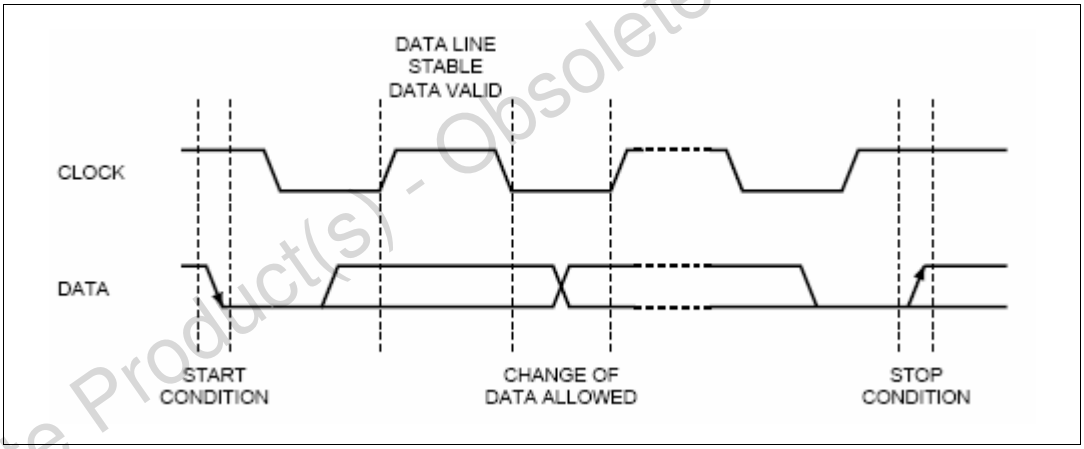
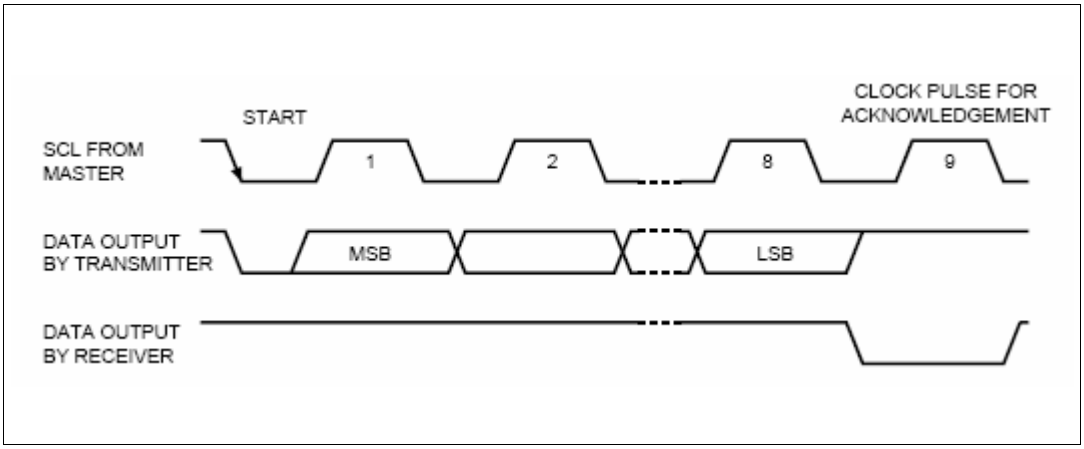


Figure 10. Acknowledgement sequence



6.3 Watchdog timer

The watchdog timer can be used to detect an out of control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the Watchdog Register, address 09h. Bits BMB4-BMB0 store a binary multiplier and the three bits RB2-RB0 select the resolution where:

- 000 = 1/16 second (16Hz)
- 001 = 1/4 second (4Hz)
- 010 = 1 second (1Hz)
- 011 = 4 seconds (1/4Hz)
- 100 = 1 minute (1/60Hz)

*Note: Invalid combinations (101, 110, and 111) do NOT enable a watchdog time-out. Setting the BMB4-BMB0 = 0 with any combination of RB2-RB0, other than 000, will result in an immediate watchdog time-out. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog register = 3*1 or 3 seconds). If the processor does not reset the timer within the specified period, the STFPC320 generates a watchdog output pulse on the IRQ_N/SQW pin.*

The watchdog timer can only be reset by having the microprocessor perform a WRITE of the Watchdog register. The time-out period then starts over. Should the watchdog timer time-out, any value may be written to the Watchdog Register in order to clear the IRQ_N/SQW pin. A value of 00h will disable the watchdog function until it is again programmed to a new value. A READ of the Flags Register will reset the Watchdog flag (Bit D7; Register 0Fh). The watchdog function is automatically disabled upon power-up, and the Watchdog Register is cleared.

6.4 Real-time clock (RTC)

The RTC keeps track of the date and time. Once the date and time are set, the clock works when the STFPC320 is in normal operation and standby operation. The wake-up alarm feature is included in the RTC module. The accuracy of the RTC is approximately 10 ppm (±25 secs/month).

The wakeup alarm is programmed to wake up once the date and time set are met. This feature is present in normal and standby mode of operation. Only one date and time is available for setting.

The real-time clock (RTC) uses an external 32.768 kHz quartz crystal to maintain an accurate internal representation of the second, minute, hour, day, date, month, and year. The RTC has leap-year correction. The clock also corrects for months having fewer than 31 days.

6.4.1 Reading the real-time clock

The real-time clock (RTC) is read by specifying the address corresponding to the register of the real-time clock and then initiating a Read command. The RTC registers can then be read in a sequential read mode. Since the clock runs continuously and a read takes a finite amount of time, there is the possibility that the clock could change during the course of a read operation. In this device, the time is latched by the read command (falling edge of the clock on the ACK bit prior to RTC data output) into a separate latch to avoid time changes during the read operation. The clock continues to run. Alarms occurring during a read are unaffected by the read operation.

6.4.2 Writing to the real-time clock

The time and date may be set by writing to the RTC registers. To avoid changing the current time by an uncompleted write operation, the current time value is loaded into a separate buffer at the falling edge of the clock on the ACK bit before the RTC data input bytes, the clock continues to run. The new serial input data replaces the values in the buffer. This new RTC value is loaded back into the RTC register by a stop bit at the end of a valid write sequence. An invalid write operation aborts the time update procedure and the contents of the buffer are discarded. After a valid write operation the RTC will reflect the newly loaded data beginning with the next “one second” clock cycle after the stop bit is written. The RTC continues to update the time while an RTC register write is in progress and the RTC continues to run during any nonvolatile write sequences. A single byte may be written to the RTC without affecting the other bytes.