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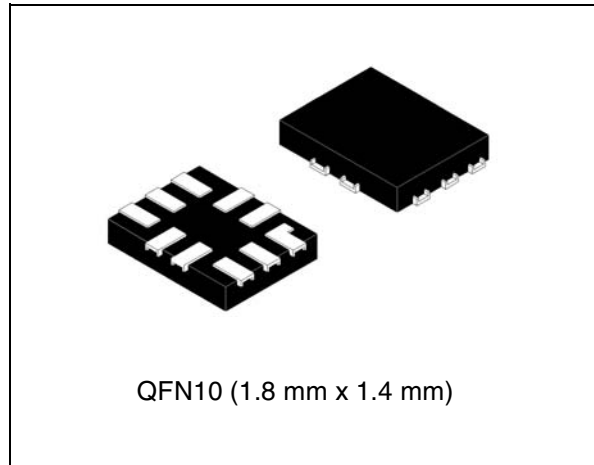


STG3696E

Low voltage dual SPDT switch for USB/audio signal switching
with 8 kV ESD protection

Features

- Low distortion negative signal swing capability for audio switch (range = V_{CC} to $V_{CC} - 5.0$ V)
- Single supply operating voltage:
 $V_{CC} = 2.7$ V to 4.5 V
- Typical bandwidth (-3 dB) of 950 MHz on all channels
- USB (2.0) high speed (480 Mbps) signal switching compliant
- Integrated fail safe function to protect against short to 5.5 V
- Internal shunt resistors for pop noise suppression
- Auto detection of V_{BUS} for switch selection
- Low R_{ON} resistance of 2.5 Ω (typ.)
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance exceeds JESD22 (COM pins to GND) ± 8 kV Human Body Model (A114-A)
- ESD performance exceeds JESD22 (other pins) ± 2 kV Human Body Model (A114-A)



Applications

- Mobile phones
- MP3 and other personal media players

Table 1. Device summary

Order code	Package	Packing
STG3696EQTR	QFN10 (1.8 mm x 1.4 mm)	Tape and reel

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1 Description

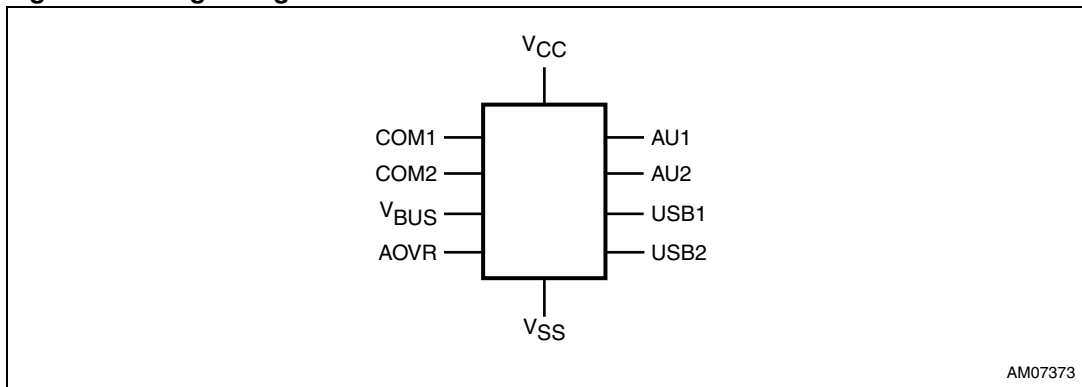
STG3696E is a high speed ESD protected dual SPDT (single pole dual throw) switch that combines low distortion audio and accurate USB 2.0 high speed (480 Mbps) data signal switching in the same device.

When the audio path is selected, the switch allows the audio signal to swing below ground (up to $V_{CC} - 5.0\text{ V}$). Superior channel-to-channel crosstalk also minimizes interference. Integrated shunt resistors in the device helps to suppress pop noise on the audio path.

When V_{BUS} is greater than $V_{BUSTHRES}$, STG3696E will automatically switch from the audio channel to the USB channel. The device is compatible with the requirements of USB 2.0 and features low on capacitance plus low resistance needed to achieve high performance switching in mobile applications.

The device allows the D+/D- pins to withstand an overvoltage condition of 5.5 V in compliant with the USB 2.0 fault protection specification.

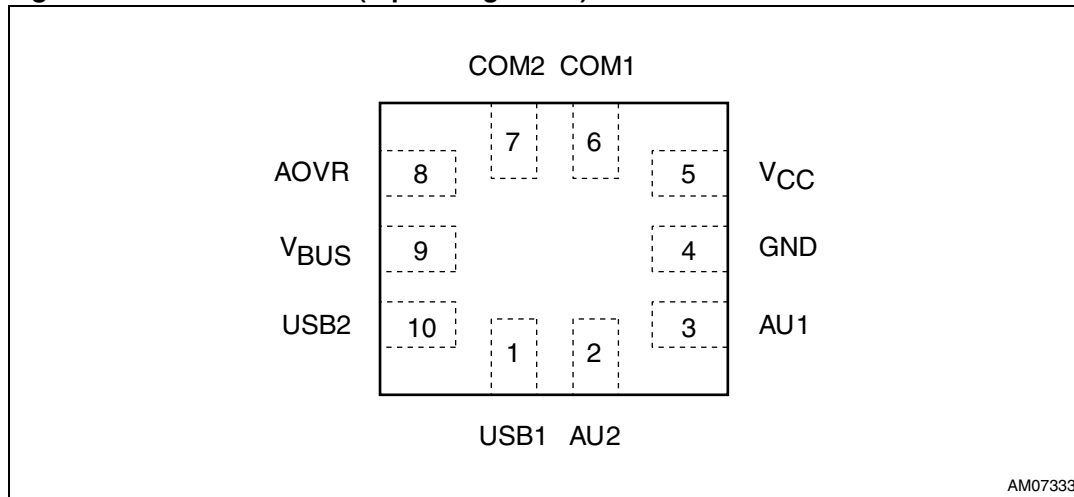
Figure 1. Logic diagram



2 Pin settings

2.1 Pin connection

Figure 2. Pin connection (top through view)



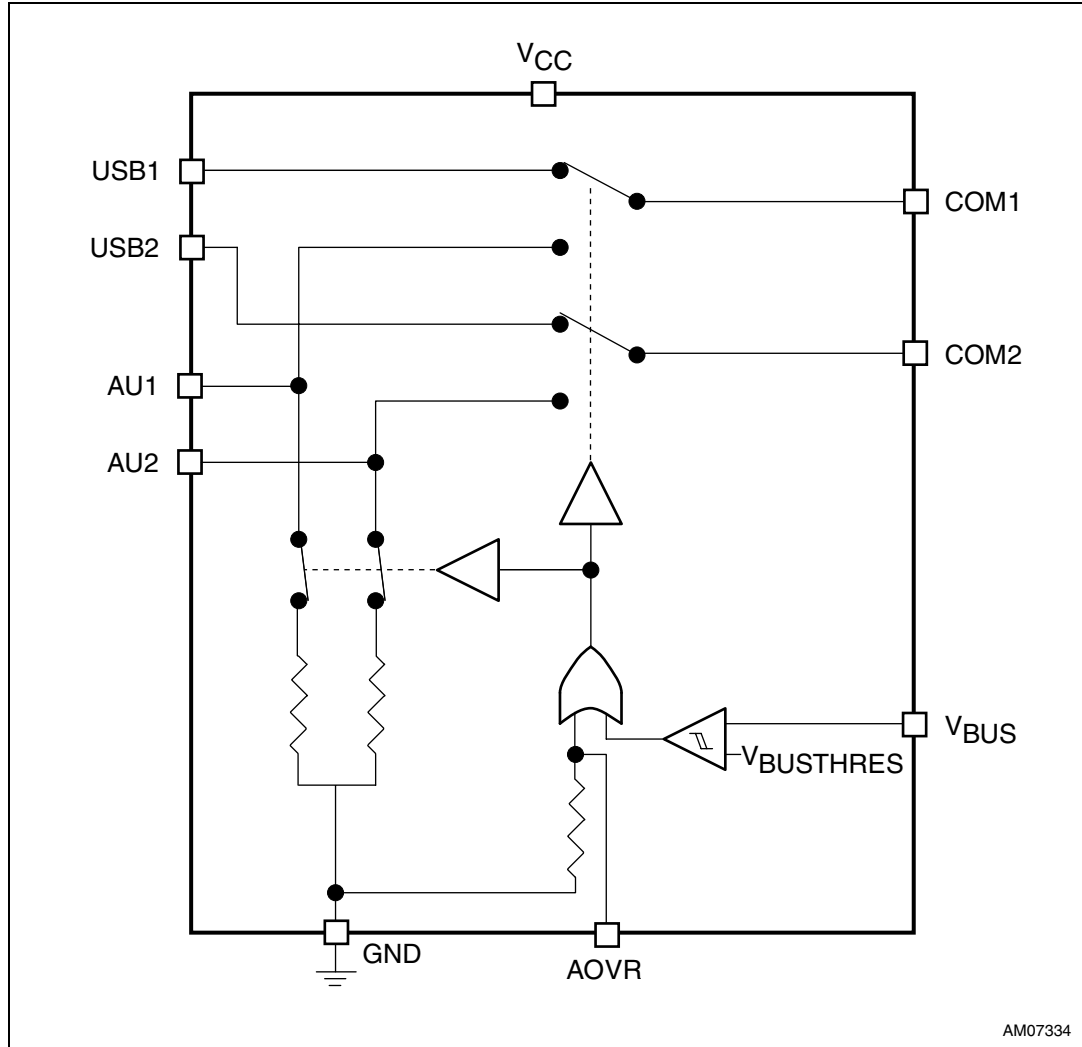
2.2 Pin description

Table 2. Pin assignment

Pin number	Symbol	Name and function
1	USB1	USB channel 1
2	AU2	Audio channel 2
3	AU1	Audio channel 1
4	GND	Ground (0 V)
5	V _{CC}	Positive supply voltage
6	COM1	Common channel 1
7	COM2	Common channel 2
8	AOVR	Audio Override Enable. When AOV is low, switch selection is controlled by V _{BUS} . When AOV is high, COM channels will be connected to audio channels. AOV has an internal pull-down resistor to GND.
9	V _{BUS}	V _{BUS} detection. If V _{BUS} ≥ V _{BUSTHRES} , COM channels are connected to USB channels. Otherwise, COM channels will be connected to audio channels.
10	USB2	USB channel 2

3 Functional diagram

Figure 3. Functional diagram



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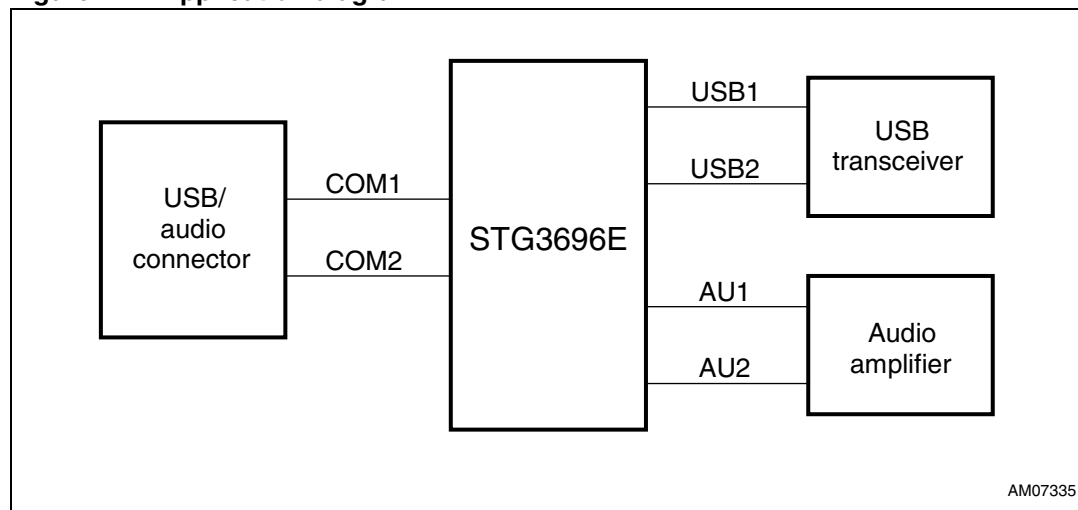
Table 3. Truth table

V_{BUS}	AOVR	USBn	AUn	AUn shunt
$\geq V_{BUSTHRES}$	LOW	ON	OFF	ON
$< V_{BUSTHRES}$	LOW	OFF	ON	OFF
$X^{(1)}$	ON	OFF	ON	OFF

1. Don't care.

4 Application diagram

Figure 4. Application diagram



5 Operation

5.1 Overvoltage fault protection

STG3696E features an overvoltage fault protection in compliance to USB fault protection specification. The fault protection circuitry is triggered when the voltage on the COMn channels raise above V_{OVDT} . The overvoltage fault protection helps to protect the switch and USB transceiver from being damaged by excessive voltage levels.

5.2 Negative charge pump for negative rail audio signaling

STG3696E uses a negative charge pump to generate a negative supply which allows the audio signal to swing below ground (up to $V_{CC} - 5.0$ V) on the AUn channels. If the device fault protection is activated when the voltage on the COMn channels raise above V_{OVDT} , there must not be a negative voltage attached to the AUn channels.

5.3 V_{BUS} detection feature

The connection between USBn and COMn is triggered when V_{BUS} voltage is detected to be higher than $V_{BUSTHRES}$. If V_{BUS} is constantly present in the application, driving the audio override enable (AOVR) high will connect the AUn channels to the COMn channels. If AOVR is low, the switching between AUn and USBn is controlled by the V_{BUS} detection.

5.4 Pop noise suppression

When the AUn channels are not connected to the COMn channels, the AUn channels are automatically connected to $200\ \Omega$ shunt resistors which helps to discharge any capacitance built up on the AUn channels. This will reduce the possibility of pop and click noise occurrence when switching between USB and audio sources.

6 Maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the “Operating” sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		-0.5 to 6.0	V
V_{COMn}	Common port voltage	$AOVR = 1$ or $V_{BUS} < V_{BUSTHRES}$	$-(V_{CC} - 6.0)$ to 6.0	V
		$V_{BUS} \geq V_{BUSTHRES}$	-0.5 to 6.0	
V_{AUn}	Audio port voltage	$AOVR = 1$ or $V_{BUS} < V_{BUSTHRES}$	$-(V_{CC} - 6.0)$ to $V_{CC} + 0.5$	V
		$V_{BUS} \geq V_{BUSTHRES}$	-0.5 to $V_{CC} + 0.5$	
V_{USBn}	USB port voltage		-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC input diode current		± 50	mA
I_{OK}	DC output diode current		± 20	mA
I_O	DC output current		± 150	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)		± 400	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current		± 100	mA
P_D	Power dissipation at $T_A = 70\text{ }^\circ\text{C}^{(1)}$		1120	mW
T_{stg}	Storage temperature		-65 to +150	$^\circ\text{C}$
T_L	Lead temperature (10 s)		300	$^\circ\text{C}$

1. Derate above 70 $^\circ\text{C}$ by 18.5 mW/ $^\circ\text{C}$.

7 DC and AC parameters

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 4.5	V
V_{IO}	Input/output voltage	V_{USBn}	0 to V_{CC}
		V_{AU_n}	$V_{CC} - 5.0$ to V_{CC}
		V_{COMn} (AOVR = 1 or $V_{BUS} < V_{BUSTHRES}$)	$V_{CC} - 5.0$ to V_{CC}
		V_{COMn} ($V_{BUS} \geq V_{BUSTHRES}$)	0 to V_{CC}
T_{op}	Operating temperature	-40 to 85	°C

Table 6. DC and AC characteristics

Symbol	Parameter	V_{CC} (V)	Test conditions ⁽¹⁾	Value			Unit
				Min.	Typ. ⁽²⁾	Max.	
V_{IH}	High level input voltage			1.6			V
V_{IL}	Low level input voltage					0.4	V
$V_{BUSTHRES}$	V_{BUS} detect threshold voltage				0.5 x V_{CC}		V
V_{OVDT} ⁽³⁾	COM overvoltage detect threshold	2.7 - 3.3	$T_A = 25\text{ °C}$	$V_{CC} + 0.35$		$V_{CC} + 1.0$	V
$R_{ON(AU)}$	Audio channel ON Resistance	3.0	$V_{AU_n} = -1.5\text{ V}, 1.5\text{ V}$ $I_{COMn} = 10\text{ mA}$		2.4	5	Ω
$R_{ON(USB)}$	USB channel ON Resistance	3.0	$V_{USBn} = 0\text{ V}, V_{CC}$ $I_{COMn} = 10\text{ mA}$		2.4	5	Ω
$\Delta R_{ON(AU)}$ ^{(4), (5)}	ON resistance matching between audio channels	3.0	$V_{AU_n} = 0\text{ V}$ $I_{COMn} = 10\text{ mA}$			0.5	Ω
$\Delta R_{ON(USB)}$ ^{(4), (5)}	ON resistance matching between USB channels	3.0	$V_{USBn} = 0\text{ V}$ $I_{COMn} = 10\text{ mA}$			0.5	Ω
$R_{FLAT(AU)}$ ⁽⁶⁾	ON resistance flatness for audio channels	3.0	$V_{AU_n} = -1.5\text{ V to } 1.5\text{ V}$ $I_{COMn} = 10\text{ mA}$		0.03	0.25	Ω
$R_{FLAT(USB)}$ ⁽⁶⁾	ON resistance flatness for USB channels	3.0	$V_{USBn} = 0\text{ V to } V_{CC}$ $I_{COMn} = 10\text{ mA}$		0.05	0.5	Ω
R_{SH}	Shunt switch resistance		$I_{AU_n} = 1\text{ mA}$		200	300	Ω
$I_{USB(OFF)}$	USB channel off leakage current	3.0	$V_{USBn} = 2.5\text{ V}, 0\text{ V}$ $V_{COMn} = -1.5\text{ V}, 2.5\text{ V}$	-15		15	nA
$I_{COM(OFF)}$	Common channel off leakage current	0	$V_{COMn} = 3.6\text{ V}$ $V_{USBn} = V_{AU_n} = 0\text{ V}$			500	μA

Table 6. DC and AC characteristics (continued)

Symbol	Parameter	V _{CC} (V)	Test conditions ⁽¹⁾		Value			Unit
					Min.	Typ. ⁽²⁾	Max.	
I _{COM(ON)}	Common channel on leakage current	3.0	USB mode	V _{AUn} = 0 V, 2.5 V, unconnected V _{COMn} = 0 V, 2.5 V		0.3	1	μA
		3.0	Audio mode	V _{USBn} = 0 V, 2.5 V, unconnected V _{COMn} = -1.5 V, 2.5 V		0.3	1	
I _{CC}	Quiescent supply current	3.3	V _{AOVR} = 0, V _{BUS} = V _{BUSTHRES}			9	24	μA
			V _{AOVR} = V _{CC} , V _{BUS} = 0 V			9	24	
		4.5	V _{AOVR} = 0, V _{BUS} > V _{BUSTHRES}			18	36	
			V _{AOVR} = V _{CC} , V _{BUS} = 0 V			18	36	
t _{FP}	Fault-protection response time	3.0	V _{COMn} = 1 V to 5 V step, R _{USBn} + R _{AUn} = 1 kΩ			1.3	5.0	μs
t _{FPR}	Fault-protection recovery time	3.0	V _{COMn} = 5 V to 1 V step, R _{USBn} + R _{AUn} = 1 kΩ			-55		μs
t _{ON}	Turn on time	3.0	AUn to COMn	(V _{AOVR} = 0 V, V _{BUS} = 5.0 V to 0 V) or (V _{BUS} = 5.0 V, V _{AOVR} = 0 V to V _{CC})		55	85	μs
		3.0	USBn to COMn	V _{AOVR} = 0V, V _{BUS} = 0 V to 5.0 V		55	85	
t _{OFF}	Turn off time	3.0	AUn to COMn	(V _{AOVR} = 0 V, V _{BUS} = 0 V to 5.0 V) or (V _{BUS} = 5.0 V, V _{AOVR} = V _{CC} to 0 V)		1.4	5	μs
		3.0	USBn to COMn	(V _{AOVR} = 0 V, V _{BUS} = 5.0 V to 0 V) or (V _{BUS} = 5.0 V, V _{AOVR} = 0 V to V _{CC})		0.7	5	
t _D	Break-before-make time delay			R _L = 50 Ω		55		μs
t _{SK(0)}	Channel-to-channel skew					40		ps
t _{SK(P)}	Skew of opposite transition of the same output					40		ps
OIRR	OFF isolation ⁽⁷⁾		V _{COM} = 1 V _{RMS} , f = 100 kHz, R _S = R _L = 50 Ω			-65		dB
Xtalk	Crosstalk ⁽⁸⁾		V _{COM} = 1 V _{RMS} , f = 100 kHz, R _S = R _L = 50 Ω			-70		dB
THD + N	Total Harmonic Distortion + noise		AUn to COMn f = 20 Hz to 20 kHz, V _{COM} = 0.5 V _{PP} , DC bias = 0 V, R _L = 600 Ω			0.05		%
PSRR	Power supply rejection ratio	2.7 - 3.3	f = 10 kHz, R _{COMn} = 50 Ω			35		dB

Table 6. DC and AC characteristics (continued)

Symbol	Parameter	V _{CC} (V)	Test conditions ⁽¹⁾		Value			Unit
					Min.	Typ. ⁽²⁾	Max.	
BW	-3 dB bandwidth		AUn	R _S = R _L = 50 Ω signal = 0 dBm		850		MHz
			USBn			850		
C _{COM(ON)}	On capacitance		USBn to COMn	V _{COM} = 0.5V _{P-P} DC bias = 0 V, f = 240 MHz		8		pF
			AUn to COMn	V _{COM} = 0.5 V _{P-P} DC bias = 0 V, f = 1 MHz		8		
C _{AU(OFF)}	Audio channel off capacitance			V _{COM} = 0.5 V _{P-P} DC bias = 0 V, f = 1 MHz		8		pF
C _{USB(OFF)}	USB channel off capacitance			V _{COM} = 0.5 V _{P-P} DC bias = 0 V, f = 240 MHz		3.3		

1. Valid for ambient operating temperature: T_A = -40 to 85 °C, V_{CC} = 2.7 V to 4.5 V (except where noted).
2. Typical values are T_A = 25 °C.
3. When the voltage goes above V_{OVDT}, the switch turns off and protects the downstream circuits in case of a fault condition.
4. ΔR_{ON} = max ImSN-nSNI, where m and n = 1, 2 and N = 1, 2.
5. Guaranteed by design.
6. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
7. Off isolation = 20 Log₁₀ (V_D/V_S), V_D = output, V_S = input to off switch.
8. Between the two switches.

8 Package mechanical data

ECOPACK®

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Figure 5. Package outline for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch

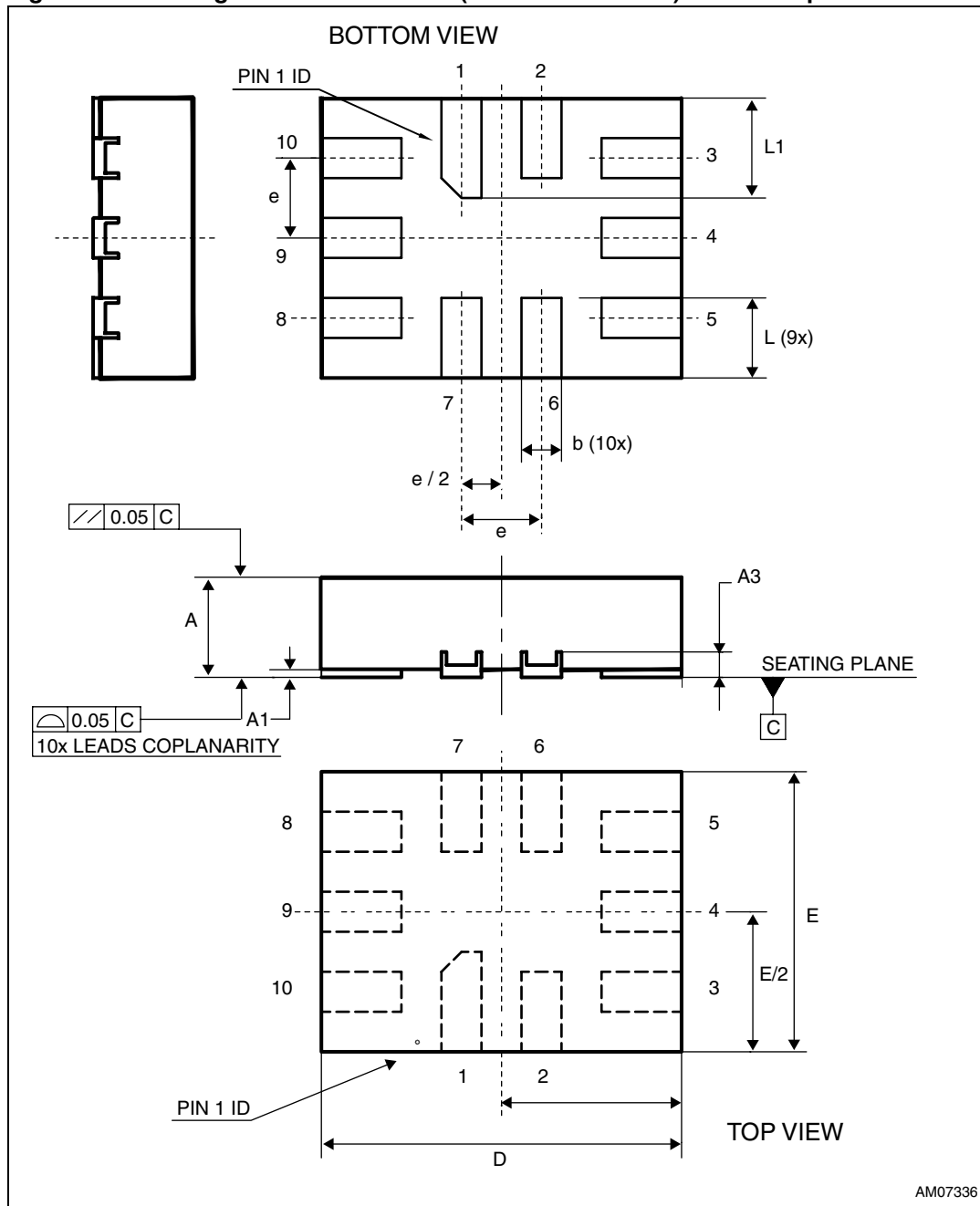


Table 7. Mechanical data for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch

Symbol	millimeters			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.50	0.55	0.0177	0.0197	0.0217
A1	0	0.02	0.05	0.0000	0.0008	0.0020
A3		0.127			0.0050	
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
D	1.75	1.80	1.85	0.0689	0.0709	0.0728
E	1.35	1.40	1.45	0.0531	0.0551	0.0571
e		0.40			0.0157	
L	0.35	0.40	0.45	0.0138	0.0157	0.0177
L1	0.45	0.50	0.55	0.0177	0.0197	0.0217

Figure 6. Recommended footprint for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch

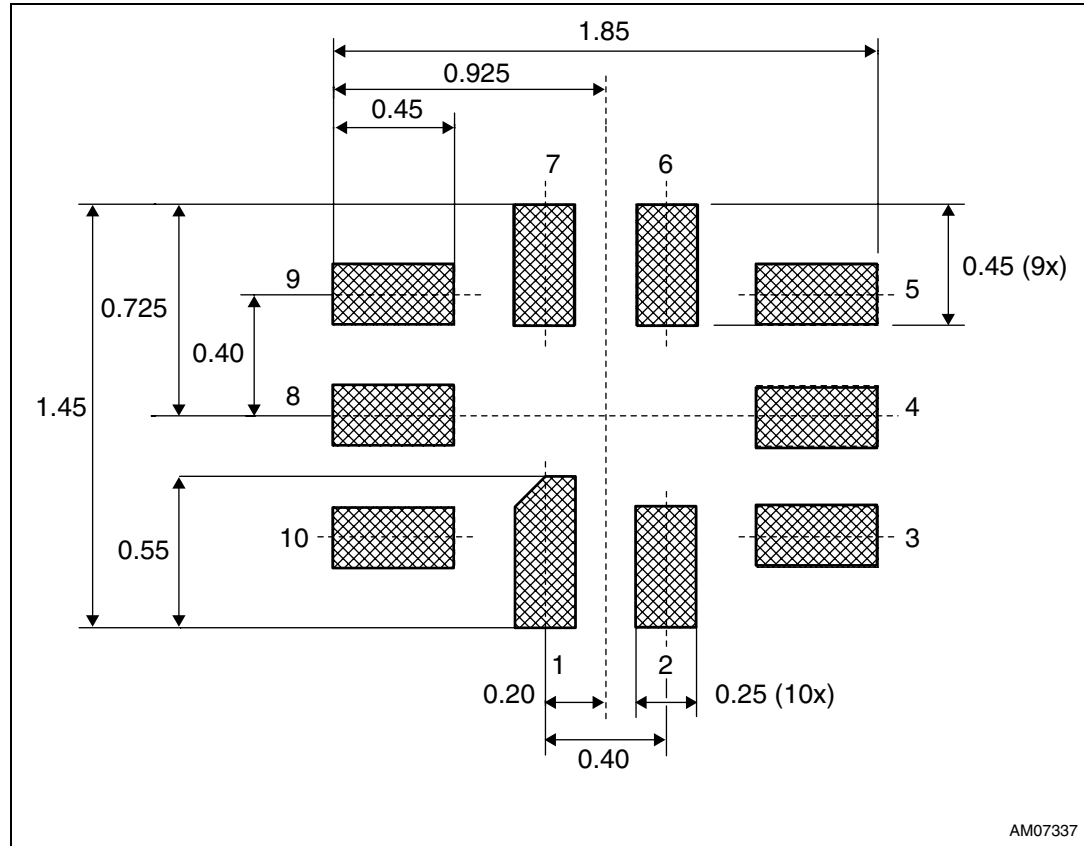


Figure 7. Carrier tape for QFN10 (1.8 x 1.4 x 0.5 mm)

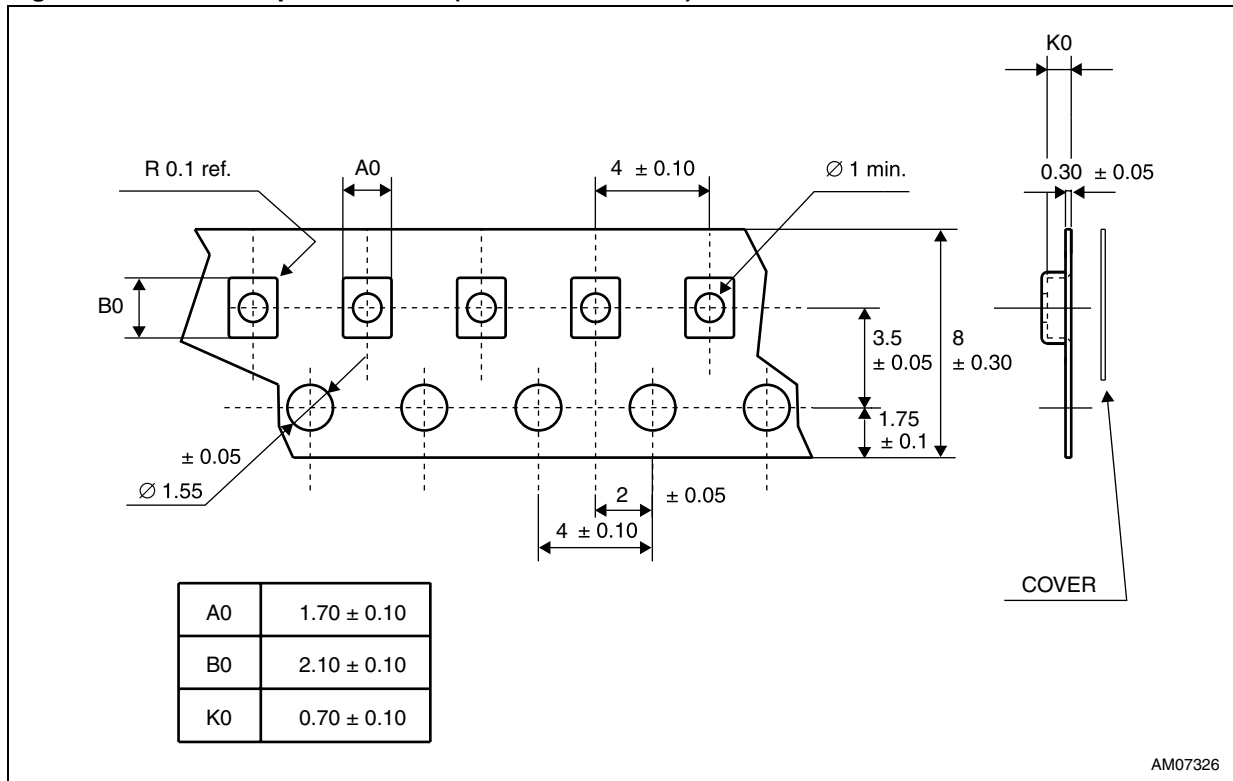


Figure 8. Reel information (front side) for QFN10 (1.8 x 1.4 x 0.5 mm)

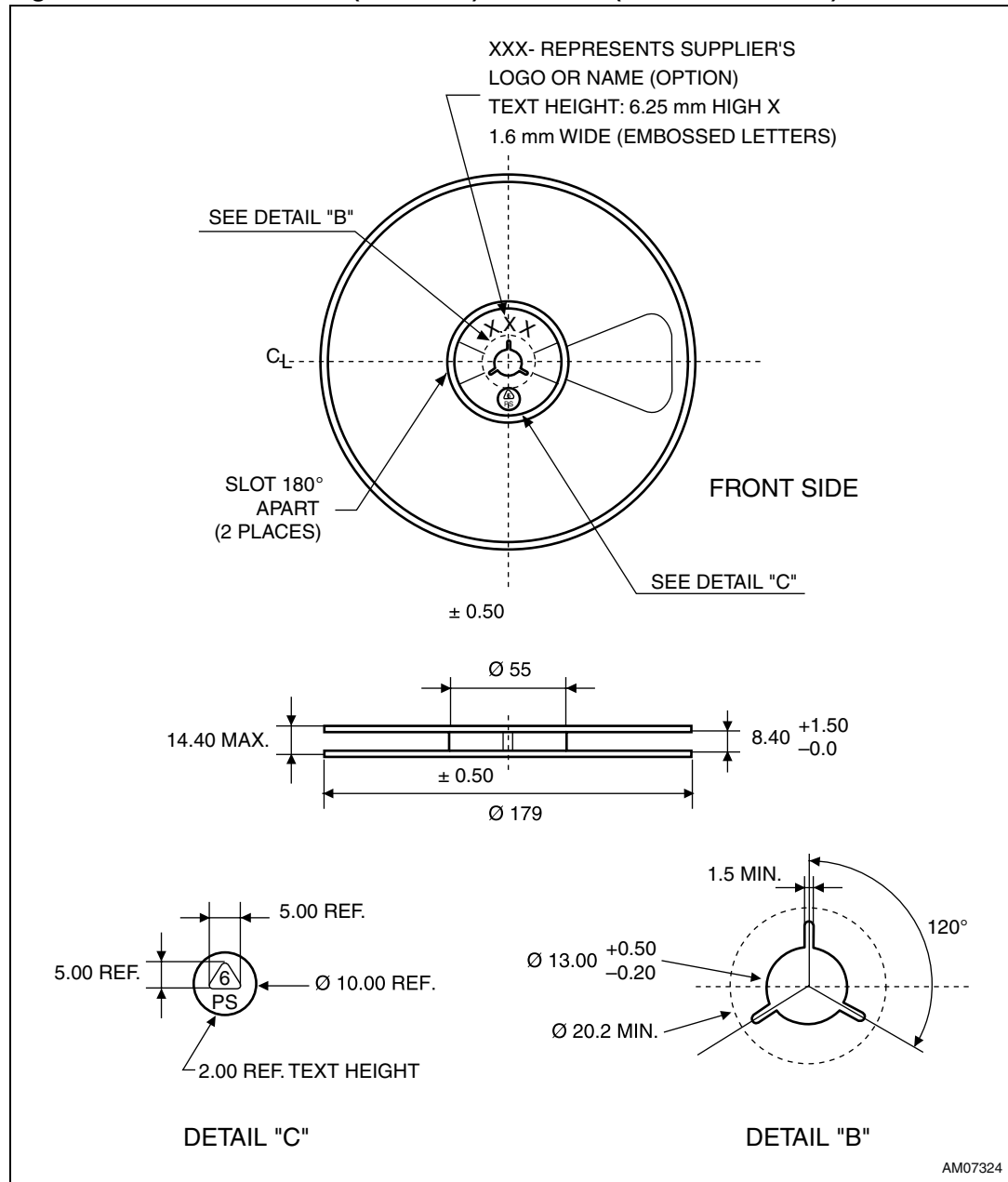
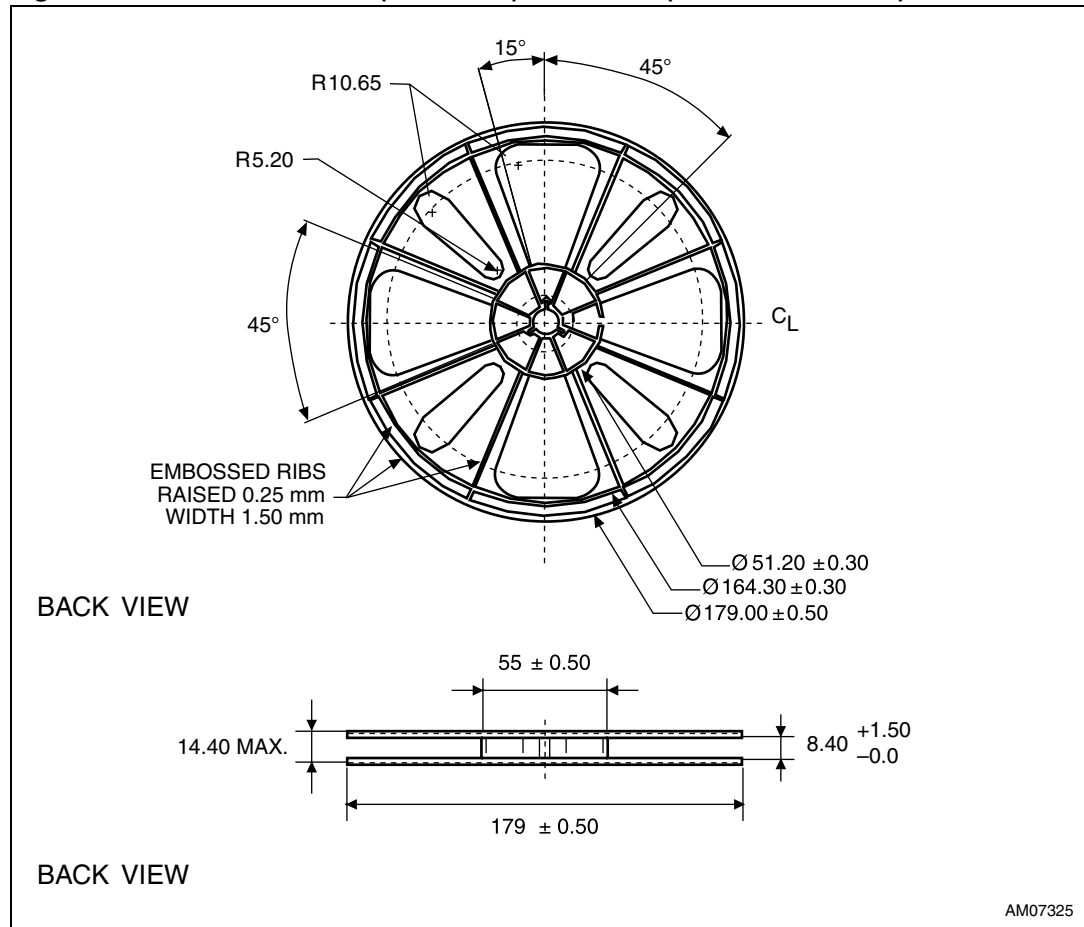
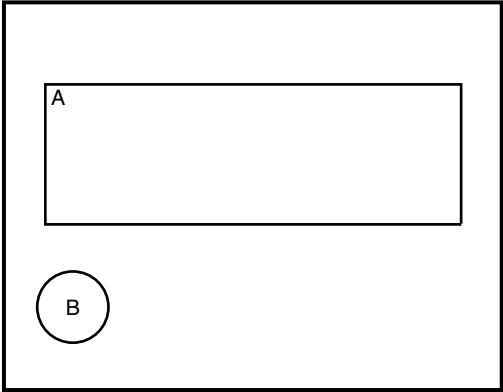


Figure 9. Reel information (back view) for QFN10 (1.8 x 1.4 x 0.5 mm)



9 Package marking information

Table 8. Device topside marking information

Step type marking		
Marking composition CD00155614 for V885 VFQFPN 10L 1.81 x 1.4 x 0.5 (pin1 dot at TLC)		
<p>PACKAGE FACE: TOP</p>  <p style="text-align: right; font-size: small;">AM07377</p>	<p>LEGEND</p> <ul style="list-style-type: none"> ■ Unmarkable surface □ Marking composition field <p>A - 47862 - MARKING AREA (123) B - 47861 - DOT</p>	
<p>CODE 47862</p>	<p>COMPOSN FLD TYPE MARKING AREA</p>	<p>MARKING VALUE U47</p>

10 Revision history

Table 9. Document revision history

Date	Revision	Changes
27-Oct-2010	1	Initial release.
26-Jan-2011	2	Updated Table 6 , corrected typo in Table 2 , Table 3 and Table 5 .

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