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STG3699B

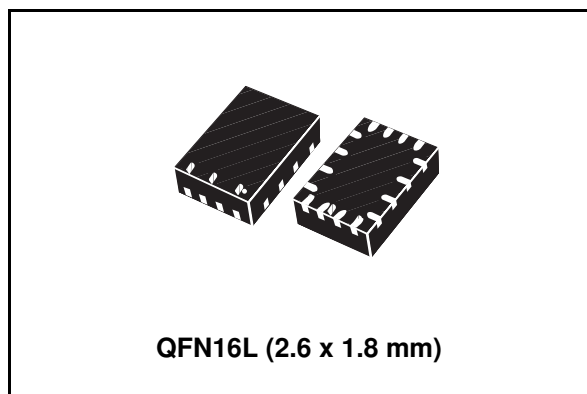
Low voltage 0.5 Ω max, quad SPDT switch
with break-before-make feature

Features

- High speed:
 - $t_{PD} = 1.5$ ns (typ.) at $V_{CC} = 3.0$ V
 - $t_{PD} = 1.5$ ns (typ.) at $V_{CC} = 2.3$ V
- Ultra low power dissipation:
 - $I_{CC} = 0.2$ μ A (max.) at $T_A = 85^\circ$ C
- Low ON resistance $V_{IN} = 0$ V:
 - $R_{ON} = 0.50$ Ω (max. $T_A = 25^\circ$ C) at $V_{CC} = 4.3$ V
 - $R_{ON} = 0.55$ Ω (max. $T_A = 25^\circ$ C) at $V_{CC} = 3.0$ V
 - $R_{ON} = 0.55$ Ω (max. $T_A = 25^\circ$ C) at $V_{CC} = 2.7$ V
- Wide operating voltage range:
 - V_{CC} (OPR) = 1.65 to 4.3 V single supply
- 4.3 V tolerant and 1.8 V compatible thresholds on digital control input at $V_{CC} = 2.3$ to 3.0 V
- Latch-up performance exceed 300 mA (JESD 17)
- ESD performance (analog chan. vs. GND):
HBM > 2 kV (MIL STD 883 method 3015)

Description

The STG3699B is a high-speed CMOS low voltage quad analog SPDT (single-pole double-throw) switch or 2:1 multiplexer/demultiplexer switch fabricated using silicon gate C²MOS technology. Designed to operate from 1.65 to 4.3 V, this device is ideal for portable applications.



It offers very low ON resistance ($R_{ON} < 0.5$ Ω) at $V_{CC} = 3.0$ V. The n_{IN} inputs are provided to control the independent channel switches $nS1$ and $nS2$. The switches $nS1$ are ON (connected to common ports D_n) when the n_{IN} input is held high and OFF (state of high impedance exists between the two ports) when n_{IN} is held low. The switches $nS2$ are ON (connected to common ports D_n) when the n_{IN} input is held low and OFF (state of high impedance exists between the two ports) when IN is held high. Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD and excess transient voltage immunity.

The STG3699B is available in the commercial temperature range of -40 to 125° C in a QFN16L, 2.6 x 1.8 mm package.

Table 1. Device summary

Order code	Temperature range	Package	Packaging
STG3699BVTR	-40 to 125° C	QFN16L (2.6 x 1.8 mm)	Tape and reel

Contents

1	Summary description	3
	1.1 Pin connection	3
2	Maximum rating	5
3	DC and AC parameters	6
4	Typical application	9
5	Test circuit	10
6	Waveforms	11
7	Package mechanical data	14
8	Revision history	17

1 Summary description

1.1 Pin connection

Figure 1. Connections diagram (top through view)

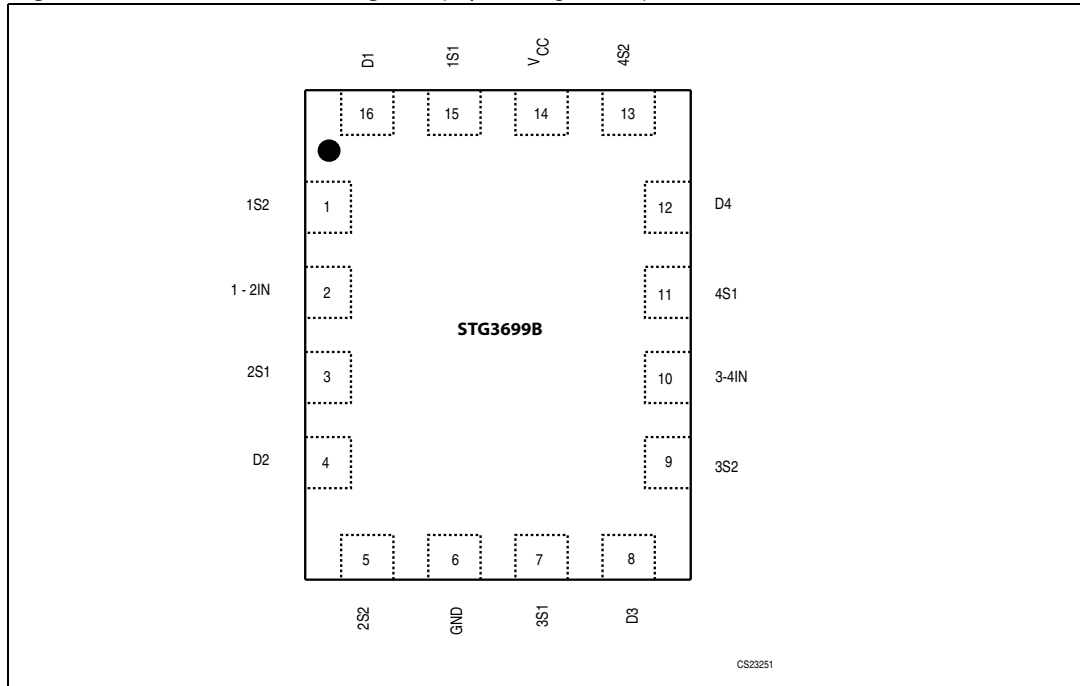


Table 2. Pin description

Pin N°	Symbol	Name and function
15, 3, 7, 11, 1, 5, 9, 13	1S1 to 4S1, 1S2 to 4S2	Independent channels switches
16, 4, 8, 12	D1 to D4	Common channels
2, 10	1-2IN, 3-4IN	Input controls
14	V _{CC}	Positive supply voltage
6	GND	Ground (0V)

Figure 2. Input equivalent circuit

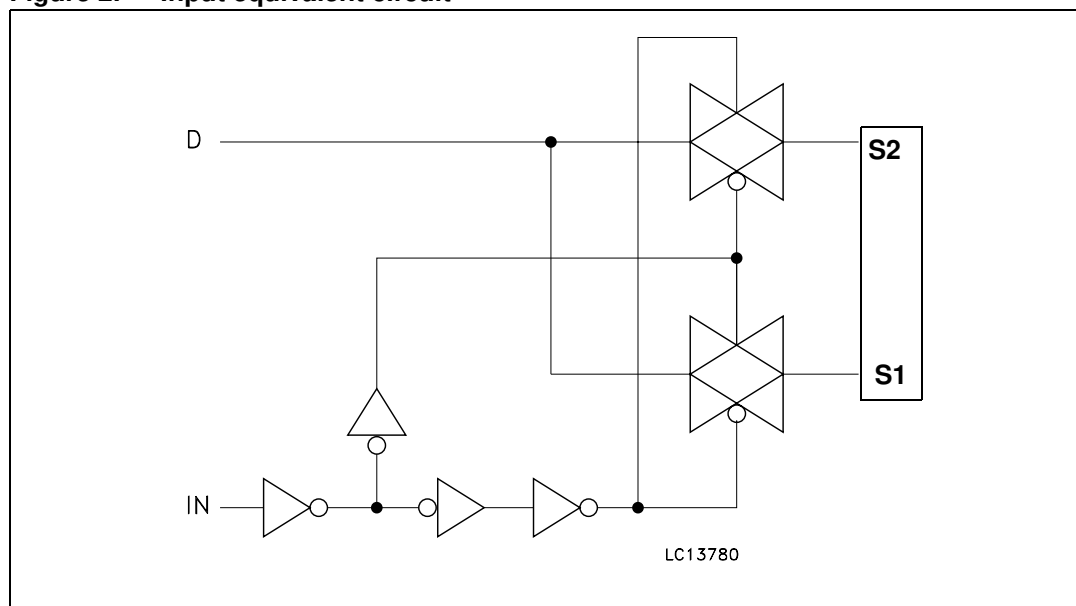


Table 3. Truth table

1-2IN	3-4IN	ON switches
L	-	1S2-D1, 2S2-D2
H	-	1S1-D1, 2S1-D2
-	L	3S2-D3, 4S2-D4
-	H	3S1-D3, 4S1-D4

2 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IKC}	DC input diode current on control pin ($V_{IN} < 0$ V)	-50	mA
I_{IK}	DC input diode current ($V_{IN} < 0$ V)	± 50	mA
I_{OK}	DC output diode current	± 50	mA
I_O	DC output current	± 300	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	± 500	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	± 100	mA
P_D	Power dissipation at $T_A = 70^\circ\text{C}$ ⁽¹⁾	1120	mW
T_{STG}	Storage temperature	-65 to 150	$^\circ\text{C}$
T_L	Lead temperature (10 sec)	300	$^\circ\text{C}$

1. Derate above 70°C : by 18.5mW/ $^\circ\text{C}$.

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit	
V_{CC}	Supply voltage (truth table guaranteed: 1.2 to 4.3 V)	1.65 to 4.3	V	
V_I	Input voltage	0 to V_{CC}	V	
V_{IC}	Control input voltage	0 to 4.3	V	
V_O	Output voltage	0 to V_{CC}	V	
T_{OP}	Operating temperature	-55 to 125	$^\circ\text{C}$	
dt/dv	Input rise and fall time control input	$V_{CC} = 1.65$ to 2.7 V	0 to 20	ns/V
		$V_{CC} = 3.0$ to 4.3 V	0 to 10	

3 DC and AC parameters

Table 6. DC specification

Symbol	Parameter	V _{CC} (V)	Test condition	Value						Unit	
				T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min		Max
V _{IH}	High level input voltage	1.65 – 1.95		0.65 V _{CC}			0.65 V _{CC}		0.65 V _{CC}		V
		2.3 – 2.5		1.2			1.2		1.2		
		2.7 – 3.0		1.3			1.3		1.3		
		3.3		1.4			1.4		1.4		
		3.6		1.5			1.5		1.5		
		4.3		1.6			1.6		1.6		
V _{IL}	Low level input voltage	1.65 – 1.95				0.25		0.25		0.25	V
		2.3 – 2.5				0.25		0.25		0.25	
		2.7 – 3.0				0.25		0.25		0.25	
		3.3				0.30		0.30		0.30	
		3.6				0.30		0.30		0.30	
		4.3				0.40		0.40		0.40	
R _{ON}	Switch ON resistance	4.3	V _S = 0 V to V _{CC} I _S = 100 mA		0.35	0.50		0.60			Ω
		3.0			0.45	0.55		0.65			
		2.7			0.45	0.55		0.65			
		2.3			0.45	0.70		0.80			
		1.8			0.55	1.5		2.0			
		1.65			0.65	1.5		2.0			
ΔR _{ON}	ON resistance match between channels ⁽¹⁾	2.7	V _S at R _{ON} max I _S = 100 mA		0.15						Ω
R _{FLAT}	ON resistance flatness ⁽²⁾	4.3	V _S = 0 V to V _{CC} I _S = 100 mA		0.15	0.20		0.20			Ω
		3.0			0.20	0.25		0.25			
		2.7			0.20	0.25		0.25			
		2.3			0.20	0.25		0.25			
		1.65			0.32	0.42		0.42			
I _{OFF}	OFF state leakage current (nSn), (Dn)	4.3	V _S = 0.3 or 4 V			±20		±100			nA

Table 6. DC specification (continued)

Symbol	Parameter	V _{CC} (V)	Test condition	Value						Unit	
				T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min		Max
I _{IN}	Input leakage current	0 – 4.3	V _{IN} = 0 to 4.3V			±0.1		±1			μA
I _{CC}	Quiescent supply current	1.65 – 4.3	V _{IN} = V _{CC} or GND			±0.05		±0.2		±1	μA
I _{CCLV}	Quiescent supply current low voltage driving	4.3	V _{1-2IN} , V _{3-4IN} = 1.65 V		±37	±50		±100			μA
			V _{1-2IN} , V _{3-4IN} = 1.80 V		±33	±40		±50			
			V _{1-2IN} , V _{3-4IN} = 2.60 V		±12	±20		±30			

1. ΔR_{ON} = R_{ON(Max)} – R_{ON(Min)}
2. Flatness is defined as the difference between the maximum and minimum value of ON resistance as measured over the specified analog signal ranges.

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, t_r = t_f ≤ 5 ns)

Symbol	Parameter	V _{CC} (V)	Test condition	Value						Unit	
				T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min		Max
t _{PLH} , t _{PHL}	Propagation delay	1.65 – 1.95	V _I = OPEN		0.45						ns
		2.3 – 2.7			0.40						
		3.0 – 3.3			0.30						
		3.6 – 4.3			0.30						
t _{ON}	Turn-ON time	1.65 – 1.95	V _S = 0.8 V		120						ns
		2.3 – 2.7	V _S = 1.5 V		45	55		65			
		3.0 – 3.3			42	55		65			
		3.6 – 4.3			40	55		65			
t _{OFF}	Turn-OFF time	1.65 – 1.95	V _S = 0.8 V		22						ns
		2.3 – 2.7	V _S = 1.5 V		18	30		40			
		3.0 – 3.3			16	30		40			
		3.6 – 4.3			15	30		40			

Table 7. AC electrical characteristics ($C_L = 35 \text{ pF}$, $R_L = 50 \text{ } \Omega$, $t_r = t_f \leq 5 \text{ ns}$) (continued)

Symbol	Parameter	V _{CC} (V)	Test condition	Value						Unit	
				T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min		Max
t _D	Break-before- make time delay	1.65 – 1.95	C _L = 35 pF R _L = 50 Ω V _S = 1.5 V		53					ns	
		2.3 – 2.7			28						
		3.0 – 3.3			12						
		3.6 – 4.3			8						
Q	Charge injection	1.65 – 1.95	C _L = 100 pF R _L = 1 MΩ V _{GEN} = 0 V R _{GEN} = 0 Ω		42					pC	
		2.3 – 2.7			48						
		3.0 – 3.3			48						
		3.6 – 4.3			57						

Table 8. Analog switch characteristics ($C_L = 5 \text{ pF}$, $R_L = 50 \text{ } \Omega$, T_A = 25°C)

Symbol	Parameter	V _{CC} (V)	Test condition	Value						Unit	
				T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min		Max
OIRR	Off Isolation (1)	1.65 – 4.3	V _S = 1V _{RMS} f = 100 kHz		-71						dB
Xtalk	Crosstalk	1.65 – 4.3	V _S = 1 V _{RMS} f = 100 kHz		-72						dB
THD	Total harmonic distortion	2.3 – 4.3	R _L = 600 Ω V _{IN} = 2V _{PP} f = 20 Hz to 20 kHz		0.03						%
BW	-3dB Bandwidth	1.65 – 4.3	R _L = 50 Ω		40						MHz
C _{IN}	Control pin input capacitance				5						pF
C _{Sn}	Sn port capacitance	3.3	f = 1 MHz		80						
C _D	D port capacitance when switch is enabled	3.3	f = 1 MHz		170						

1. Off-isolation = 20 log₁₀ (V_D/V_S), V_D = output, V_S = input to off switch

4 Typical application

Figure 3. ON resistance

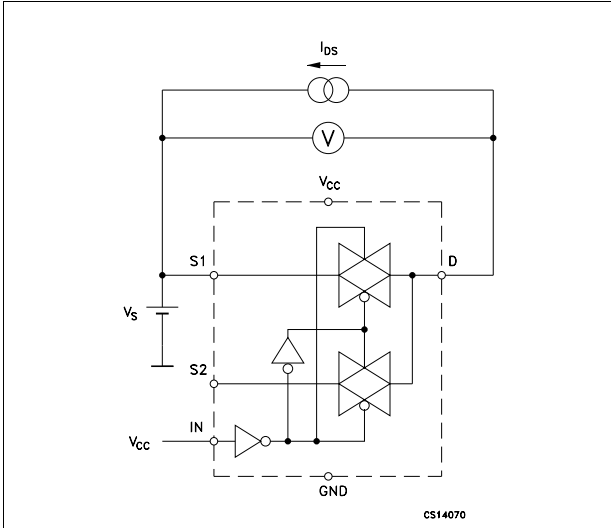


Figure 4. Bandwidth

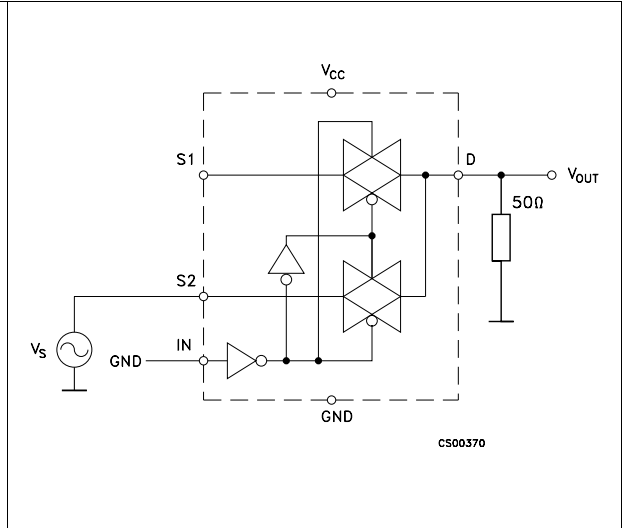


Figure 5. OFF leakage

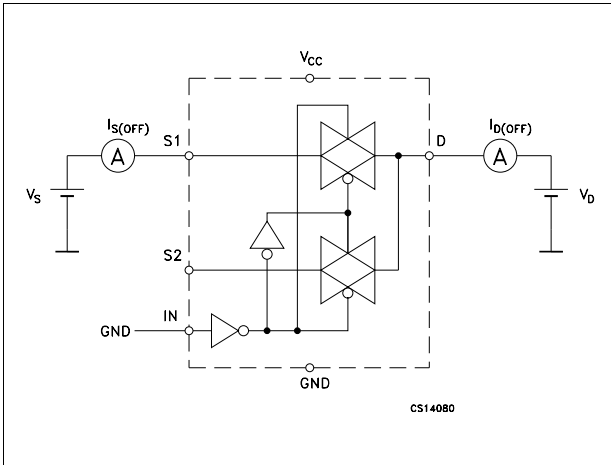


Figure 6. Channel-to-channel crosstalk

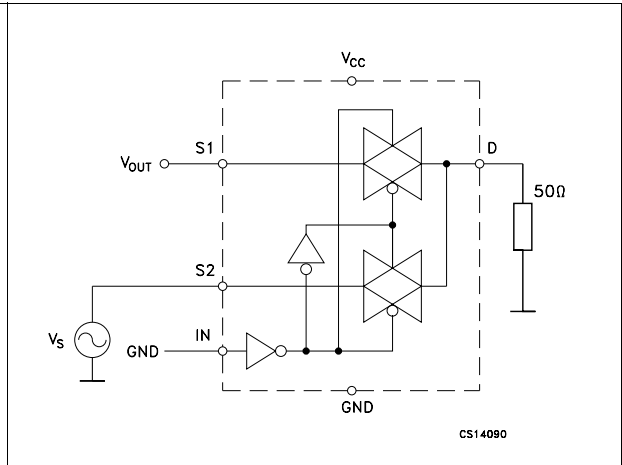
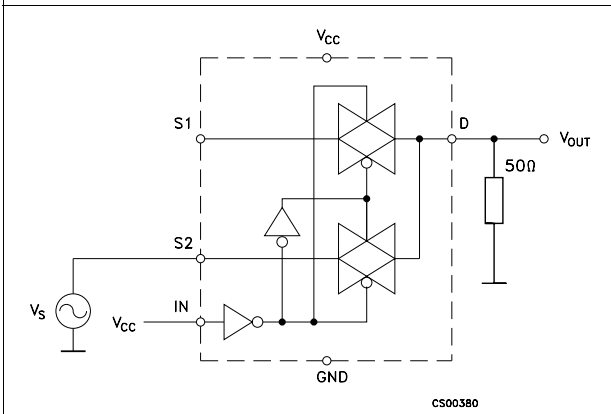
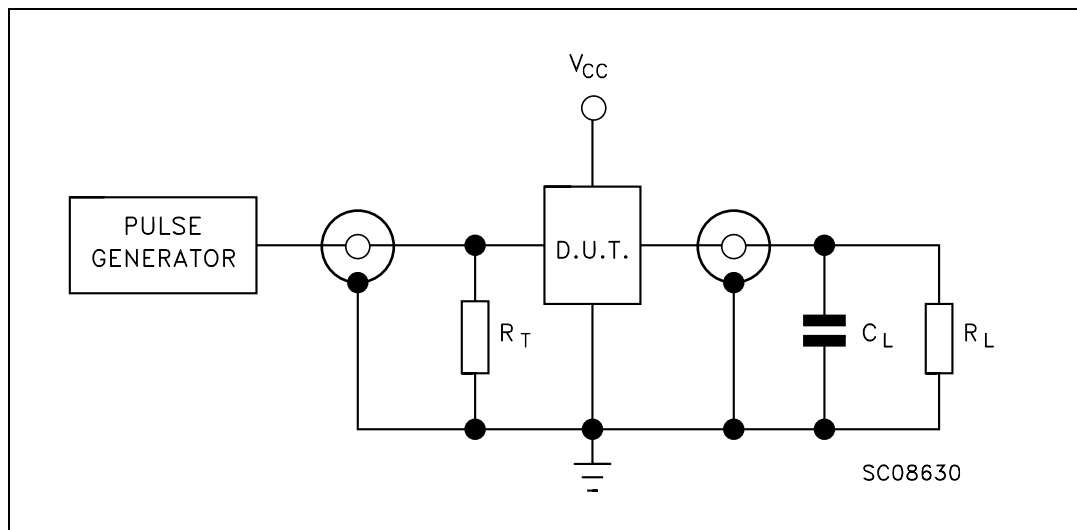


Figure 7. OFF isolation



5 Test circuit

Figure 8. Test circuit



$C_L = 5/35$ pF or equivalent (includes jig and probe capacitance)

$R_L = 50 \Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

6 Waveforms

Figure 9. Break-before-make time delay

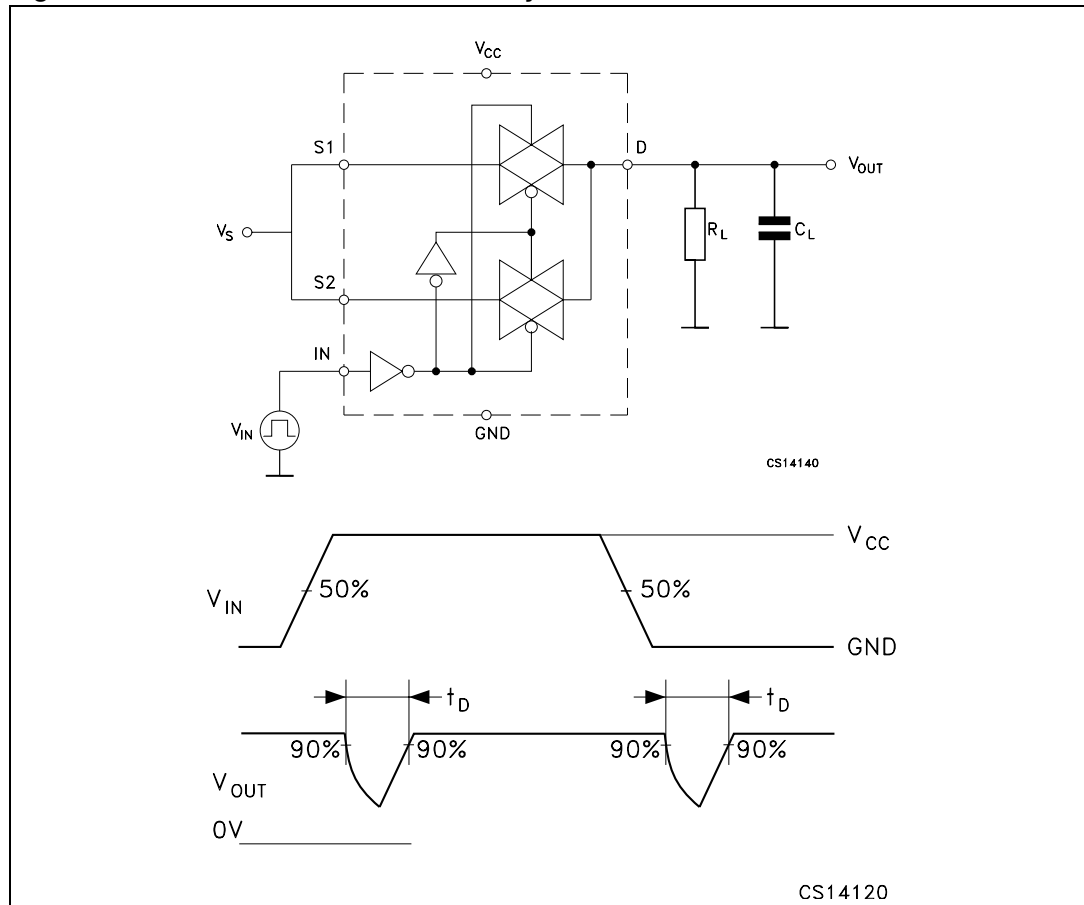
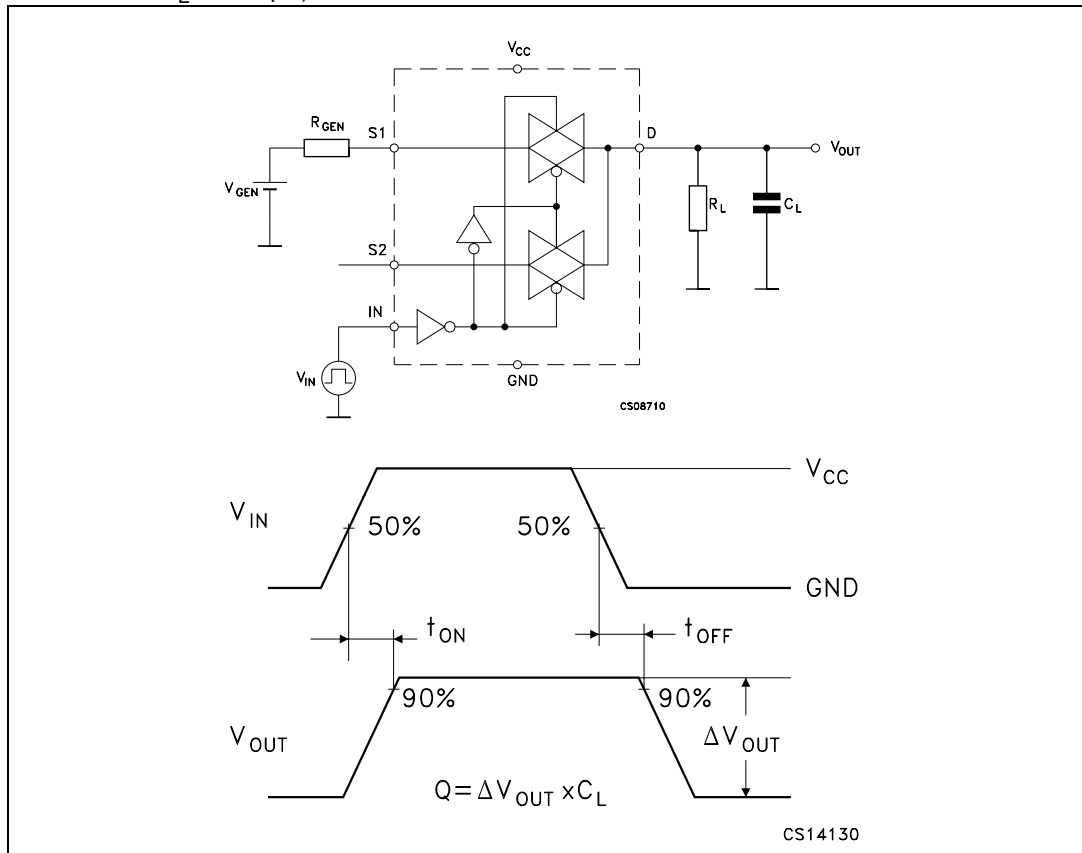


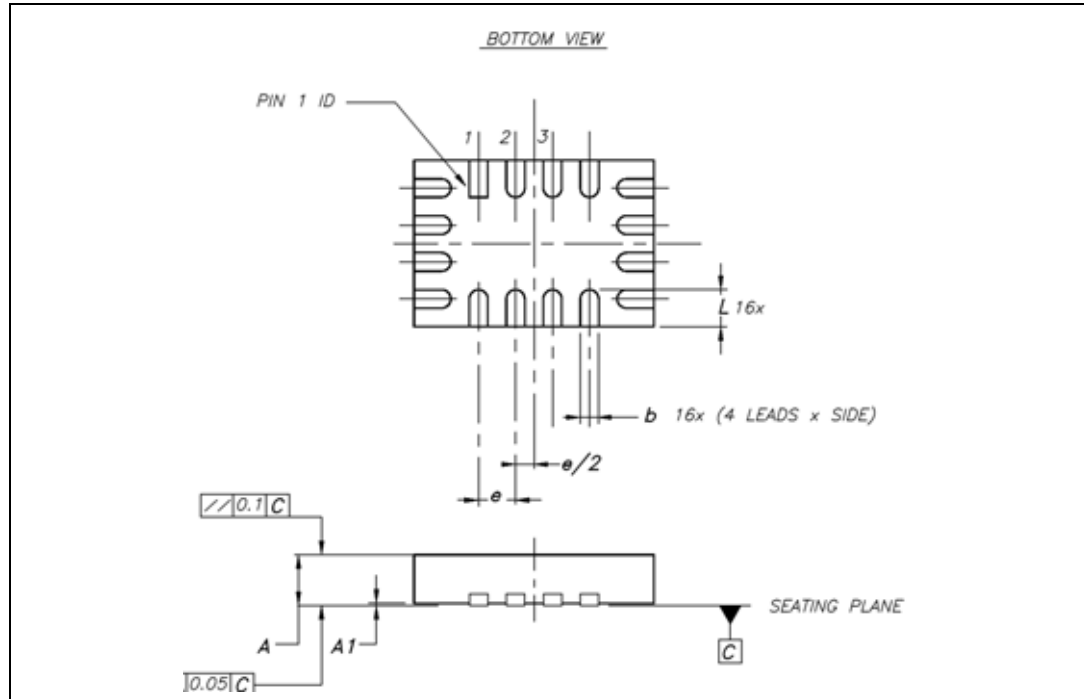
Figure 10. Switching time and charge injection ($V_{GEN} = 0\text{ V}$, $R_{GEN} = 0\ \Omega$, $R_L = 1\text{ M}\Omega$, $C_L = 100\text{ pF}$)



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 12. QFN16L (2.6 x 1.8 mm) package outline

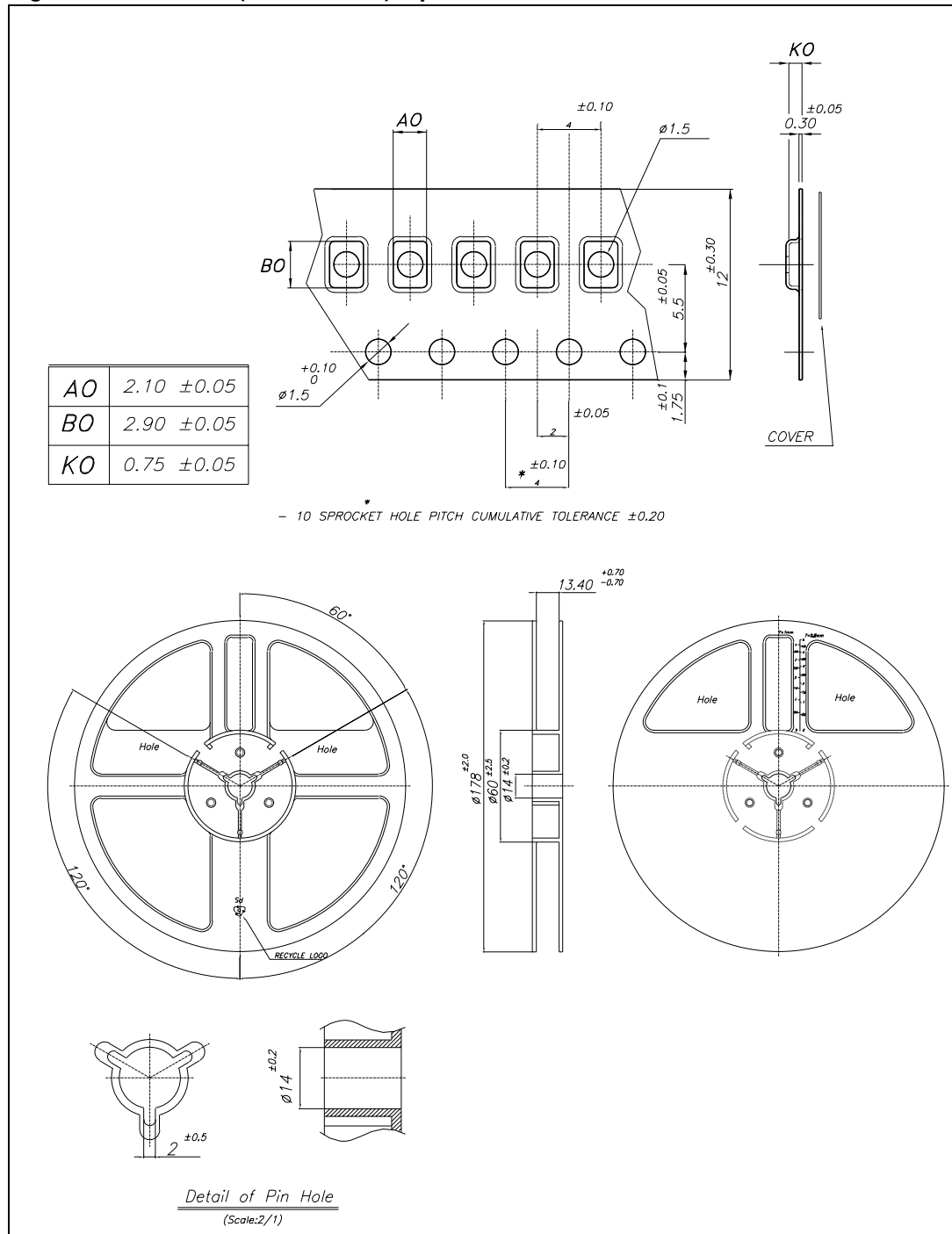


1. Drawing not to scale.

Table 9. QFN16L (2.6 x 1.8 mm) mechanical data

Dimensions			
Symbol	Databook (mm)		
	Nom	Min	Max
A	0.55	0.45	0.60
A1	0.02	0	0.05
b	0.20	0.15	0.25
D	2.60	2.50	2.70
E	1.80	1.70	1.90
e	0.40		
L	0.40	0.35	0.45

Figure 14. QFN16L (2.6 x 1.8 mm) tape & reel information



8 Revision history

Table 10. Document revision history

Date	Revision	Changes
13-Oct-2005	1	First Release.
21-Dec-2005	2	Added tape & reel information.
17-Feb-2006	3	R _{FLAT} updated in Table 6: DC specification on page 6 .
10-Aug-2006	4	New template, Table 1 updated.
19-Feb-2007	5	Updated OIRR, Xtalk values in Table 8 on page 8 .
4-Sept-2007	6	Updated I _{OK} value in Table 4 on page 5 , small text changes, restructured layout.

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