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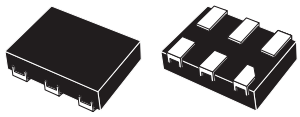
STG5123

Low voltage 1 Ω single SPDT switch with break-before-make feature

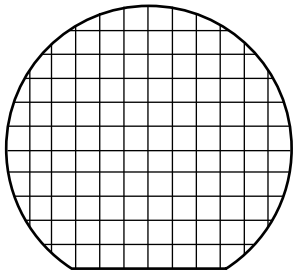
Datasheet – production data

Features

- High speed:
  - t_{PD} = 130 ps (typ.) at V_{CC} = 3.0 V
  - t_{PD} = 140 ps (typ.) at V_{CC} = 2.3 V
- Ultra low power dissipation:
  - I_{CC} = 0.2 µA (max.) at T_A = 85 °C
- Low ON-resistance:
  - R_{ON} = 1.0 Ω (typ.) at V_{CC} = 4.5 V
  - R_{ON} = 1.2 Ω (typ.) at V_{CC} = 3.0 V
  - R_{ON} = 2.0 Ω (typ.) at V_{CC} = 1.8 V
- Wide operating voltage range:
  - V_{CC} (opr.) = 1.65 to 4.5 V single supply
- 5 V tolerant and 1.8 V compatible threshold ON digital control input at V_{CC} = 1.65 to 4.5 V
- Latch-up performance exceeds 200 mA per JESD 78, Class II
- ESD performance tested per JESD 22
  - 2000 V human-body model (A114-B, Class II)
  - 200 V machine model (A115-A)
  - 1000 V charged-device model (C101)



DFN6L



Wafer

Description

The STG5123 is a high speed CMOS low voltage single analog SPDT (single-pole double-throw) switch or 2:1 multiplexer/demultiplexer switch manufactured using silicon gate C^2MOS technology. Designed to operate from a 1.65 to 4.5 V supply, this device is ideal for portable applications.

The device offers very low ON-resistance (1 Ω) at V_{CC} = 4.5 V. Switch S1 is ON (connected to common ports Dn) when the SEL input is held high, and OFF (state of high impedance exists between the two ports) when SEL is held low.

Switch S2 is ON (connected to common port D) when the SEL input is held low, and OFF (state of high impedance exists between the two ports) when SEL is held high.

Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits to protect against static discharge, giving them immunity from ESD and transient excess voltage.

Table 1. Device summary

Order code	Package	Packaging
STG5123DTR	DFN6L (1.2 x 1 mm)	Tape and reel
JSTG5123-CD1		Unsawn wafer

Contents

List of tables

List of figures

1 Pin connections and functions

Figure 1. Pin connections (top through view)

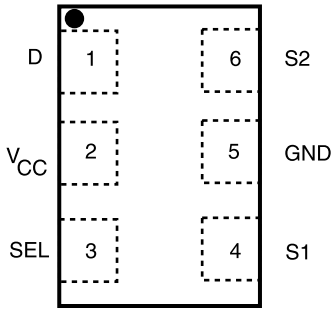


Table 2. Pin descriptions

Pin number	Symbol	Name and function
4	S1	Independent channel
6	S2	Independent channel
1	D	Common channels
3	SEL	Control
2	V_{CC}	Positive supply voltage
5	GND	Ground (0 V)

Figure 2. Input equivalent circuit

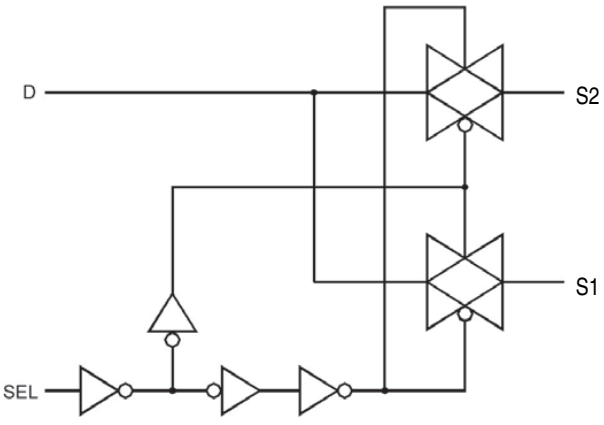


Table 3. Truth table

Sel	Switch S1	Switch S2
H	ON	OFF(1)
L	OFF(1)	ON

1. High impedance.

2 Electrical ratings

Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 5: Recommended operating conditions* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics™ SURE program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	–0.5 to 5.5	V
V_I	DC input voltage	–0.5 to V_{CC} +0.5	V
V_{IC}	DC control input voltage	–0.5 to 5.5	V
V_O	DC output voltage	–0.5 to V_{CC} +0.5	V
I_{IKC}	DC input diode current on control pin (V_{SEL} < 0 V)	–50	mA
I_{IK}	DC input diode current (V_{IN} < 0 V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±200	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	±400	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70 °C(1)	1120	mW
T_{STG}	Storage temperature	–65 to 150	°C
T_L	Lead temperature (10 s)	300	°C

1. Derate above 70 °C by 18.5 mW/°C.

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.5	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.5	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		–40 to 85	°C
dt/dv	Input rise and fall time control input	V_{CC} = 1.65 to 2.7 V	0 to 20	ns/V
		V_{CC} = 3.0 to 4.5 V	0 to 10	

3 Electrical characteristics

3.1 DC electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High level input voltage	1.65 – 1.95		0.65 V_{CC}			0.65 V_{CC}		V
		2.3 – 2.5		1.2			1.2		
		2.7 – 3.0		1.3			1.3		
		3.3 – 3.6		1.4			1.4		
		4.5		1.6			1.6		
V_{IL}	Low level input voltage	1.65 – 1.95				0.40		0.40	V
		2.3 – 2.5				0.60		0.60	
		2.7 – 3.0				0.60		0.60	
		3.3 – 3.6				0.60		0.60	
		4.5				0.80		0.80	
R_{ON}	Switch ON-resistance	1.8	V_S = 0 V to V_{CC} I_S = 100 mA		2.0	3.0		3.5	Ω
		2.7			1.3	1.6		1.8	
		3.0			1.2	1.5		1.7	
		4.5			1.0	1.2		1.4	
ΔR_{ON}	ON-resistance match between channels(1)	1.8	V_S at R_{ON} max I_S = 100 mA		0.06				Ω
		2.7			0.05				
		3.0			0.05				
		4.5			0.05				
R_{FLAT}	ON-resistance flatness(2)	1.8	V_S = 0 V to V_{CC} I_S = 100 mA		1.0	1.5		1.5	Ω
		2.7			0.45	0.60		0.70	
		3.0			0.43	0.50		0.60	
		4.5			0.39	0.50		0.60	
I_{OFF}	OFF state leakage current (Sn), (D)	4.3	V_S = 0.3 or 4 V			±20		±100	nA
I_{IN}	Input leakage current	0 – 4.5	V_{SEL} = 0 to 4.5 V			±0.1		±1.0	µA
I_{CC}	Quiescent supply current	1.65 – 4.5	V_{SEL} = V_{CC} or GND			±0.1		±1.0	µA

Table 6. DC specifications (continued)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
I_{CCLV}	Quiescent supply current low voltage driving	4.3	V_{SEL} = 1.65 V		±17	±35		±70	µA
		4.3	V_{SEL} = 1.80 V		±15	±30		±60	
		4.3	V_{SEL} = 2.60 V		±5	±10		±20	

1. $\Delta R_{ON} = R_{ON(Max)} - R_{ON(Min)}$.
2. Flatness is defined as the difference between the maximum and minimum value of ON-resistance as measured over the specified analog signal ranges.

3.2 AC electrical characteristics

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, $t_r = t_f \leq 5$ ns)

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				T_A = 25 °C			– 40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation delay	1.65 – 1.95			0.15				ns
		2.3 – 2.7			0.14				
		3.0 – 3.3			0.13				
		3.6 – 5.0			0.13				
t_{ON}	Turn-ON time	1.65 – 1.95	V_S = 0.8 V		36				ns
		2.3 – 2.7	V_S = 1.5 V		31	40		45	
		3.0 – 3.3			24	31		40	
		3.6 – 5.0			21	28		32	
t_{OFF}	Turn-OFF time	1.65 – 1.95	V_S = 0.8 V		29				ns
		2.3 – 2.7	V_S = 1.5 V		17	27		37	
		3.0 – 3.3			12	23		33	
		3.6 – 5.0			11	21		31	
t_D	Break-before-make time delay	1.65 – 1.95	C_L = 35 pF, R_L = 50 Ω, V_S = 1.5 V		15				ns
		2.3 – 2.7			10				
		3.0 – 3.3			8				
		3.6 – 5.0			6				
Q	Charge injection	1.65	C_L = 100 pF, V_{GEN} = 0 V, R_{GEN} = 0 Ω		16				pC
		2.3			22				
		3			26				
		5.0			33				

3.3 Analog switch characteristics

Table 8. Analog switch characteristics (C_L = 5 pF, R_L = 50 Ω, T_A = 25 °C)

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
OIRR	OFF isolation(1)	1.65 – 5.0	V_S = 1 V_{RMS} f = 100 kHz		– 75				dB
Xtalk	Crosstalk	1.6 – 5.0	V_S = 1 V_{RMS} f = 100 kHz		– 80				dB
THD	Total harmonic distortion	2.3 – 5.0	R_L = 600 Ω V_S = 2 V_{PP} f = 20 Hz to 20 kHz		0.03				%
BW	-3 dB bandwidth	1.65 – 5.0	R_L = 50 Ω		150				MHz
C_{IN}	Control pin input capacitance				6				pF
C_{ON}	Sn port capacitance when switch is enabled	3.3	f = 1 MHz		52				
C_{OFF}	Sn port capacitance when switch is disabled	3.3	f = 1 MHz		25				
C_D	D port capacitance when switch is enabled	3.3	f = 1 MHz		50				

1. OFF isolation = 20 $\log_{10}$ (V_D/V_S), V_D = output. V_S = input to OFF switch.

4 Test circuits

Figure 3. ON-resistance

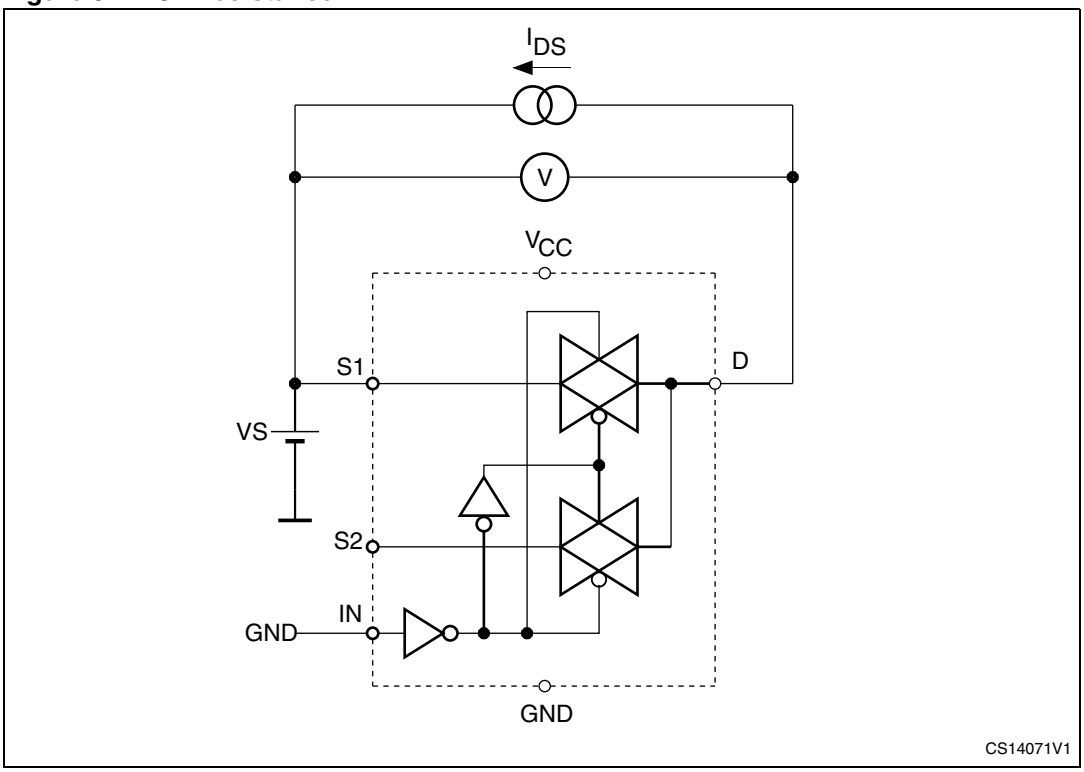


Figure 4. Bandwidth

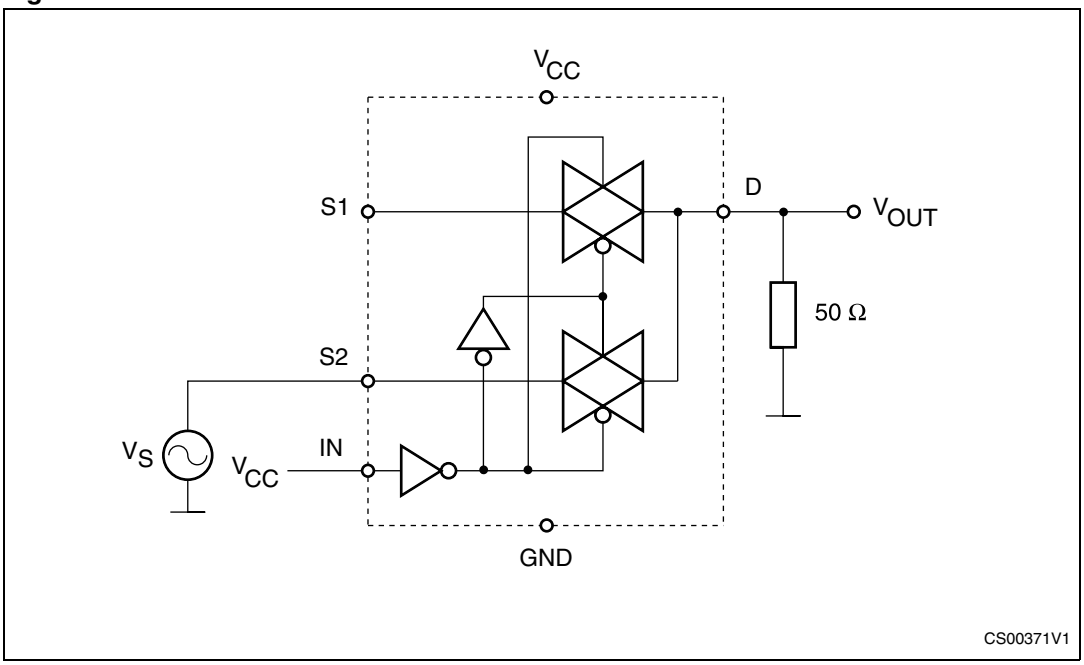


Figure 5. OFF leakage

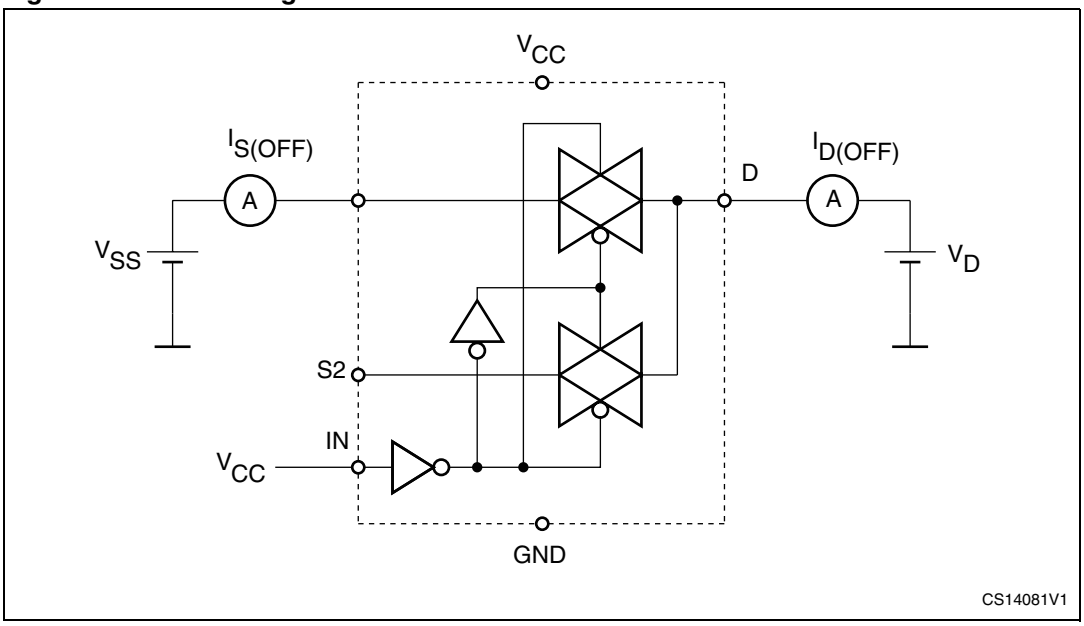


Figure 6. Channel-to-channel crosstalk

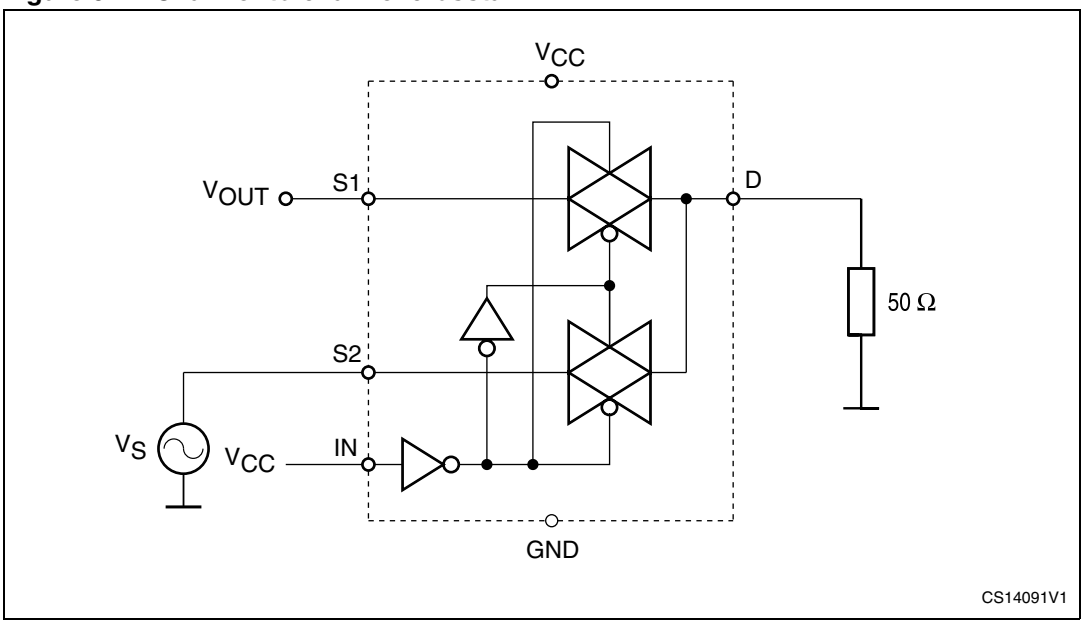


Figure 7. OFF isolation

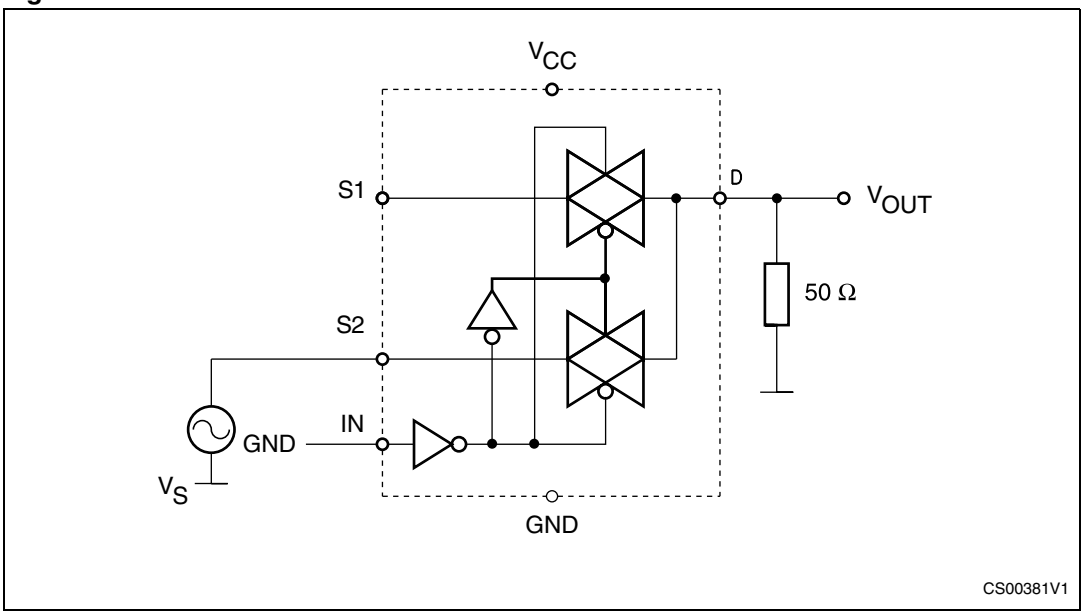
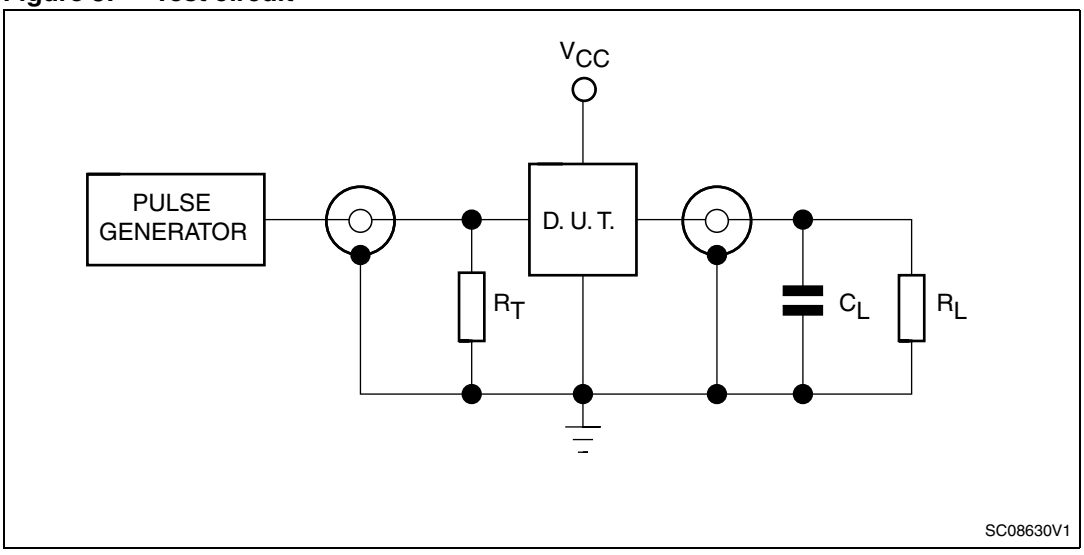


Figure 8. Test circuit



1. C_L = 5/35 pF or equivalent: (includes jig capacitance).
2. R_L = 50 Ω or equivalent.
3. R_T = Z_{OUT} of pulse generator (typically 50 Ω).

Figure 9. Break-before-make time delay

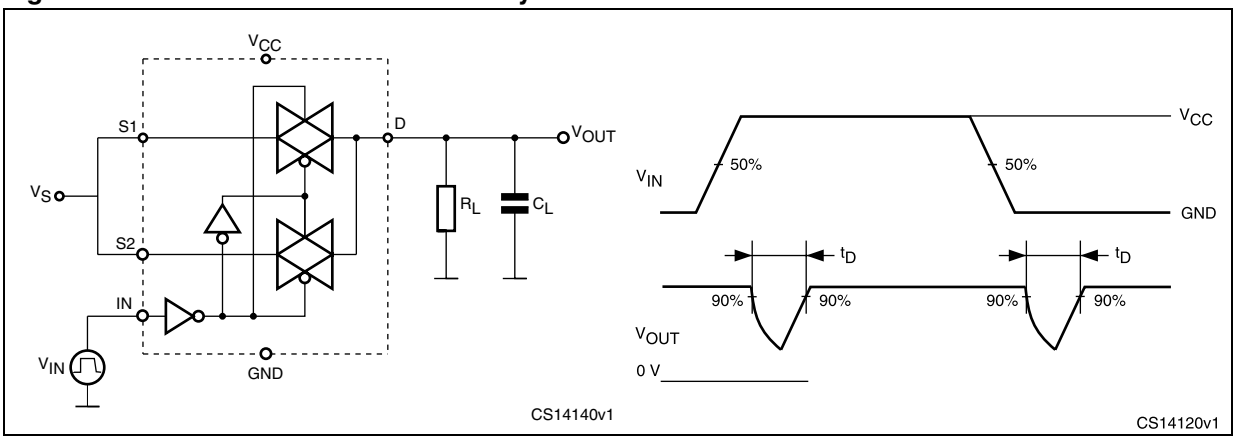


Figure 10. Switching time and charge injection (V_{GEN} = 0 V, R_{GEN} = 0 Ω, R_L = 1 MΩ, C_L = 100 pF)

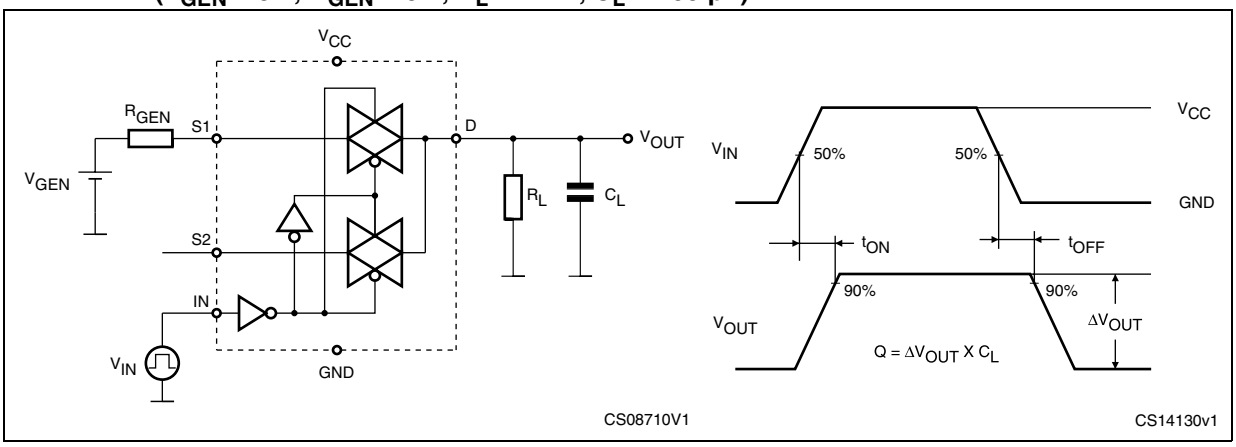
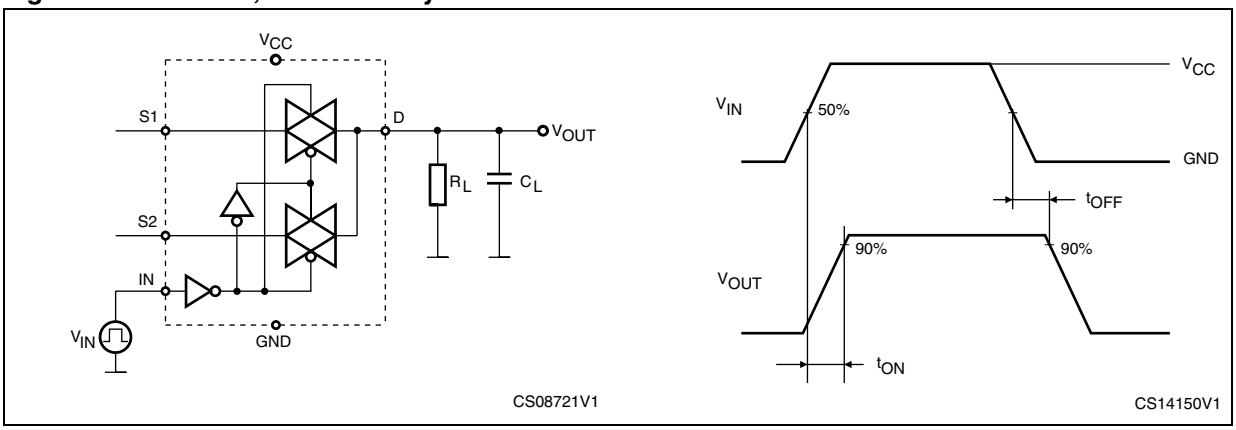


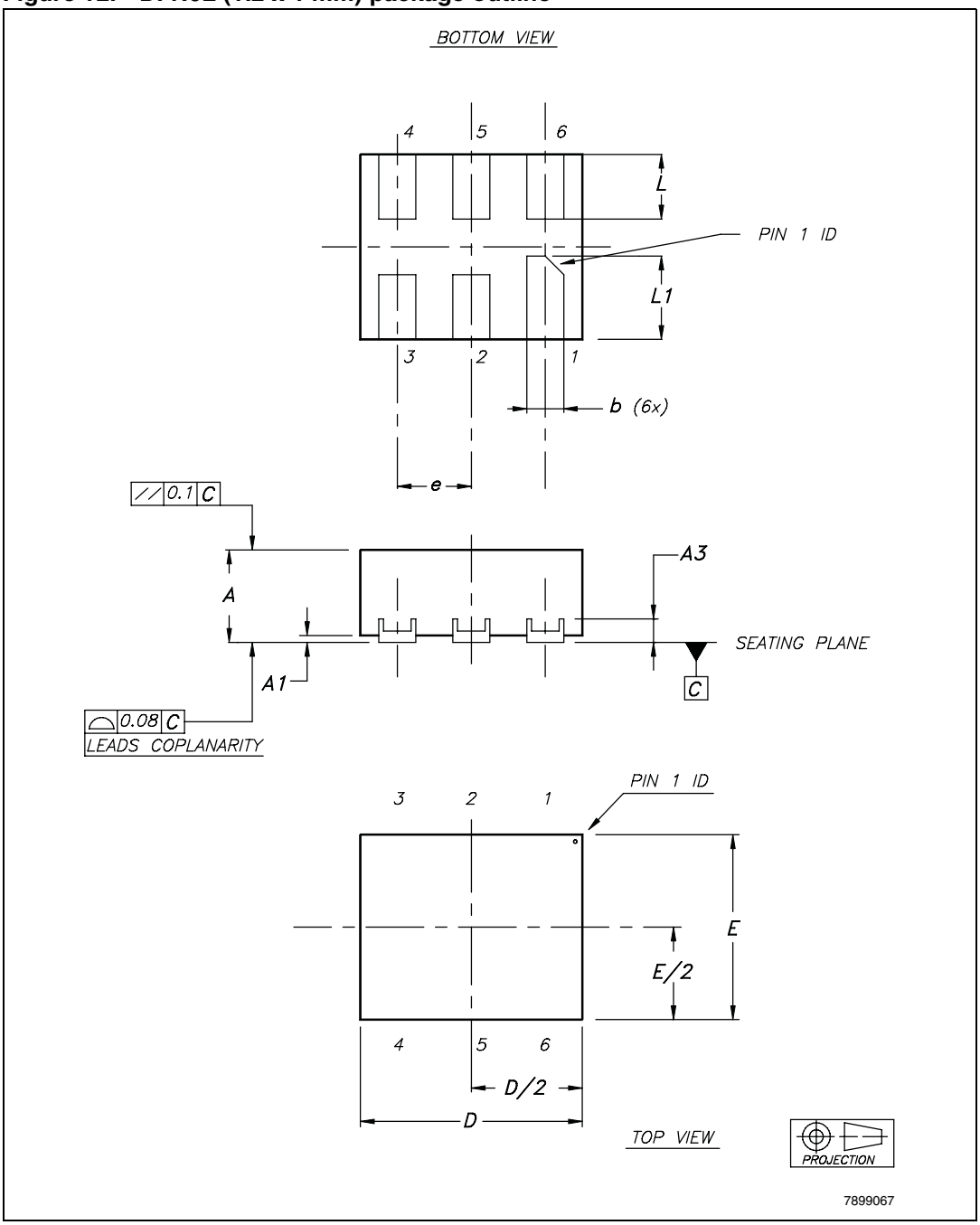
Figure 11. Turn-on, turn-off delay time



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 12. DFN6L (1.2 x 1 mm) package outline



1. Drawing is not to scale.

Table 9. DFN6L (1.2 x 1 mm) mechanical data

Symbol	Dimensions (millimeters)		
	Typ.	Min.	Max.
A	0.50	0.45	0.55
A1	0.02	0	0.05
A3	0.127		
b	0.20	0.15	0.25
D	1.20	1.15	1.25
E	1	0.95	1.05
e	0.40		
L	0.35	0.30	0.40
L1	0.45	0.40	0.50

Figure 13. DFN6L (1.2 x 1 mm) footprint recommendation

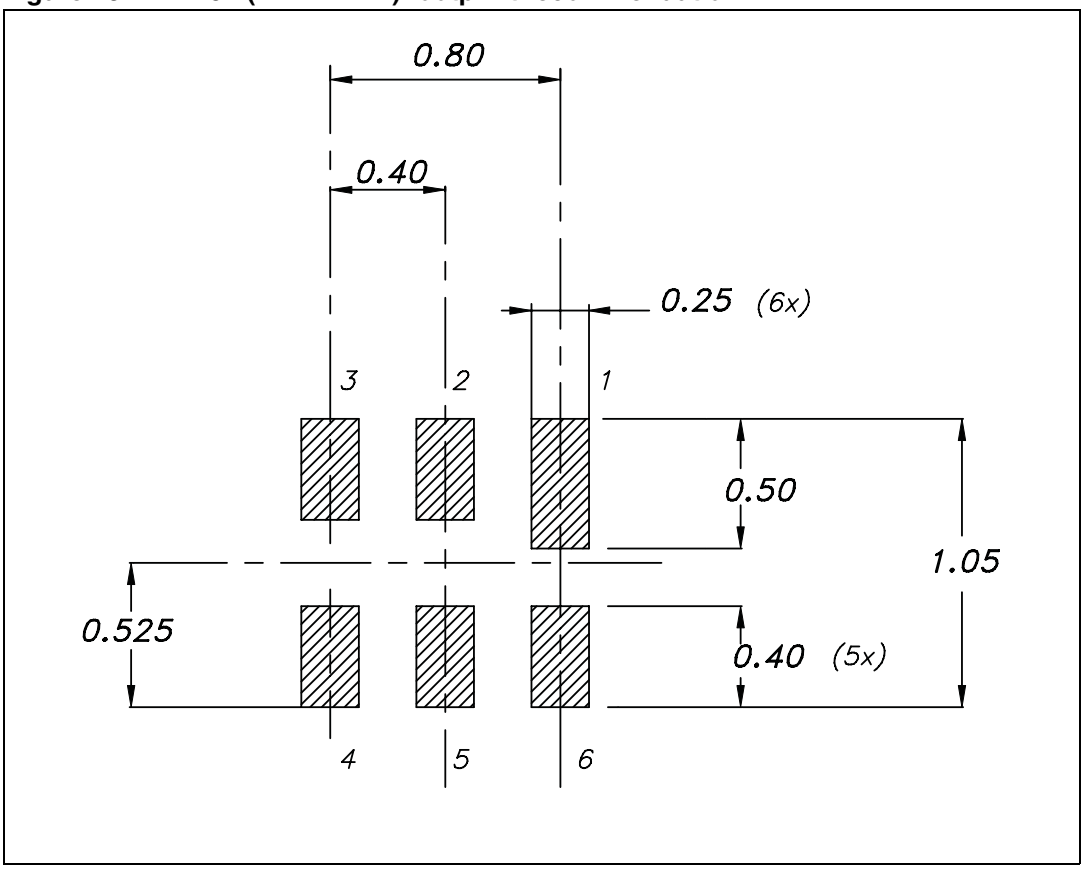
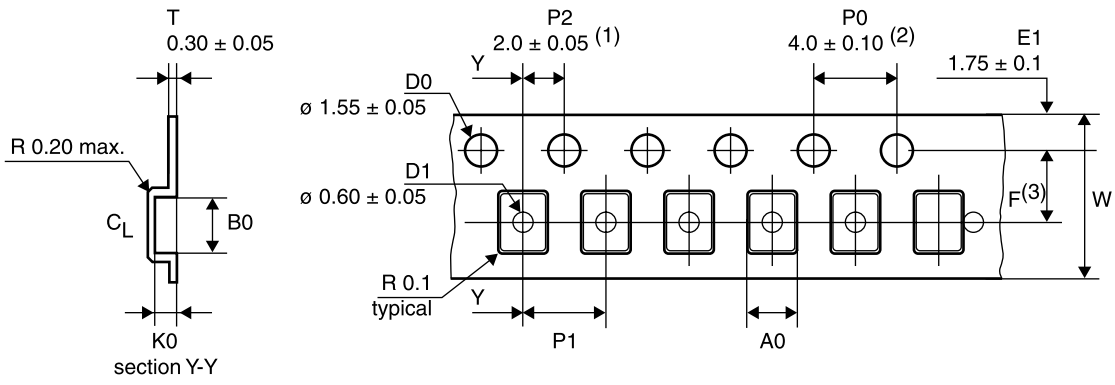


Figure 14. DFN6L carrier tape information

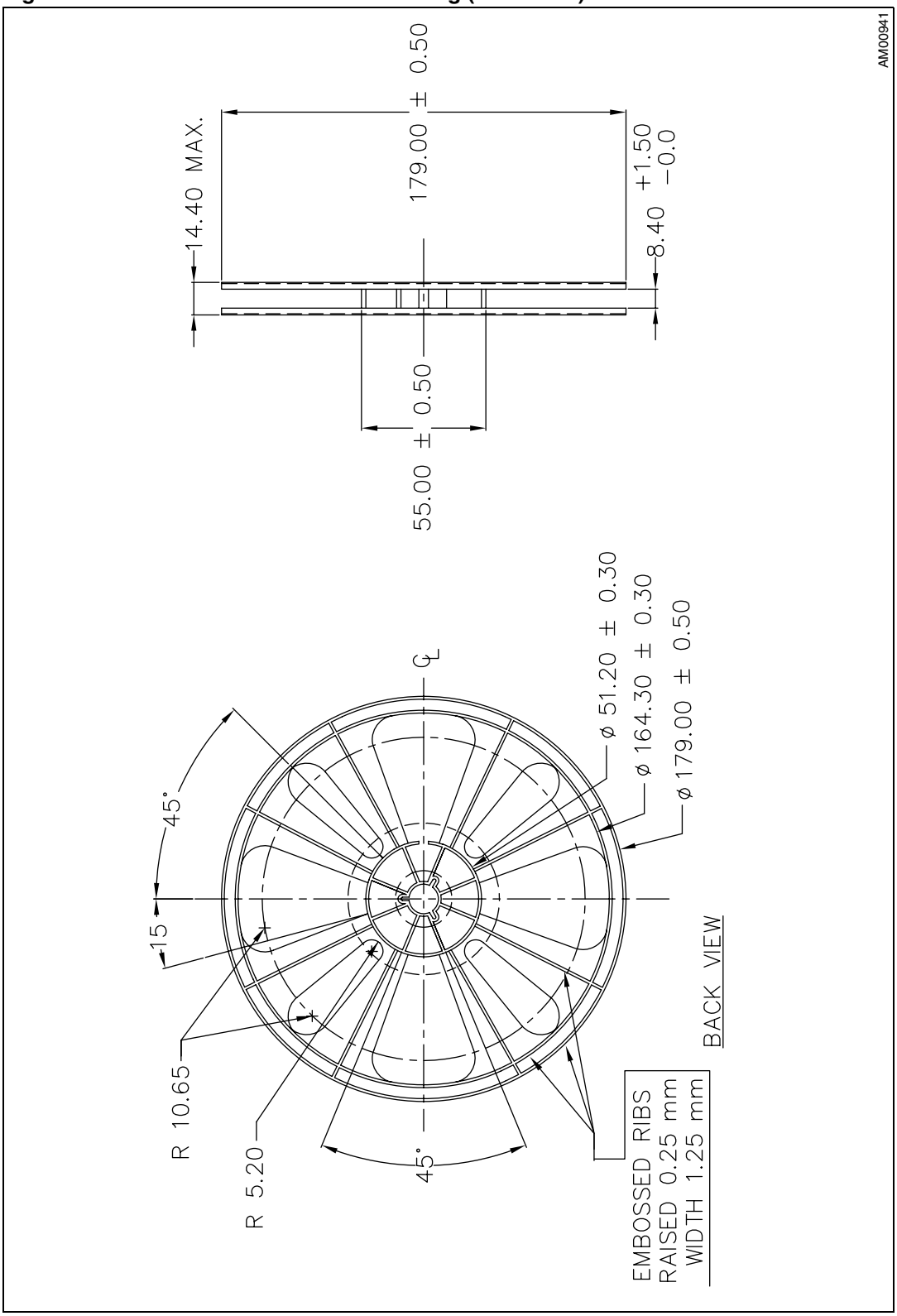


A0	1.17 ± 0.05
B0	1.40 ± 0.05
K0	0.65 ± 0.05
F	3.50 ± 0.05
P1	4.00 ± 0.1
W	8.00 ± 0.3

AM07379

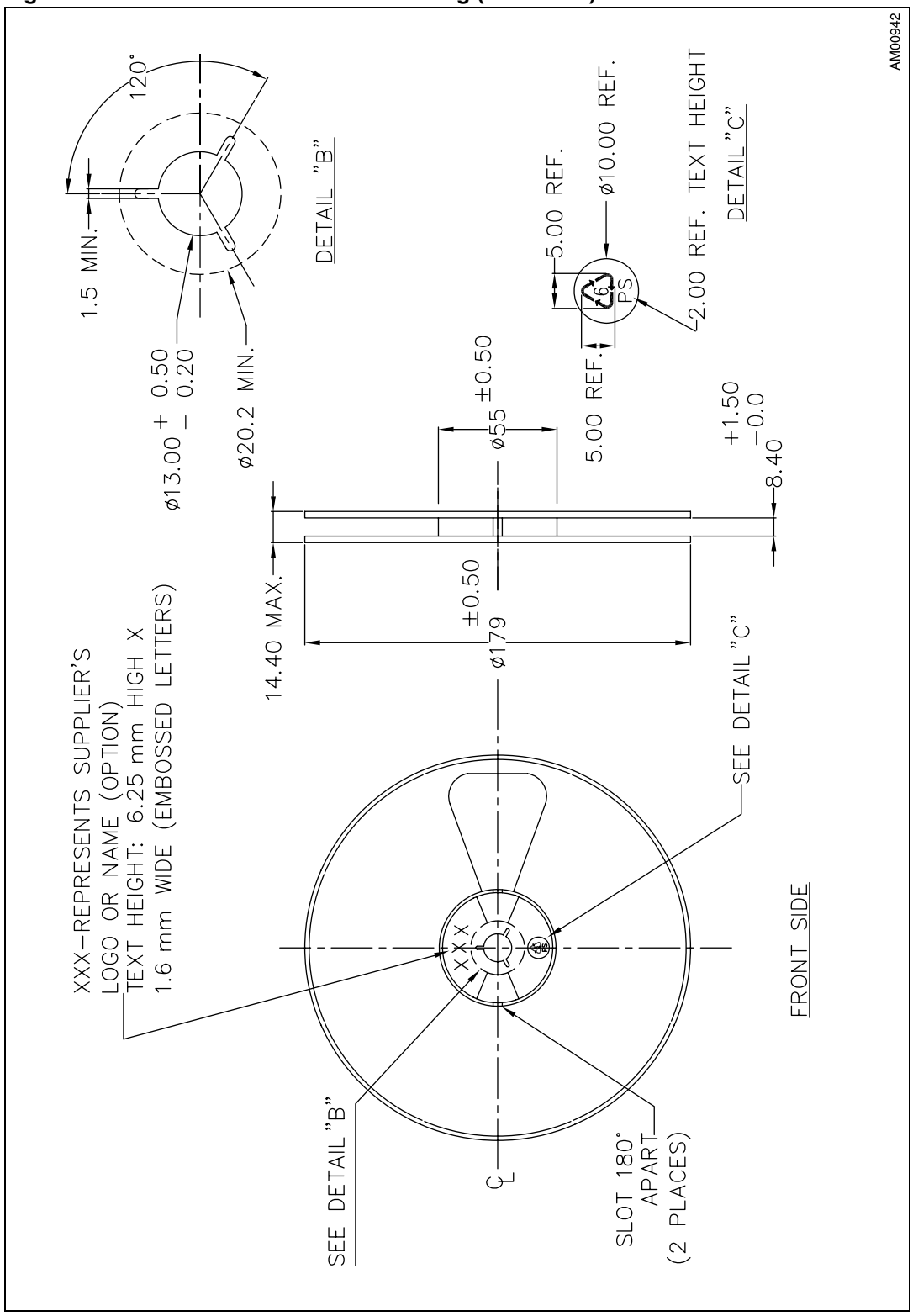
1. Measured from centreline of sprocket hole to centreline of pocket.
2. Cumulative tolerance of 10 sprocket holes is ± 0.20.
3. Measured from centreline of sprocket hole to centreline of pocket.
4. Other material available.
5. Drawing is not to scale.
6. All dimensions are in millimeters unless otherwise stated.

Figure 15. DFN6L reel information drawing (back view)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Figure 16. DFN6L reel information drawing (front view)



1. Drawing not to scale.
2. Dimensions are in millimeters.

6 Die description

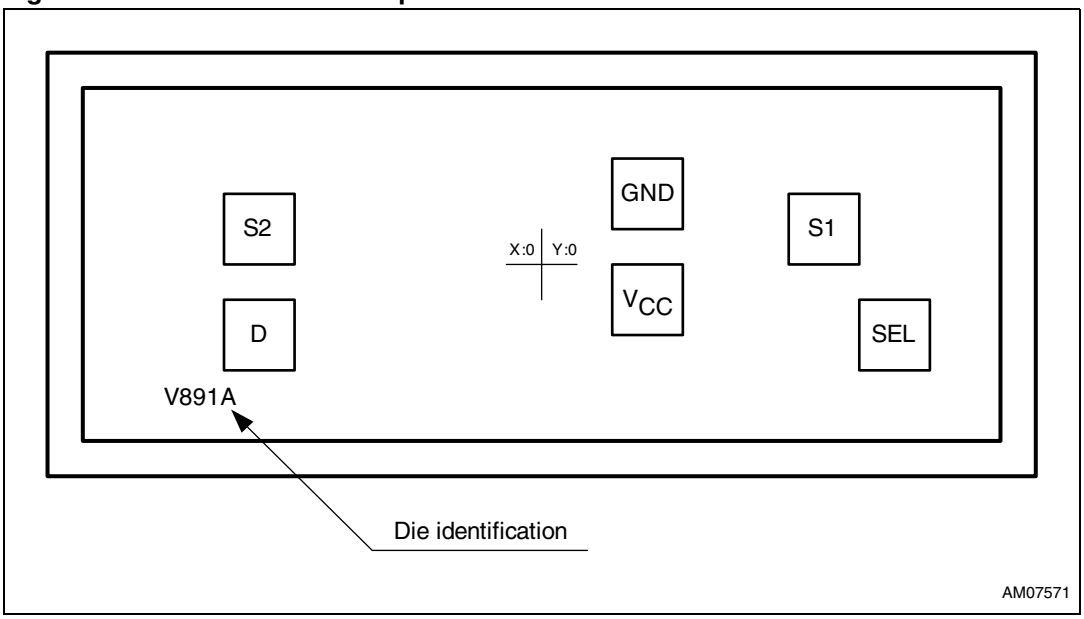
Product JSTG5123-CD1

- Wafer size: 203 mm (8 inches)
- Wafer thickness: 725 µm + 25 µm
- Die identification: V891A.

Die layout

- Design die size (X x Y): 900 x 350 µm
- Scribe line: 100 x 62 µm
- Stepping die size: 1000 x 412 µm
- Pad opening: 76 x 76 µm
- DI: die identification (at the position shown in *Figure 17*)
- Pads: pad contact (at the position shown in *Figure 17* and *Table 10*).

Figure 17. JSTG5123-CD1 die plot



Refer to *Table 10* for the pad locations.

Table 10. Pad information

Pad function	X (µm)	Y(µm)
S2	-292.25	52
GND	96.75	86
S1	292.25	52
SEL	361	-52
V_{CC}	96.75	-18
D	-292.25	-52

Pad locations are measured relative to the die center (where X and Y are the horizontal and vertical axis, respectively, measured in µm). Refer to *Figure 17*.

7 Revision history

Table 11. Document revision history

Date	Revision	Changes
30-Oct-2007	1	Initial release.
21-Apr-2010	2	*Table 6: DC specifications on page 7*: Modified values for “Input leakage current” and “Quiescent supply current”. Updated ECOPACK® statement in *Section 5: Package information*. Minor text changes throughout the document.
08-Feb-2011	3	Corrected typo in *Table 2*, *Section 2*, *Table 6* to *Table 9*, *Figure 12*, updated *Figure 14*.
21-Dec-2011	4	Added wafer, *Section 6: Die description*, updated *Table 1*, *Section 2: Electrical ratings* and Disclaimer, minor text corrections throughout document.
02-Apr-2012	5	Added product maturity information, updated *Table 1* and *Section 6* (replaced RPN JTS5123-CD1 by JSTG5123-CD1), minor text corrections throughout document.

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