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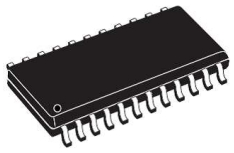
STGAP1S

gapDRIVE™: galvanically isolated single gate driver

Datasheet - production data



SO24W

Features

- Qualified for automotive applications according to AEC-Q100
- High voltage rail up to 1500 V
- Driver current capability: 5 A sink/source current at 25 °C
- dV/dt transient immunity ± 50 V/ns in full temperature range
- Overall input/output propagation delay: 100 ns
- Separate sink and source for easy gate driving configuration
- Negative gate drive ability
- Active Miller clamp
- Desaturation detection
- SENSE input
- V_{CE} active clamping
- Output 2-level turn-off
- Diagnostic status output
- UVLO and OVLO functions
- Programmable input deglitch filter
- Asynchronous stop command
- Programmable deadtime, with violation error
- SPI interface for parameters programming
- Temperature warning and shutdown protection
- Self-diagnostic routines for protection features
- Full effective fault protection

Applications

- 600/1200 V inverters
- Inverters for EV\HEV
- EV charging stations
- Industrial drives
- UPS equipment
- DC/DC converters
- Solar inverters

Description

The STGAP1S gapDRIVE™ is a galvanically isolated single gate driver for N-channel MOSFETs and IGBTs with advanced protection, configuration and diagnostic features. The architecture of the STGAP1S isolates the channel from the control and the low voltage interface circuitry through true galvanic isolation.
The gate driver is characterized by 5 A capability, making the device also suitable for high power inverter applications such as motor drivers in hybrid and electric vehicles and in industrial drives. The output driver section provides a rail-to-rail output with the possibility to use a negative gate driver supply.
The input to output propagation delay results contained within 100 ns, providing high PWM control accuracy.
Protection functions such as the Miller clamp, desaturation detection, dedicated sense pin for overcurrent detection, output 2-level turn-off, VCE overvoltage protection, UVLO and OVLO are included to easily design high reliability systems. Open drain diagnostic outputs are present and detailed device conditions can be monitored through the SPI. Each function's parameter can be programmed via the SPI, making the device very flexible and allowing it to fit in a wide range of applications. Separate sink and source outputs provide high flexibility and bill of material reduction for external components.

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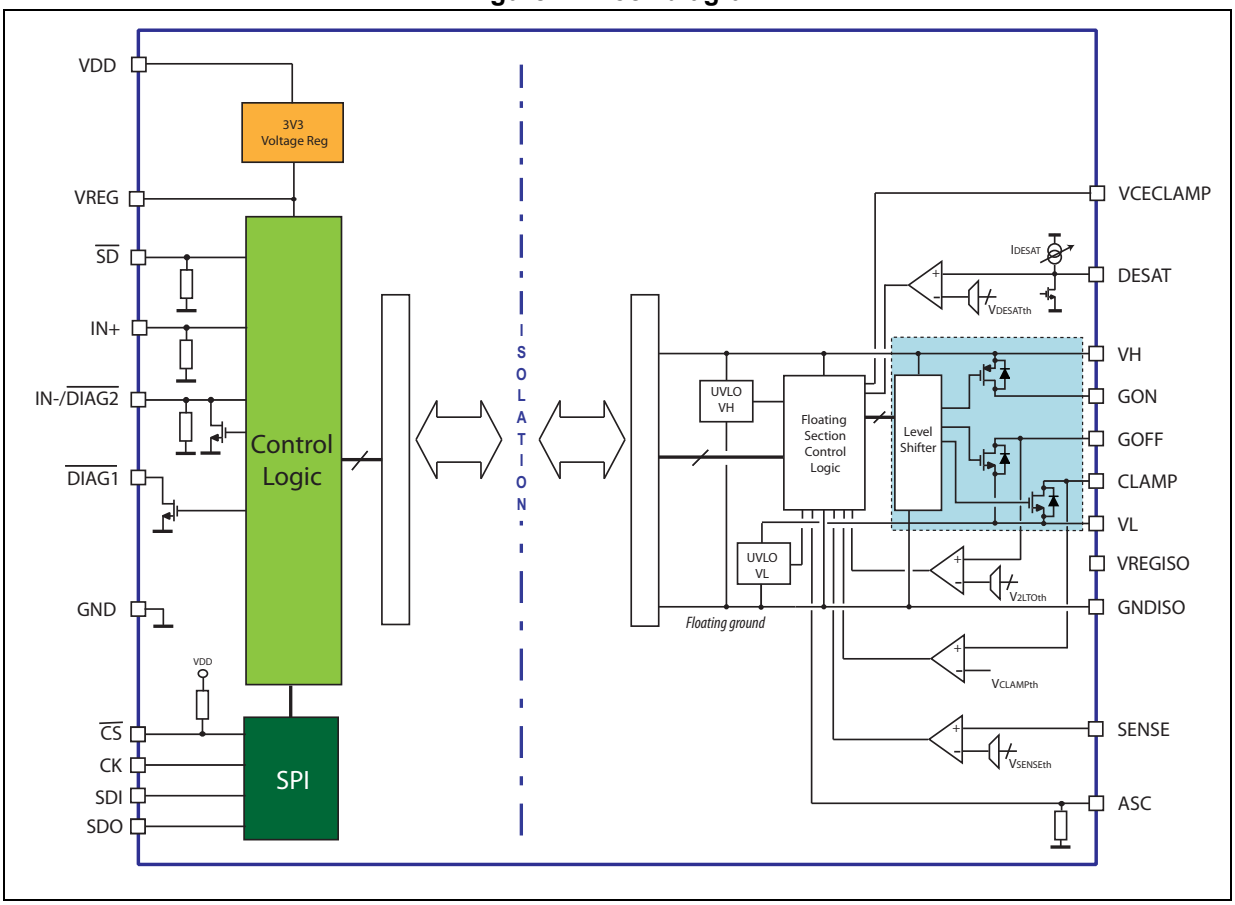
1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top view)

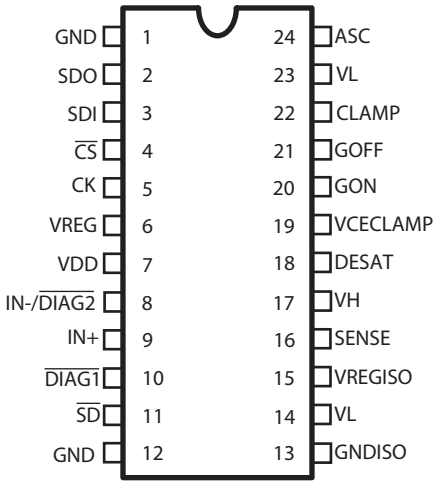


Table 1. Pin description

Pin no.	Pin name	Type	Function
7	VDD	Power supply	Internal 3.3 V regulator input supply pin
6	VREG	Power supply	Internal 3.3 V regulator output and supply pin
11	$\overline{SD}$	Logic input	Shutdown input (active low)
9	IN+	Logic input	Gate command input
8	IN-/DIAG2	Logic input/open drain output	Gate command input /open drain diagnostic output
10	DIAG1	Open drain output	Open drain diagnostic output
1, 12	GND	Ground	Low voltage section ground
4	$\overline{CS}$	Logic input	SPI chip select (active low)
5	CK	Logic input	SPI clock
3	SDI	Logic input	SPI serial data input
2	SDO	Logic output	SPI serial data output
19	VCECLAMP	Analog input	V_{CE} active clamping protection
18	DESAT	Analog input	Desaturation protection
15	VREGISO	Power supply	Internal regulator output pin for decoupling
17	VH	Power supply	Positive voltage supply
20	GON	Analog output	Gate source output
21	GOFF	Analog output	Gate sink output
22	CLAMP	Analog output	Miller clamp

Table 1. Pin description (continued)

Pin no.	Pin name	Type	Function
14, 23	VL	Power supply	Negative supply voltage or ground
13	GNDISO	Ground	High voltage section (isolated) ground
16	SENSE	Analog input	Sense input for overcurrent protection
24	ASC	Analog input	Asynchronous stop command

3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Min.	Max.	Unit
dV_{ISO}/dt	Common mode transient immunity	V_{CM} = 1500 V		50	V/ns
VDD	Integrated 3.3 V voltage regulator input voltage vs. GND		-0.30	6.50	V
VREG	Integrated 3.3 V voltage regulator output voltage vs. GND		-0.30	3.60	V
VREG_ISO	Isolated logic supply voltage vs. GNDISO		-0.30	3.60	V
V_{LOGIC}	Logic pins voltage vs. GND		-0.30	VDD + 0.30	V
VHL	Differential supply voltage (VH vs. VL)		-0.30	40	V
VH	Positive supply voltage (VH vs. GNDISO)		-0.30	40	V
VL	Negative supply voltage (VL vs. GNDISO)		-15	0.30	V
V_{OUT}	Voltage on gate driver outputs (GON, GOFF, CLAMP vs. VL)		VL - 0.30	VH + 0.30	V
V_{DESAT}	Voltage on DESAT pin vs. GNDISO		-0.30	VH + 0.30	V
V_{SENSE}	Voltage on SENSE pin vs. GNDISO		-2	$(VH + 0.30, 20)_{min}$	V
$V_{CECLAMP}$	Voltage on VCECLAMP pin vs. VL		VL - 0.30	VH + 0.30	V
V_{ASC}	Voltage on ASC pin vs. GNDISO		-0.30	VH + 0.30	V
I_{DIAGx}	Open drain DC output current	V_{DIAGx} < 0.8 V		20	mA
V_{DIAGx}	Open drain output voltage		-0.30	6.50	V
T_J	Junction temperature		-40	150	°C
T_S	Storage temperature		-50	150	°C
T_A	Ambient temperature		-40	125	°C
P_{Din}	Power dissipation input chip	f_{sw} = 1 MHz		65	mW
P_{Dout}	Power dissipation output chip			$(T_{J,max} - T_A)/R_{th(JA)} - P_{Din}$	W
dH/dt	Magnetic field immunity			100	A/(m·s)
ESD	Human body model		2		kV

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient(1)	65	°C/W

1. The STGAP1S mounted on the EVALSTGAP1S rev 2.0 board (two-layer FR4 PCB).

3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Max.	Unit
VH	17	Positive supply voltage (VH vs. GNDISO)		4.50(1)	36	V
VL	14, 23	Negative supply voltage (VL vs. GNDISO)		GNDISO - 10	GNDISO(2)	V
VHL		Differential supply voltage (VH vs. VL)			36	V
VDD	7	Integrated 3.3 V voltage regulator input voltage vs. GND		4.50	5.50	V
VREG	6	Internal logic supply voltage vs. GND	(3)	3	3.60	V
V_{LOGIC}	2, 3, 4, 5, 8, 9, 11	Logic pins voltage vs. GND			$(VDD, 5)_{min}$	V
ASC	24	ASC pin voltage		GNDISO	$(VH, 15)_{min}$	V
$V_{DESATth}$	18	Desaturation protection threshold	DESAT enabled		VH - 1.50	V
f_{SW}		Maximum switching frequency(4)			1	MHz

1. When UVLO is enabled this value is $VH_{on,max}$.
2. When UVLO is enabled this value is $VL_{on,min}$.
3. When VDD is connected to the VREG pin (refer to *Section 6 on page 22*).
4. Actual limit depends on power dissipation constraints.

4 Electrical characteristics

4.1 AC operation

Table 5. AC operation electrical characteristics
(T_j = -40 to 125 °C, VDD = 5 V; VH = 15 V, VL = GNDISO)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{deglitch}$	8, 9, 11	Input deglitch time	INfilter = '11'	50	70	90	ns
			INfilter = '01'	140	210	280	ns
			INfilter = '10'	490	560	630	ns
t_{INmin}		Minimum propagated input pulse	INfilter = '00' and (2LTO_EN = '0' or 2LTOtime = 0x0)			20	ns
t_{Don}	8, 9, 11, 20	Input to output propagation delay ON	Deglitch filter and 2LTO disabled	90	100	130	ns
t_{Doff}	8, 9, 11, 21	Input to output propagation delay OFF	Deglitch filter and 2LTO disabled	90	100	130	ns
t_r	20	GON rise time	VL = 0 V; C_L = 2 nF, 10% ÷ 90%			25	ns
t_f	21	GOFF rise time	VL = 0V C_L = 2 nF, 90% ÷ 10%			25	ns
PWD	8, 9, 11, 20, 21	Pulse width distortion $\lvert t_{Don} - t_{Doff} \rvert$	t_{IN} > 100 ns Deglitch filter and 2LTO disabled		4	10	ns
DT	8, 9, 20, 21	Deadtime	DTset = '01'	205	250	295	ns
			DTset = '10'	650	800	945	
			DTset = '11'	985	1200	1415	
$t_{release}$	11	Minimum flag release time	SD = '0', SD_FLAG = '1'			105	µs

4.2 DC operation

Table 6. DC operation electrical characteristics
(T_j = -40 to 125 °C, VDD = 5 V; VH = 15 V, VL = GNDISO)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Logic inputs/output							
V_{ol}	2	SDO logic “0” output voltage	I = 4 mA			0.15	V
V_{oh}		SDO logic “1” output voltage	I = 4 mA	4.85			V
I_{INh}	8, 9	INx logic “1” input bias current	V_{IN} = 5 V (pin 8 used as IN-)	55	85	145	µA
I_{INl}		INx logic “0” input bias current	V_{IN} = 0 V (pin 8 used as IN-)			0.10	µA
I_{SDh}	11	SD logic “1” input bias current	V_{SD} = 5 V	55	85	145	µA
I_{SDl}		SD logic “0” input bias current	V_{SD} = 0 V			0.10	µA
R_{in_pd}	8, 9, 11	Input pull-down resistors	V_{IN} = 5 V (pin 8 used as IN-)	35	60	85	kΩ
R_{in_pu}	4	CS input pull-up resistor	CS = GND	35	55	80	kΩ
V_{il}	3, 4, 5, 8, 9, 11	Low logic level voltage		0.29 · VDD	0.33 · VDD	0.37 · VDD	V
V_{ih}		High logic level voltage		0.62 · VDD	0.66 · VDD	0.79 · VDD	V
Driver buffer section							
I_{GON}	20	Source short-circuit current	$V_{IN} < V_{ih}$, Tpulse < 5 µs, DC = 1% T_j = 25 °C T_j = -40 ÷ +125 °C	 2.50	5	 7	A
I_{GOFF}	21	Sink short-circuit current	$V_{IN} < V_{ih}$, Tpulse < 5 µs, DC = 1% T_j = 25 °C T_j = -40 ÷ +125 °C	 2.50	5	 6	A
V_{GOFFL}	21	GOFF output low level voltage	I_{GOFF} = 0.1 A I_{GOFF} = 1 A	VL + 0.03 VL + 0.50	VL + 0.09 VL + 1	VL + 0.15 VL + 1.80	V
V_{GONH}	20	GON output high level voltage	I_{GON} = 0.1 A I_{GON} = 1 A	VH - 0.18 VH - 2.10	VH - 0.10 VH - 1.30	VH - 0.05 VH - 0.50	V
SafeClp	20, 21, 22	GOFF active clamp	I_{GOFF} = 0.2 A; VH floating; GON = GOFF = CLAMP			3	V

Table 6. DC operation electrical characteristics
(T_j = -40 to 125 °C, VDD = 5 V; VH = 15 V, VL = GNDISO) (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage							
I_{REG}	6	VREG short-circuit current (see *Section 7.3 on page 29*)	0.1 V < VREG < 3.0 V		60	120	mA
			VREG < 0.1 V		15	35	
VDD_{on}	7	VDD UVLO turn-on threshold		3.95	4.10	4.30	V
VDD_{off}		VDD UVLO turn-off threshold		3.65	3.80	4	V
VDD_{hys}		VDD UVLO hysteresis		0.15			V
$OVVDD_{on}$		VDD OVLO turn-on threshold		5.30	5.50	5.90	V
$OVVDD_{off}$		VDD OVLO turn-off threshold		5.40	5.70	6.10	V
OV_{VDDhys}		VDD OVLO hysteresis		100	200	300	mV
I_{QDD}	7	VDD quiescent supply current	VDD = 5 V; SD = 5 V; INx = GND; f = 0 Hz	5.20	6.50	7.50	mA
			VDD = 5 V; SD = 5 V; $f_{SW} = f_{SW,max}$	7.50	8.50	9.50	mA
VH_{on}	17	VH UVLO turn-on threshold	VHONth = '01'	9.40	10	10.50	V
			VHONth = '10'	11.30	12	12.60	
			VHONth = '11'	13.15	14	14.70	
VH_{off}		VH UVLO turn-off threshold	VHONth = '01'	8.50	9	9.45	V
			VHONth = '10'	10.35	11	11.55	
			VHONth = '11'	12.25	13	13.65	
VH_{hyst}		VH UVLO hysteresis		0.70	1	1.30	V
VL_{on}	14, 23	VL UVLO turn-on threshold	VLONth = '01'	-3.15	-3	-2.80	V
			VLONth = '10'	-5.25	-5	-4.70	
			VLONth = '11'	-7.35	-7	-6.55	
VL_{off}		VL UVLO turn-off threshold	VLONth = '01'	-2.15	-2	-1.90	V
			VLONth = '10'	-4.25	-4	-3.80	
			VLONth = '11'	-6.35	-6	-5.70	
VL_{hys}		VL UVLO hysteresis		0.70	1	1.20	V

Table 6. DC operation electrical characteristics (T_j = -40 to 125 °C, VDD = 5 V; VH = 15 V, VL = GNDISO) (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
OV_{VHoff}	17	VH OVLO turn-off threshold	OVLO_EN = '1'	17.80	19	20	V
OV_{VHon}		VH OVLO turn-on threshold	OVLO_EN = '1'	16.90	18	18.90	V
OV_{VHhys}		VH OVLO hysteresis	OVLO_EN = '1'	0.60	1	1.30	V
OV_{VLoff}	14, 23	VL OVLO turn-off threshold	OVLO_EN = '1'	-10.50	-10	-9.40	V
OV_{VLon}		VL OVLO turn-on threshold	OVLO_EN = '1'	-9.45	-9	-8.55	V
OV_{VLhyst}		VL OVLO hysteresis	OVLO_EN = '1'	0.70	1	1.30	V
I_{QH}	17	VH quiescent supply current	SD = 5 V; IN+ = 5 V; IN- = GND	5	6.70	7.50	mA
			SD = 5 V; $f_{SW} = f_{SW,max}$; No load	10	14	19	mA
I_{QL}	14, 23	VL quiescent supply current	VL = -5 V; SD = 5 V; IN+ = IN- = GND	300	420	550	µA
Desaturation protection							
$V_{DESATth}$	18	Desaturation threshold	DESATth = '000';	2.60	3	3.10	V
			DESATth = '001'	3.60	4	4.20	
			DESATth = '010'	4.60	5	5.30	
			DESATth = '011'	5.50	6	6.30	
			DESATth = '100'	6.50	7	7.40	
			DESATth = '101'	7.40	8	8.40	
			DESATth = '110'	8.30	9	9.40	
			DESATth = '111'	9.30	10	10.50	
$t_{DESfilter}$		DESAT pin deglitch filter	DESATth = '100'(1)	10	20	30	ns
I_{DESAT}		DESAT blanking charge current	DESATcur = '00'; V_{DESAT} = 0 V	220	250	265	µA
			DESATcur = '01'; V_{DESAT} = 0 V	440	500	525	
			DESATcur = '10'; V_{DESAT} = 0 V	660	750	800	
			DESATcur = '11'; V_{DESAT} = 0 V	885	1000	1050	
I_{DESoff}		DESAT blanking discharge current	V_{DESAT} = 8 V	50	70	90	mA

Table 6. DC operation electrical characteristics
(T_j = -40 to 125 °C, VDD = 5 V; VH = 15 V, VL = GNDISO) (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{BLK}	18	DESAT protection fixed blanking time		160	250	340	ns
t_{DESAT}		DESAT protection intervention time	V_{DESAT} = V_{DESAth} to GOFF 90% C_{LOAD} = 10 nF 2LTO disabled	80	150	220	ns
SENSE overcurrent function							
$V_{SENSEth}$	16	SENSE protection threshold	SENSEth = '000'	88	100	112	mV
			SENSEth = '001'	110	125	140	
			SENSEth = '010'	135	150	165	
			SENSEth = '011'	158	175	192	
			SENSEth = '100'	185	200	215	
			SENSEth = '101'	235	250	268	
			SENSEth = '110'	285	300	315	
			SENSEth = '111'	380	400	420	
t_{SENSE}		SENSE protection intervention time	SENSEth = '111' 0 →1 V step on V_{SENSE} to GOFF 90%; C_{LOAD} = 10 nF 2LTO disabled		95	120	ns
2-level turn-off function							
V_{2LTOth}	21	2LTO threshold	2LTOth = '0000'	6.65	7.00	7.35	V
			2LTOth = '0001'	7.12	7.50	7.88	
			2LTOth = '0010'	7.60	8.00	8.40	
			2LTOth = '0011'	8.07	8.50	8.93	
			2LTOth = '0100'	8.55	9.00	9.45	
			2LTOth = '0101'	9.02	9.50	9.98	
			2LTOth = '0110'	9.50	10.00	10.50	
			2LTOth = '0111'	9.97	10.50	11.03	
			2LTOth = '1000'	10.45	11.00	11.55	
			2LTOth = '1001'	10.92	11.50	12.08	
			2LTOth = '1010'	11.40	12.00	12.60	
			2LTOth = '1011'	11.87	12.50	13.13	
			2LTOth = '1100'	12.35	13.00	13.65	
			2LTOth = '1101'	12.82	13.50	14.18	
			2LTOth = '1110'	13.30	14.00	14.70	
			2LTOth = '1111'	13.77	14.50	15.23	

Table 6. DC operation electrical characteristics (T_j = -40 to 125 °C, VDD = 5 V; VH = 15 V, VL = GNDISO) (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{2LTOtime}$	21	2LTO time	2LTOtime = '0001'	0.64	0.75	0.89	µs
			2LTOtime = '0010'	0.89	1.00	1.15	
			2LTOtime = '0011'	1.36	1.50	1.65	
			2LTOtime = '0100'	1.83	2.00	2.18	
			2LTOtime = '0101'	2.30	2.50	2.70	
			2LTOtime = '0110'	2.77	3.00	3.23	
			2LTOtime = '0111'	3.25	3.50	3.75	
			2LTOtime = '1000'	3.47	3.75	4.03	
			2LTOtime = '1001'	3.71	4.00	4.29	
			2LTOtime = '1010'	3.94	4.25	4.56	
			2LTOtime = '1011'	4.18	4.50	4.82	
			2LTOtime = '1100'	4.42	4.75	5.08	
			2LTOtime = '1101'	4.66	5.00	5.34	
			2LTOtime = '1110'	4.90	5.25	5.63	
			2LTOtime = '1111'	5.12	5.50	5.95	
Diagnostic outputs							
$t_{DIAG1,2}$	8, 10	Fault event to DIAGx Low delay	Fault event to DIAGx 90%		5		µs
I_{DIAG1}		DIAG1 low level sink current	V_{DIAG1} = 0.4 V	10	18	30	mA
I_{DIAG2}		DIAG2 low level sink current	V_{DIAG2} = 0.4 V	10	18	30	mA
$R_{DIAG1,2}$		DIAGx pull-down resistor		300	550	800	kΩ
Clamp Miller function							
$V_{CLAMPth}$	22	CLAMP voltage threshold	CLAMP vs. GNDISO	1.70	2	2.30	V
I_{CLAMP}		Clamp short-circuit current	$V_{IN} < V_{ih}$, Tpulse < 5 µs, DC = 1% T_j = 25 °C T_j = -40 ÷ +125 °C	2.50	5	6	A
V_{CLAMP_L}		Clamp low level output voltage	I_{CLAMP} = 1 A	VL + 0.50	VL + 1	VL + 1.80	V
V_{CE} active clamping protection							
$V_{VCECLth}$	19	V_{CE} clamping threshold		VL + 1.20	VL + 1.60	VL + 2	V
$V_{VCECLhyst}$		V_{CE} clamping threshold hysteresis		0.30	0.50	0.60	V

Table 6. DC operation electrical characteristics (T_j = -40 to 125 °C, VDD = 5 V; VH = 15 V, VL = GNDISO) (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{VCECLoff}$	19	V_{CE} clamping time-out		2	2.30	2.60	µs
t_{VCECL}		V_{CE} clamping intervention time(1)			20		ns
ASC function							
V_{ASCl}	24	Low logic level voltage		0.80	1.10	1.40	V
V_{ASCh}		High logic level voltage		1.80	2.20	2.40	V
I_{ASCh}		ASC logic “1” input bias current	V_{ASC} = 5 V	55	100	145	µA
I_{ASCl}		ASC logic “0” input bias current	V_{ASC} = 0 V			0.10	µA
R_{ASC}		ASC pull-down resistors	V_{ASC} = 5 V	35	50	70	kΩ
t_{ASC}		ASC intervention time	V_{ASC} = 5 V	100		250	ns
Functionality checks							
t_{Gchk}	20, 21	Gate path check time (GON/GOFF)(2)				30	µs
V_{Gchk}	20	Gate path check voltage (GON)		0.7 x VH	0.76 x VH	0.84 x VH	V
t_{Rchk}	16	SENSE resistor check time				15	µs
$I_{GOFFchk}$	21	GOFF path check current		-420	-350	-280	µA
$I_{SENSERchk}$	16	SENSE resistor check current	V_{SENSE} < 1 V	8	10	12	µA
$t_{SENSEchk}$		SENSE comparator check time				15	µs
$t_{DESATchk}$	18	DESAT comparator check time				15	µs
Overtemperature protection							
T_{WN}		Warning temperature(1)		125			°C
T_{SD}		Shutdown temperature(1)		155			°C
T_{hys}		Temperature hysteresis(1)			20		°C
Standby							
I_{STBY_VDD}	7	VDD standby current	VDD = 5 V	0.40	0.80	1	mA
t_{sleep}		Standby time	SD = '0', measured from CS rise	500	700	900	ns
t_{awake}		Logic wake-up time(1)	SD = '1'	5			µs

Table 6. DC operation electrical characteristics (T_j = -40 to 125 °C, VDD = 5 V; VH = 15 V, VL = GNDISO) (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
SPI(1)							
t_{CKmax}	5	Maximum SPI clock frequency		5			MHz
t_{rCK} t_{fCK}		SPI clock rise and fall time	CL = 30 pF			25	ns
t_{hCK} t_{lCK}		SPI clock high and low time		75			ns
t_{setCS}	4	CS setup time		350			ns
t_{holCS}		CS hold time		10			ns
t_{desCS}		CS deselect time(3)	Local register read	800			ns
			Remote register read	30			µs
			Start configuration	22			
			Stop configuration	5			
			Reset status register	50			
			Reset remote register	25			
			Any other command	700			ns
t_{setSDI}	3	SDI setup time		25			ns
t_{holSDI}		SDI hold time		20			ns
t_{enSDO}	2	SDO enable time				38	ns
t_{disSDO}		SDO disable time				47	ns
t_{vSDO}		SDO valid time				57	ns
t_{holSDO}		SDO hold time		37			ns
t_{SDLCSL}	4,11	SD falling to CS falling		350			ns
t_{CSHSDH}	4,11	CS rising to SD rising		350			ns

1. Characterization data, not tested in production.
2. The actual waiting time depends on the gate charge size.
3. See *Table 22 on page 50* and *Section 9.1.3 on page 48*.

5 Isolation

Table 7. Isolation and safety-related specifications

Parameter	Symbol	Value	Unit	Conditions
Clearance (minimum external air gap)	CLR	8	mm	Measured from input terminals to output terminals, shortest distance through air
Creepage (minimum external tracking)	CPG	8	mm	Measured from input terminals to output terminals, shortest distance path along body
Comparative tracking index (tracking resistance)	CTI	≥ 400		DIN IEC 112/VDE 0303 Part 1
Isolation group		II		Material group (DIN VDE 0110, 1/89, Table 1)

Table 8. IEC 60747-5-2 isolation characteristics

Parameter	Symbol	Test conditions	Characteristic	Unit
Installation classification (EN 60664-1, Table 1 - see(1)) For rated mains voltage ≤ 150 V_{rms} For rated mains voltage ≤ 300 V_{rms} For rated mains voltage ≤ 600 V_{rms}			 I - IV I - III I - II	
Pollution degree (EN 60664-1)			2	
Maximum working isolation voltage	V_{IORM}		1500	V_{PEAK}
Input to output test voltage as per IEC 60747-5-2	V_{PR}	Method a, type test $V_{PR} = V_{IORM} \times 1.6$, t_m = 10 s Partial discharge < 5 pC	2400	V_{PEAK}
		Method b, 100 % production test $V_{PR} = V_{IORM} \times 1.875$, t_m = 1 s Partial discharge < 5 pC	2815	V_{PEAK}
Transient overvoltage as per IEC 60747-5-2 (highest allowable overvoltage)	V_{IOTM}	t_{ini} = 60 s type test	4000	V_{PEAK}
Maximum surge isolation voltage	V_{IOSM}	Type test	4000	V_{PEAK}
Isolation resistance	R_{IO}	V_{IO} = 500 V at T_S	$>10^9$	Ω

1. For three-phase systems the values in the table refer to the line-to-neutral voltage.

Table 9. Isolation voltage as per UL 1577

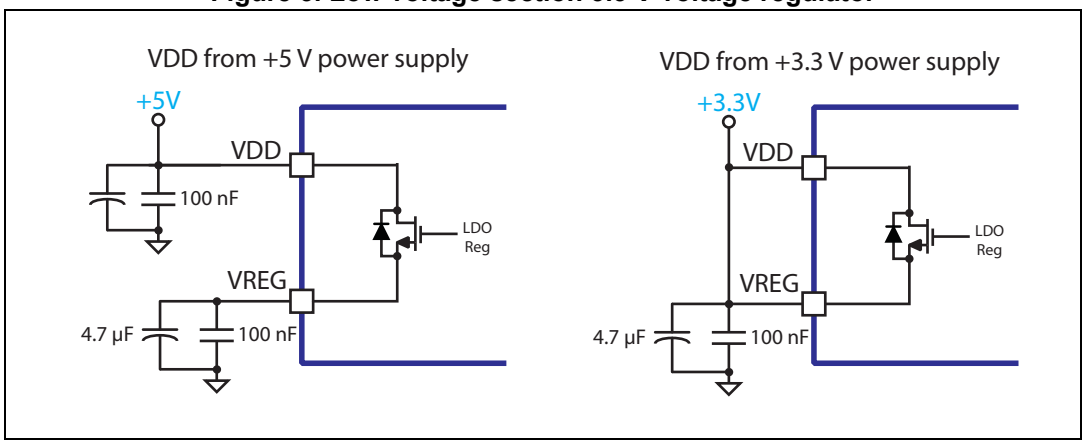
Description	Symbol	Characteristic	Unit
Isolation withstand voltage, 1 min. (type test)	V_{ISO}	2500\3536	V_{rms}\V_{PEAK}
Isolation withstand test, 1 sec. (100% production)	$V_{ISOtest}$	3000\4245	V_{rms}\V_{PEAK}

6 Logic supply management

6.1 Low voltage section voltage regulator

The device integrates in the low voltage section a linear voltage regulator that can be used to obtain the 3.3 V logic core supply voltage from an external 5 V supply voltage. If an external 3.3 V supply voltage is available the VDD and VREG have to be shorted as shown in *Figure 3*. The logic IOs are referred to the VDD voltage (see *Table 6 on page 14* for details).

Figure 3. Low voltage section 3.3 V voltage regulator



Undervoltage protection is available on the VDD supply pin (disabled by default).

When the VDD voltage goes below the VDD_{off} threshold the device and its outputs goes in “safe state” (see *Section 6.3*) and the UVLOD status flag is forced low. Once the protection is triggered, the UVLOD flag is latched and the device remains in “safe state” until the UVLOD flag is not released. See *Section 7.11 on page 35* for indication on how the failure flags can be released.

This protection can be enabled writing the UVLOD_EN bit of the CFG1 register (disabled by default).

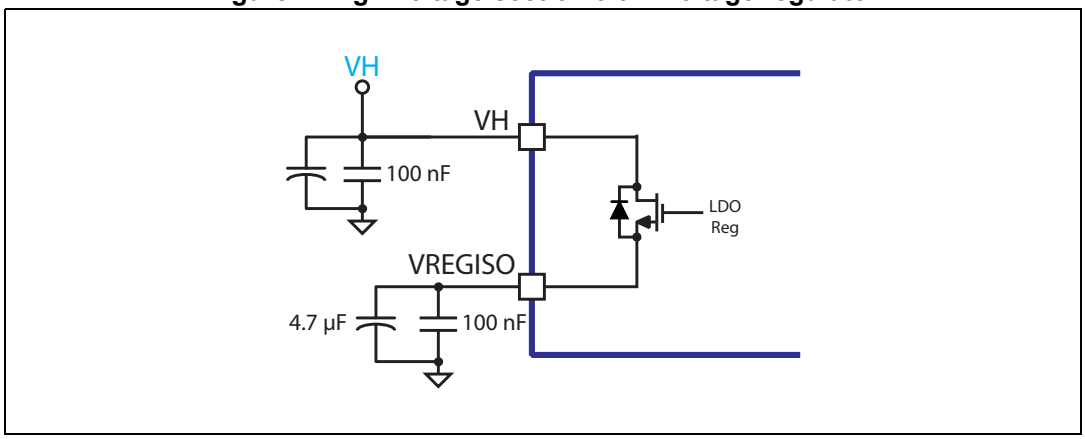
Overvoltage protection is available on the VDD supply pin.

When the VDD voltage goes over the OV_{VDDoff} threshold the device and its outputs goes in “safe state” and the OVLOD status flag is forced low. The device remains in “safe state” and the OVLOD flag is latched, see *Section 7.11* for indication on how the failure flags can be released.

6.2 High voltage section voltage regulator

The device integrates in the high voltage section a linear voltage regulator that generates the 3.3 V logic core supply voltage from an external supply voltage connected to the VH pin.

Figure 4. High voltage section 3.3 V voltage regulator



If the voltage at the VREGISO pin goes below the minimum operating threshold which causes the logic reset, the REG_ERR bit in the STATUS1 register is set high.

6.3 Power-up, power-down and “safe state”

The following conditions define the device's “safe state”:

- GOFF = ON state
- GON = high impedance
- CLAMP = ON state (if CLAMP < 'GNDISO + $V_{CLAMPth}$')
- DESAT = GNDISO (internal switch on and current generator off)

Such conditions are guaranteed at power-up of the isolated side (also for VH < VH_{on} and VL > VL_{on}) and during the whole device power-down phase (also for VH < VH_{off} and VL > VL_{off}), whatever the value of the input pins.

The device integrates a structure which clamps the driver output to a voltage smaller than SafeClp when the VH voltage is not high enough to actively turn the Goff N-channel MOSFET on.

If the VH positive supply pin is floating the GOFF pin is clamped to a voltage smaller than SafeClp.

After power-up of the isolated side the REGERRR status flag is latched and the device is forced in “safe state”. See *Section 7.11 on page 35* for indication on how the failure flags can be released.

After power-up of the low voltage side the REGERRL and UVLOD status flags are latched and the device is forced in “safe state”. See *Section 7.11* for indication on how the failure flags can be released.

The UVLOH flag is also forced high at the power-up of the low voltage side, but its value is set to zero as soon as the isolated side power-up is completed.

6.4 Standby function

The device can be put in standby mode to reduce the power consumption on VDD via the SPI command “Sleep” (refer to *Section 9.1.5 on page 49*).

The proper sequence is:

1. Pull-down the SD pin: the driver section will be put in “safe state”
2. Send a Sleep command
3. After a t_{sleep} time the device can be considered actually in the sleep mode.

To exit from the sleep mode it is necessary to set SD high for at least t_{awake} while keeping IN+ low.

After a t_{awake} time the device can accept new commands and the REGERRR bit is set to indicate that the device needs to be reprogrammed.

If the SD pin is raised while t_{sleep} is still not expired, the device returns to the operation mode within a t_{awake} time.

7 Functional description

7.1 Inputs and outputs

The device is controlled through following logic inputs:

- SD: active low shutdown input
- IN+: driver input
- CS: active low chip select (SPI)
- SDI: serial data input (SPI)
- CK: serial clock (SPI)

And following logic outputs:

- SDO: serial logic output (SPI)
- DIAG1: diagnostic signal (open drain)

And following IO pin:

- IN-/DIAG2: driver input or diagnostic open drain output.

Logic input thresholds and output ranges vary according to VDD voltage. In particular, the device is designed to work with VDD supply voltages of 5 V or 3.3 V.

The operation of the driver IOs can be programmed through DIAG_EN bits as described in *Table 10*.

Table 10. Inputs true table (device NOT in “safe state”)

Bit in CFG1 register	Input pins			Output pins	
DIAG_EN	SD	IN+	IN-	GON	GOFF
X	0	X	X	OFF	ON
0	1	0	0	OFF	ON
0	1	0	1	OFF	ON
0	1	1	0	ON	OFF
0	1	1	1	OFF	ON
1	1	0	X(1)	OFF	ON
1	1	1	X(1)	ON	OFF

1. The IN-/DIAG2 pin is used as the open drain output for diagnostic signaling (refer to *Section 7.11 on page 35*).

A deglitch filter is applied to device inputs (SD, IN+, IN-). Each input pulse, positive and negative, shorter than the programmed $t_{deglitch}$ value is neglected by internal logic.

Deglitch time can be programmed as listed in *Table 29 on page 52*.

When the deglitch filter is disabled (INfilter = '00') and the 2-level turn-off function is disabled (2LTOtime = 0x0) or enabled only after a fault event (2LTO_EN = '0'), a minimum input pulse t_{INmin} is required to change the device output status. The minimum input pulse timing filters out both positive and negative pulses at IN+, IN- and SD pins.