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STGIB15CH60TS-L

SLLIMM™- 2nd series IPM, 3-phase inverter, 20 A, 600 V short-circuit rugged IGBT

Datasheet - production data

SDIP2B-26L type L
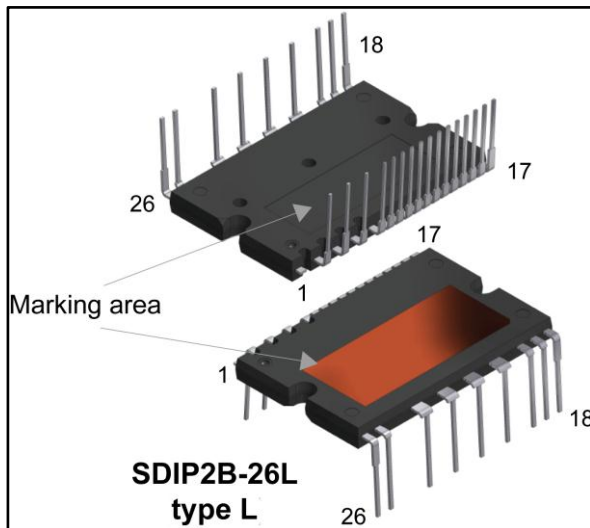
Applications

- 3-phase inverters for motor drives
- Home appliances such as: washing machines, refrigerators, air conditioners and sewing machine

Description

This second series of SLLIMM (small low-loss intelligent molded module) provides a compact, high performance AC motor drive in a simple, rugged design. It combines new ST proprietary control ICs (one LS and one HS driver) with an improved short-circuit rugged trench gate field-stop (TFS) IGBT, making it ideal for 3-phase inverter systems such as home appliances and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

Features

- IPM 20 A, 600 V 3-phase IGBT inverter bridge including 2 control ICs for gate driving and freewheeling diodes
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Internal bootstrap diode
- Undervoltage lockout of gate drivers
- Smart shutdown function
- Short-circuit protection
- Shutdown input/fault output
- Separate open emitter outputs
- Built-in temperature sensor
- Comparator for fault protection
- Short-circuit rugged TFS IGBTs
- Very fast, soft recovery diodes
- 85 kΩ NTC UL 1434 CA 4 recognized
- Fully isolated package
- 1500 Vrms/min. isolation ratings

Table 1: Device summary

Order code	Marking	Package	Packing
STGIB15CH60TS-L	GIB15CH60TS-L	SDIP2B-26L type L	Tube

www.st.com

Contents

1   Internal schematic diagram and pin configuration

Figure 1: Internal schematic diagram and pin configuration

Table 2: Pin description
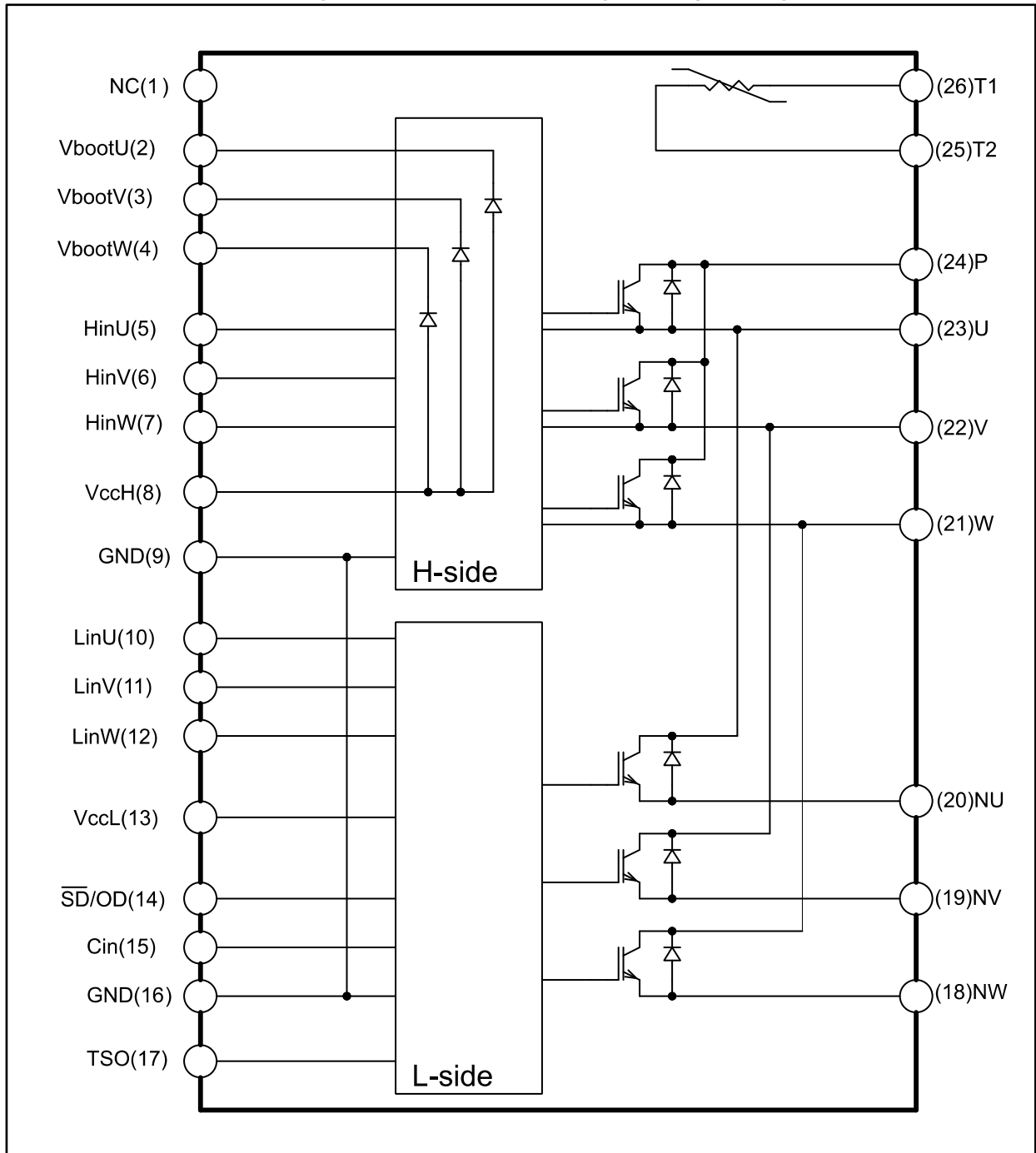
Pin	Symbol	Description
1	NC	-
2	VBOOTu	Bootstrap voltage for U phase
3	VBOOTv	Bootstrap voltage for V phase
4	VBOOTw	Bootstrap voltage for W phase
5	HINu	High-side logic input for U phase
6	HINv	High-side logic input for V phase
7	HINw	High-side logic input for W phase
8	VCCH	High-side low voltage power supply
9	GND	Ground
10	LINu	Low-side logic input for U phase
11	LINv	Low-side logic input for V phase
12	LINw	Low-side logic input for W phase
13	VCCL	Low-side low voltage power supply
14	$\overline{SD}$ /OD	Shutdown logic input (active low) / open-drain (comparator output)
15	CIN	Comparator input
16	GND	Ground
17	TSO	Temperature sensor output
18	NW	Negative DC input for W phase
19	NV	Negative DC input for V phase
20	NU	Negative DC input for U phase
21	W	W phase output
22	V	V phase output
23	U	U phase output
24	P	Positive DC input
25	T2	NTC thermistor terminal 2
26	T1	NTC thermistor terminal 1

2 Absolute maximum ratings

T_J = 25 °C unless otherwise specified

Table 3: Inverter part

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage among P -N_U, -N_V, -N_W	450	V
$V_{PN(surge)}$	Supply voltage surge among P -N_U, -N_V, -N_W	500	V
V_{CES}	Collector-emitter voltage each IGBT	600	V
± I_C	Continuous collector current each IGBT (T_C = 25 °C)	20	A
	Continuous collector current each IGBT (T_C = 80 °C)	15	
± I_{CP}	Peak collector current each IGBT (less than 1 ms)	40	A
P_{TOT}	Total dissipation at T_C = 25 °C each IGBT	81	W
t_{scw}	Short-circuit withstand time, V_{CE} = 300 V, T_J = 125 °C, V_{CC} = V_{boot} = 15 V, V_{IN} = 0 to 5 V	5	µs

Table 4: Control part

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage between V_{CCH}-GND, V_{CCL}-GND	- 0.3	20	V
V_{BOOT}	Bootstrap voltage	- 0.3	619	V
V_{OUT}	Output voltage among U, V, W and GND	V_{BOOT} - 21	V_{BOOT} + 0.3	V
V_{CIN}	Comparator input voltage	- 0.3	20	V
V_{IN}	Logic input voltage applied among HINx, LINx and GND	- 0.3	15	V
$V_{\overline{SD}/OD}$	Open-drain voltage	-0.3	7	V
$I_{\overline{SD}/OD}$	Open-drain sink current		10	mA
V_{TSO}	Temperature sensor output voltage	-0.3	5.5	V
I_{TSO}	Temperature sensor output current		7	mA

Table 5: Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 s)	1500	V
T_j	Power chip operating junction temperature range	-40 to 175	°C
T_C	Module operation case temperature range	-40 to 125	°C

2.1 Thermal data

Table 6: Thermal data

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Thermal resistance junction-case single IGBT	1.85	°C/W
	Thermal resistance junction-case single diode	2.8	

3 Electrical characteristics

T_J = 25 °C unless otherwise specified

3.1 Inverter part

Table 7: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector-cut off current	V_{CE} = 600 V, V_{CC} = V_{boot} = 15 V	-		100	µA
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{CC} = V_{boot} = 15 V, V_{IN}[1] = 0 to 5 V, I_C = 15 A	-	1.55	2.1	V
		V_{CC} = V_{boot} = 15 V, V_{IN} = 0 to 5 V, I_C = 20 A	-	1.65		
V_F	Diode forward voltage	V_{IN} = 0, I_C = 15 A	-	1.54	2.15	V
		V_{IN} = 0, I_C = 20 A	-	1.65		V

Notes:

[1]Applied among HINx, LINx and GND for x = U, V, W.

Table 8: Inductive load switching time and energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{on}[1]	Turn-on time	V_{DD} = 300 V, V_{CC} = V_{boot} = 15 V, V_{IN}[2] = 0 to 5 V, I_C = 15 A	-	320	-	ns
$t_{c(on)}$[1]	Crossover time on		-	160	-	
t_{off}[1]	Turn-off time		-	510	-	
$t_{c(off)}$[1]	Crossover time off		-	102	-	
t_{rr}	Reverse recovery time		-	290	-	
E_{on}	Turn-on switching energy		-	440	-	µJ
E_{off}	Turn-off switching energy		-	213	-	
E_{rr}	Reverse recovery energy		-	59	-	
t_{on}[1]	Turn-on time	V_{DD} = 300 V, V_{CC} = V_{boot} = 15 V, V_{IN}[2] = 0 to 5 V, I_C = 20 A	-	338	-	ns
$t_{c(on)}$[1]	Crossover time on		-	178	-	
t_{off}[1]	Turn-off time		-	500	-	
$t_{c(off)}$[1]	Crossover time off		-	92	-	
t_{rr}	Reverse recovery time		-	300	-	
E_{on}	Turn-on switching energy		-	624	-	µJ
E_{off}	Turn-off switching energy		-	296	-	
E_{rr}	Reverse recovery energy		-	80	-	

Notes:

[1]t_{on} and t_{off} include the propagation delay time of the internal drive. $t_{C(on)}$ and $t_{C(off)}$ are the switching time of the IGBT itself under the internally given gate driving conditions.

[2]Applied among HINx, LINx and GND for x = U, V, W.
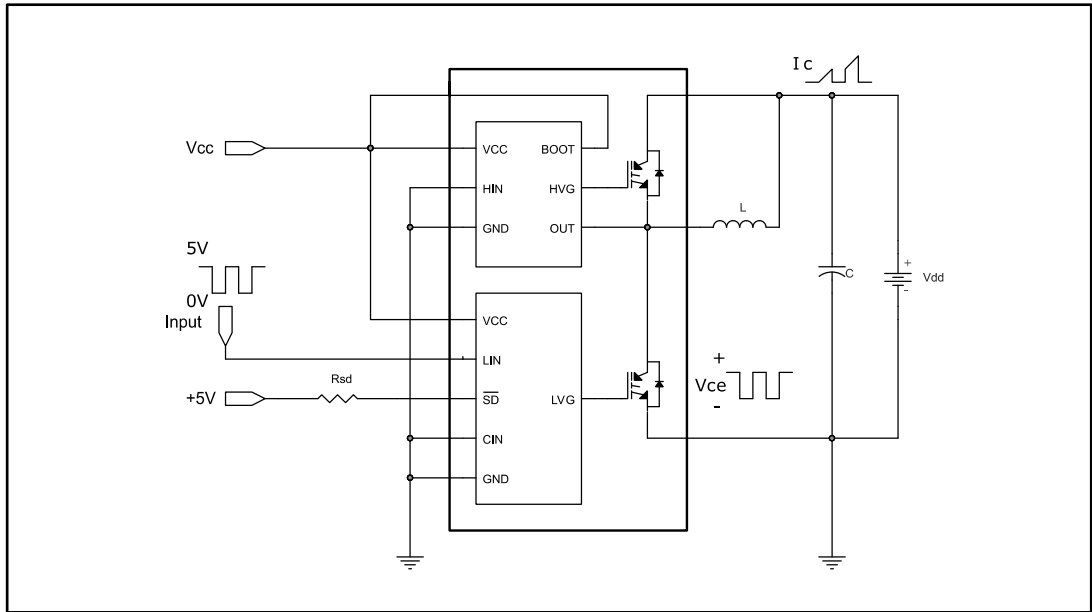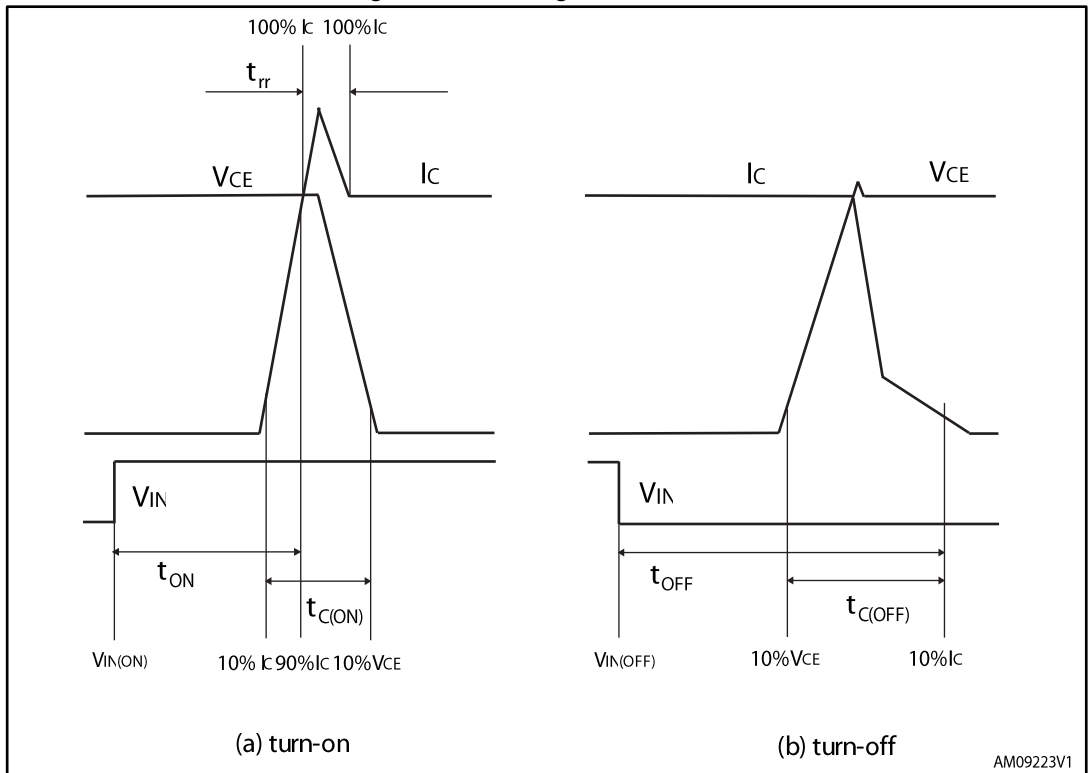
Figure 2: Switching time test circuit

Figure 3: Switching time definition

(a) turn-on   (b) turn-off

3.2   Control / protection part

Table 9: High and low-side drivers

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage				0.8	V
V_{ih}	High logic level voltage		2			V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{INh}	IN logic "1" input bias current	$IN_x = 15$ V	80	150	200	µA
I_{INl}	IN logic "0" input bias current	$IN_x = 0$ V			1	µA
High-side						
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.4	1.7	V
$V_{CC\_th(on)}$	V_{CCH} UV turn-on threshold		11	11.5	12	V
$V_{CC\_th(off)}$	V_{CC} UV turn-off threshold		9.6	10.1	10.6	V
V_{BS_hys}	V_{BS} UV hysteresis		0.5	1	1.6	V
$V_{BS\_th(on)}$	V_{BS} UV turn-on threshold		10.1	11	11.9	V
$V_{BS\_th(off)}$	V_{BS} UV turn-off threshold		9.1	10	10.9	V
I_{QBSU}	Undervoltage V_{BS} quiescent current	$V_{BS} = 9$ V, HINx [1] = 5 V		55	75	µA
I_{QBS}	V_{BS} quiescent current	$V_{CC} = 15$ V, HINx [1] = 5 V		125	170	µA
I_{qccu}	Undervoltage quiescent supply current	$V_{CC} = 9$ V, HINx [1] = 0 V		190	250	µA
I_{qcc}	Quiescent current	$V_{CC} = 15$ V, HINx [1] = 0 V		560	730	µA
$R_{DS(on)}$	BS driver ON-resistance			150		Ω
Low-side						
V_{CC_hys}	V_{CC} UV hysteresis		1.1	1.4	1.6	V
$V_{CCL\_th(on)}$	VCCL UV turn-on threshold		10.4	11.6	12.4	V
$V_{CCL\_th(off)}$	VCCL UV turn-off threshold		9.0	10.3	11	V
I_{qccu}	Undervoltage quiescent supply current	$V_{CC} = 10$ V, $\overline{SD}$ pulled to 5 V through $R_{SD} = 10$ kΩ, CIN = LINx [1] = 0		600	800	µA
I_{qcc}	Quiescent current	$V_{cc} = 15$ V, $\overline{SD} = 5$ V, CIN = LINx [1] = 0		700	900	µA
V_{SSD}	Smart $\overline{SD}$ unlatch threshold		0.5	0.6	0.75	V
I_{SDh}	$\overline{SD}$ logic "1" input bias current	$\overline{SD} = 5$ V	25	50	70	µA
I_{SDl}	$\overline{SD}$ logic "0" input bias current	$\overline{SD} = 0$ V			1	µA

Notes:

[1]Applied among HINx, LINx and GND for x = U, V, W

Table 10: Temperature sensor output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{TSO}	Temperature sensor output voltage	$T_j = 25\ °C$	0.974	1.16	1.345	V
I_{TSO_SNK}	Temperature sensor sink current capability			0.1		mA
I_{TSO_SRC}	Temperature sensor source current capability		4			mA

Table 11: Sense comparator (VCC = 15 V, unless otherwise is specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CIN}	CIN input bias current	$V_{CIN} = 1\ V$	-0.2		0.2	µA
V_{ref}	Internal reference voltage		460	510	560	mV
V_{OD}	Open-drain low level output voltage	$I_{od} = 5\ mA$			500	mV
t_{CIN_SD}	C_{IN} comparator delay to $\overline{SD}$	$\overline{SD}$ pulled to 5 V through $R_{SD} = 10\ k\Omega$; measured applying a voltage step 0-1 V to pin CIN 50% CIN to 90% $\overline{SD}$	240	320	410	ns
SR_{SD}	$\overline{SD}$ fall slew rate	$\overline{SD}$ pulled to 5 V through $R_{SD} = 10\ k\Omega$; CL=1 nF through $\overline{SD}$ and ground; 90% $\overline{SD}$ to 10% $\overline{SD}$		25		V/µs

Comparator is enabled even if V_{CC} is in UVLO condition but higher than 4 V.

4 Fault management

The device integrates an open-drain output connected to $\overline{SD}$ pin. As soon as a fault occurs the open-drain is activated and LVGx outputs are forced low. Two types of fault can be pointed out:

- Overcurrent (OC) sensed by the internal comparator (see further details in *Section 4.2: "Smart shutdown function"*)
- Undervoltage on supply voltage (V_{CC})

Each fault enables the $\overline{SD}$ open-drain for a different time; refer to the following *Table 12: "Fault timing"*

Table 12: Fault timing

Symbol	Parameter	Event time	SD open-drain enable time result
OC	Overcurrent event	≤ 20 µs	20 µs
		≥ 20 µs	OC time
UVLO	Undervoltage lock-out event	≤ 50 µs	50 µs
		≥ 50 µs until the VCC_LS exceeds the VCC_LS UV turn-ON threshold	UVLO time

Actually, the device remains in a fault condition ($\overline{SD}$ at low logic level and LVGx outputs disabled) for a time also depending on RC network connected to $\overline{SD}$ pin. The network generates a time contribute, which is added to the internal value.

Figure 4: Overcurrent timing (without contribution of RC network on $\overline{SD}$)
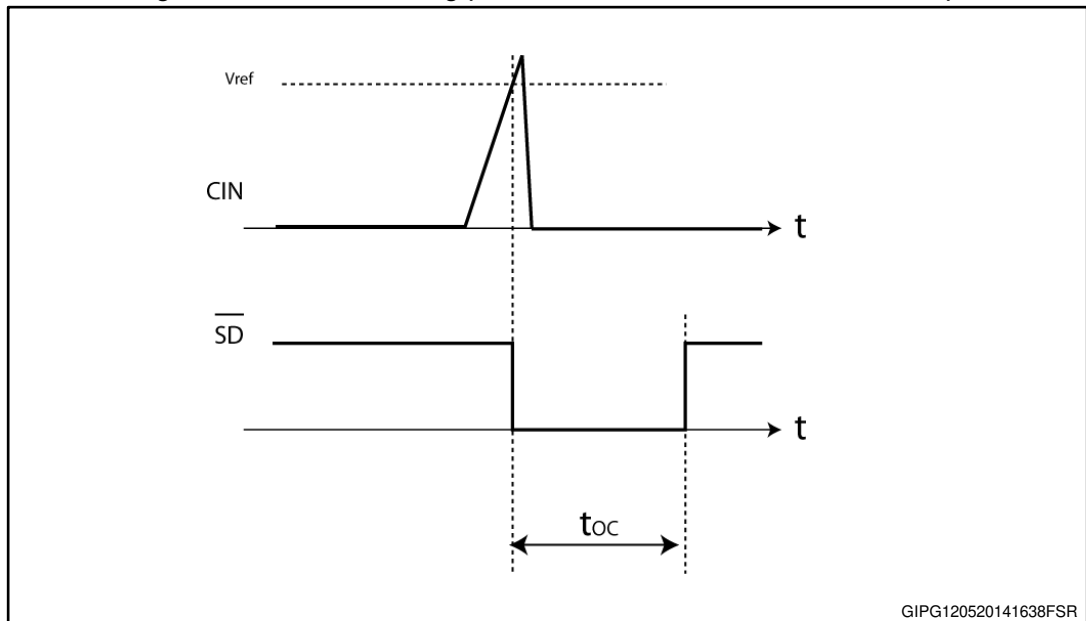
Figure 5: UVLO timing (without contribution of RC network on $\overline{SD}$)
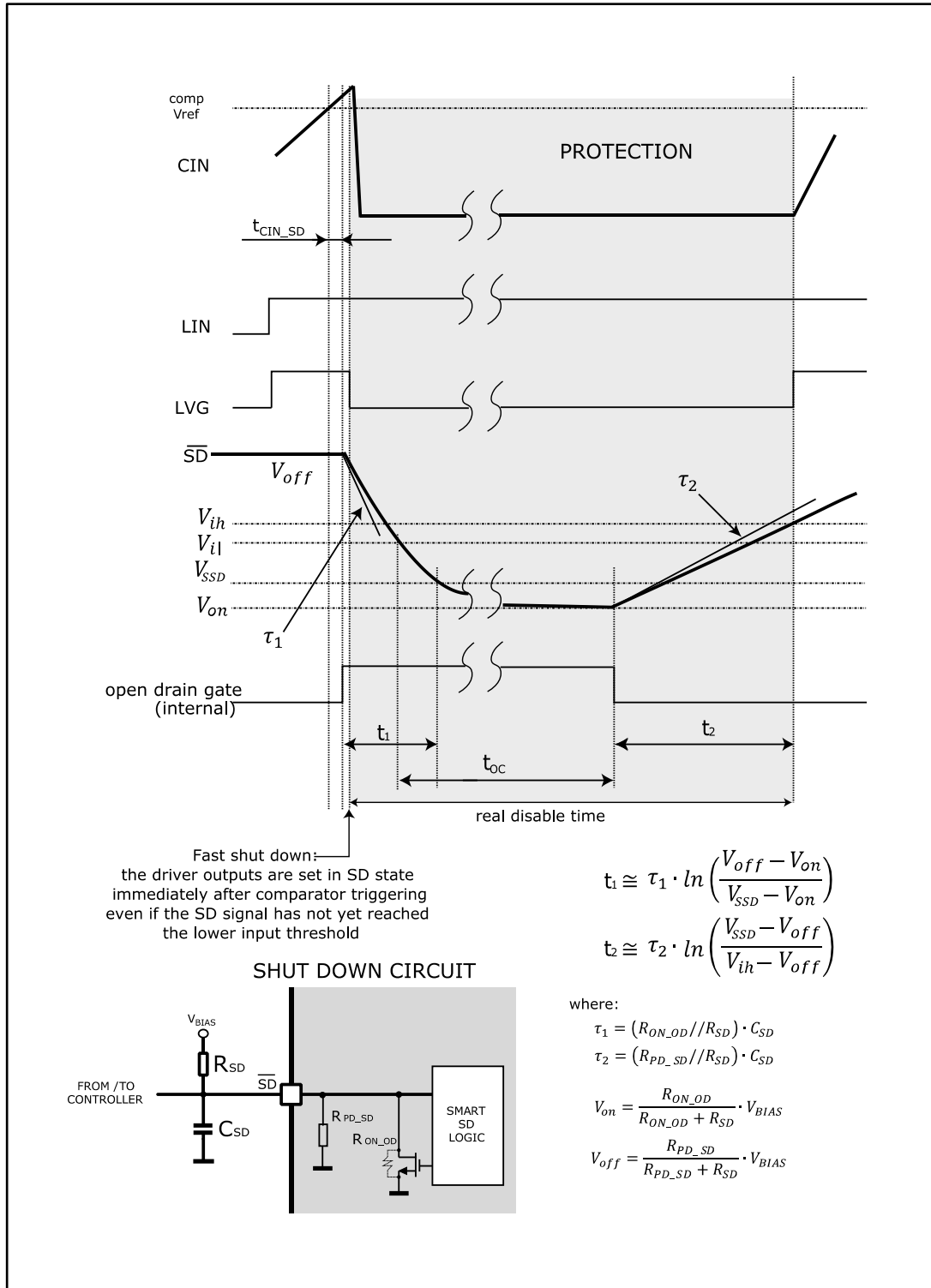

GIPG120520141644FSR
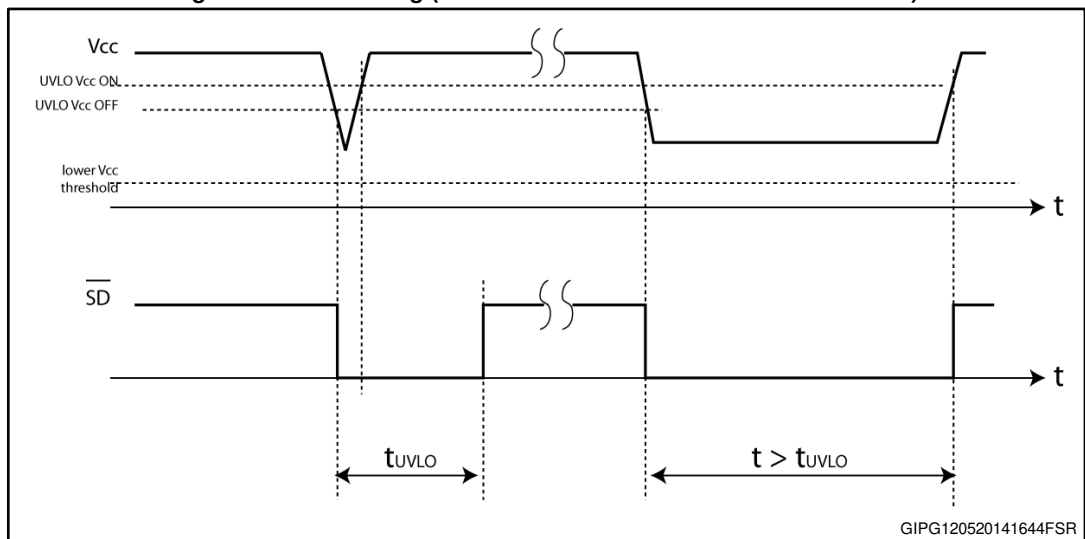
4.1 TSO output

The device integrates the temperature sensor. A voltage proportional to the die temperature is available on TSO pin. When this function is not used this pin can be left floating.

4.2 Smart shutdown function

The device integrates a comparator committed to the fault sensing function. The comparator input can be connected to an external shunt resistor in order to implement a simple overcurrent detection function.

The output signal of the comparator is fed to an integrated MOSFET with the open-drain output available on $\overline{SD}$ input. When the comparator triggers, the device is set in shutdown state and its outputs are all set to low level.

Figure 6: Smart shutdown timing waveforms in case of overcurrent event

$$t_1 \cong \tau_1 \cdot ln\left(\frac{V_{off} - V_{on}}{V_{SSD} - V_{on}}\right)$$

$$t_2 \cong \tau_2 \cdot ln\left(\frac{V_{SSD} - V_{off}}{V_{ih} - V_{off}}\right)$$

where:

$$\tau_1 = (R_{ON\_OD}//R_{SD}) \cdot C_{SD}$$

$$\tau_2 = (R_{PD\_SD}//R_{SD}) \cdot C_{SD}$$

$$V_{on} = \frac{R_{ON\_OD}}{R_{ON\_OD} + R_{SD}} \cdot V_{BIAS}$$

$$V_{off} = \frac{R_{PD\_SD}}{R_{PD\_SD} + R_{SD}} \cdot V_{BIAS}$$

R_{ON_OD} = V_{OD}/5 mA see *Table 11: "Sense comparator (VCC = 15 V, unless otherwise is specified)"*; R_{PD_SD} (typ.) = 5 V/I_{SDh}

In common overcurrent protection architectures, the comparator output is usually connected to the $\overline{SD}$ input and an RC network is connected to this $\overline{SD}$ line so to create a monostable circuit which implements a protection time following to the fault condition.

Differently from the common fault detection systems, the device smart shutdown architecture allows the output gate driver to be immediately turned-off in case of fault, by minimizing the propagation delay between the fault detection event and the output switch-off. In fact, the time delay between the fault and the output turn-off is no more dependent on the RC value of the external network connected to the pin.

In the smart shutdown circuitry, the fault signal has a preferential path which directly switches off the outputs after the comparator triggering.

At the same time the internal logic turns on the open-drain output and holds it on until the $\overline{SD}$ voltage goes below the V_{SSD} threshold and toc time is elapsed.

The driver outputs restart following the input pins as soon as the voltage on the $\overline{SD}$ pin reaches the highest threshold of this $\overline{SD}$ logic input.

The smart shutdown system allows the time constant (that is the disable time after the fault event) of the external RC network to be increased up to very wide values without increasing the delay time of the protection.

5 Application circuit example

Figure 7: Application circuit example
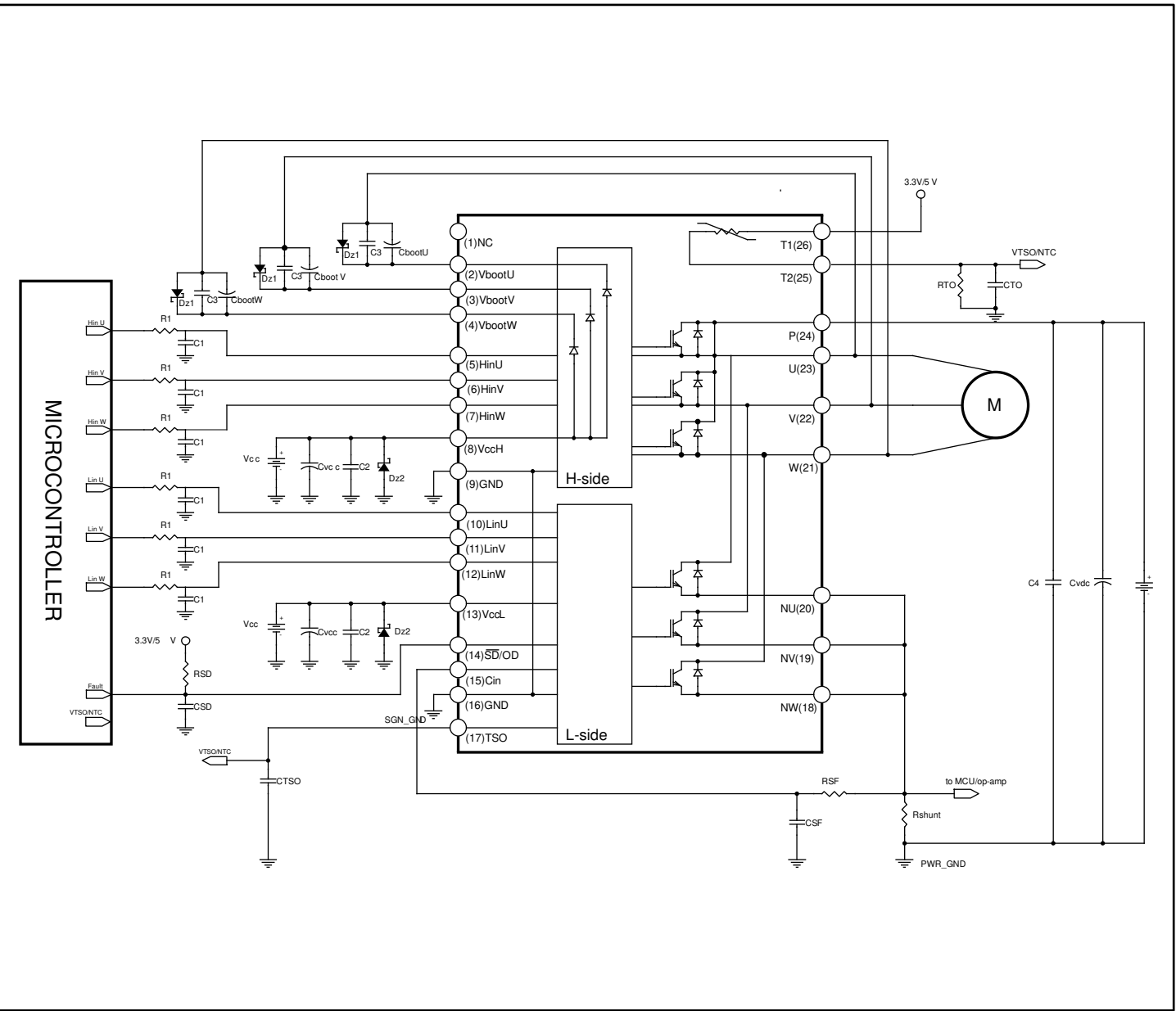
Application designers are free to use a different scheme according to the specifications of the device.

5.1   Guidelines

1. Input signals HIN, LIN are active high logic. A 100 kΩ (typ.) pull-down resistor is built-in for each input pin. To avoid input signal oscillations, the wiring of each input should be as short as possible and the use of RC filters (R1, C1) on each input signal is suggested. The filters should be with a constant time of about 100 ns and placed as close as possible to the IPM input pins.

2. The use of a bypass capacitor C_{VCC} (aluminum or tantalum) can reduce the transient circuit demand on the power supply. Besides, to reduce high frequency switching noise distributed on the power lines, a decoupling capacitor C_2 (100 to 220 nF, with low ESR and low ESL) should be placed as close as possible to each V_{CC} pin and in parallel with the bypass capacitor.

3. The use of the RC filter (RSF, CSF) prevents protection circuit malfunction. The constant time (RSF x CSF) should be set to 1 μs and the filter must be placed as close as possible to the CIN pin.

4. The $\overline{SD}$ is an input/output pin (open-drain type if it is used as output). It should be pulled up to a power supply (i.e., MCU bias at 3.3/5 V) by a resistor value that is able to keep the I_{od} no higher than 5 mA ($V_{OD} ≤ 500$ mV when open-drain MOSFET is ON). The filter on $\overline{SD}$ should be sized to get a desired restarting time after a fault event and placed as close as possible to the $\overline{SD}$ pin.

5. A decoupling capacitor C_{TSO} between 1 nF and 10 nF can be used to increase the noise immunity of the TSO thermal sensor; a similar decoupling capacitor C_{OT} (between 10 nF and 100 nF) can be implemented if the NTC thermistor is available and used. In both cases, their effectiveness is improved if these capacitors are placed close to the MCU.

6. The decoupling capacitor C_3 (100 to 220 nF with low ESR and low ESL) in parallel with each C_{boot} filters high frequency disturbances. Both C_{boot} and C_3 (if present) should be placed as close as possible to the U,V,W and V_{boot} pins. Bootstrap negative electrodes should be connected to U, V, W terminals directly and separated from the main output wires.

7. To prevent overvoltage on the V_{CC} pin, a Zener diode (Dz1) can be used. Similarly on the V_{boot} pin, a Zener diode(Dz2) can be placed in parallel with each C_{boot}.

8. The use of the decoupling capacitor C_4 (100 to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor C_{vdc} prevents surge destruction. Both capacitors C_4 and C_{vdc} should be placed as close as possible to the IPM (C_4 has priority over C_{vdc}).

9. By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an optocoupler is possible.

10. Low inductance shunt resistors should be used for phase leg current sensing.

11. In order to avoid malfunctions, the wiring on N pins, the shunt resistor and PWR_GND should be as short as possible.

12. The connection of SGN_GND to PWR_GND on one point only (close to the shunt resistor terminal) can reduce the impact of power ground fluctuation.

These guidelines ensure the specifications of the device for application designs. For further details, please refer to the relevant application note.

Table 13: Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply voltage	Applied among P-Nu, N_V, N_w		300	400	V
V_{CC}	Control supply voltage	Applied to V_{CC}-GND	13.5	15	18	V
V_{BS}	High-side bias voltage	Applied to V_{BOOTi}-OUT_i for i = U, V, W	13		18	V
t_{dead}	Blanking time to prevent arm-short	For each input signal	1.0			µs
f_{PWM}	PWM input signal	-40 °C < T_C < 100 °C -40 °C < T_j < 125 °C			20	kHz
T_C	Case operation temperature				100	°C

6 NTC thermistor

Table 14: NTC thermistor

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{25}	Resistance	T = 25 °C		85	-	kΩ
R_{125}	Resistance	T = 125 °C		2.6	-	kΩ
B	B-constant	T = 25 to 100 °C		4092	-	K
T	Operating temperature range		-40		125	°C

Figure 8: NTC resistance vs. temperature
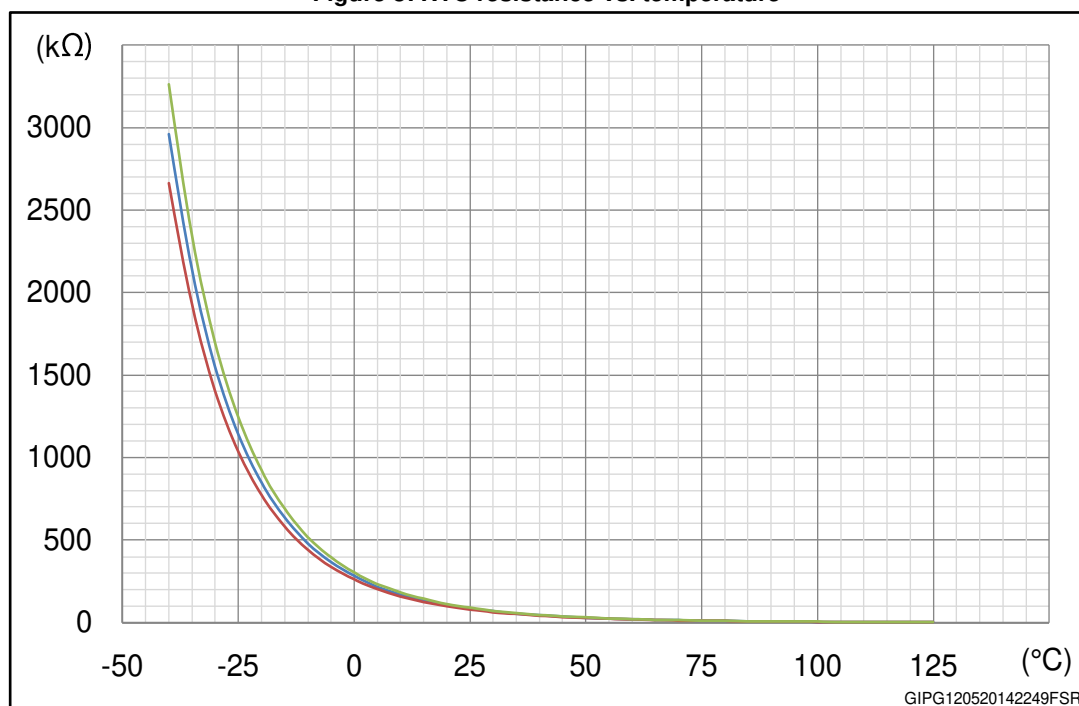
Figure 9: NTC resistance vs. temperature - zoom
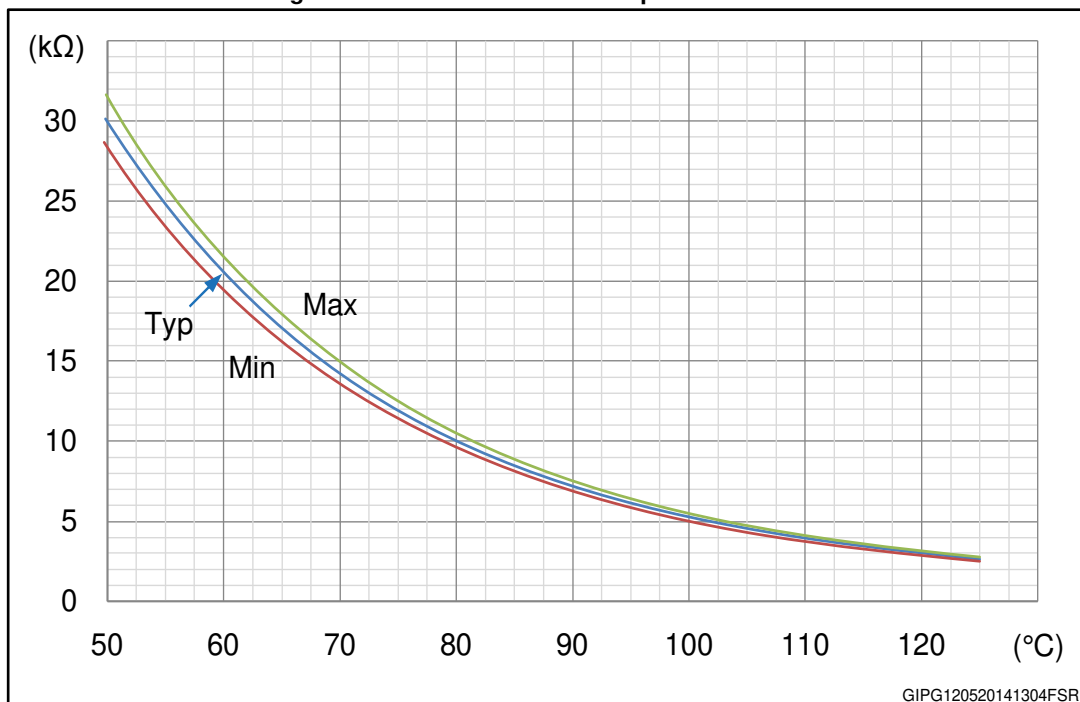
7 Electrical characteristics (curves)

Figure 10: Output characteristics

Figure 11: $V_{CE(sat)}$ vs. collector current

Figure 12: Diode V_F vs. forward current

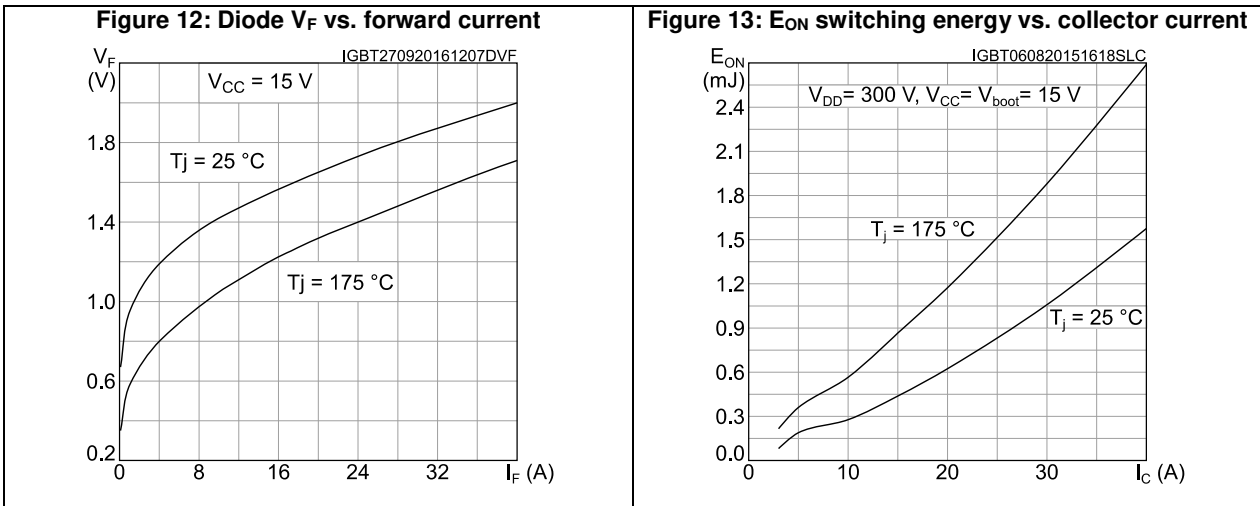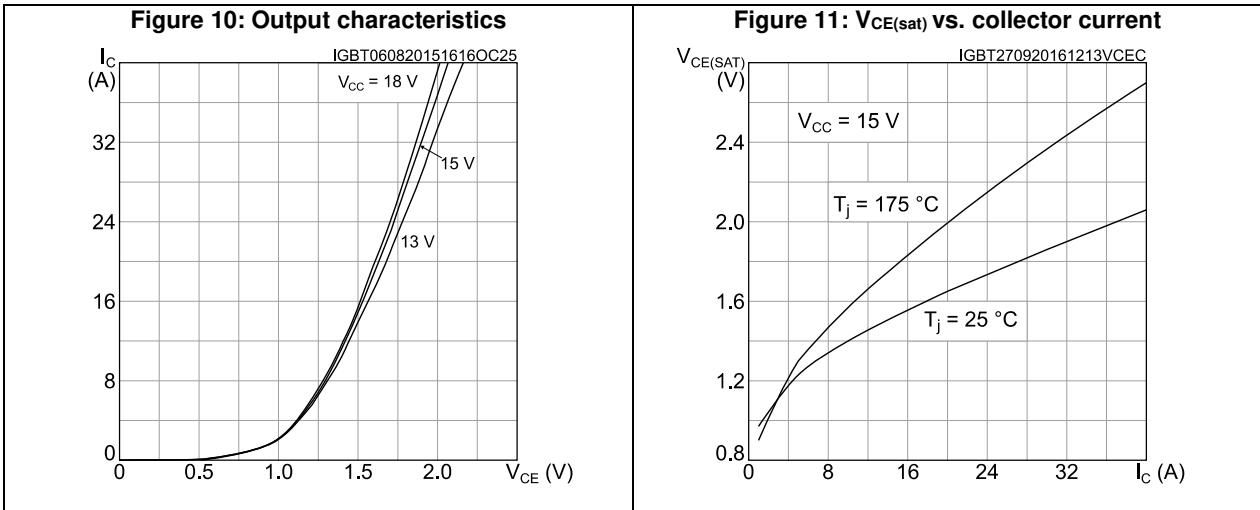**Figure 13: E_{ON} switching energy vs. collector current**

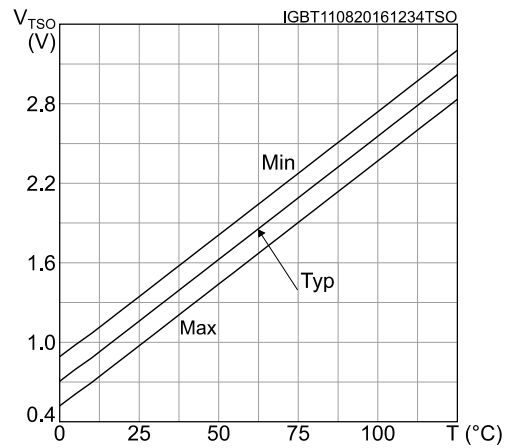| Figure 14: E$_{OFF}$ switching energy vs. collector current	Figure 15: V$_{TSO}$ output characteristics vs. LVIC temperature
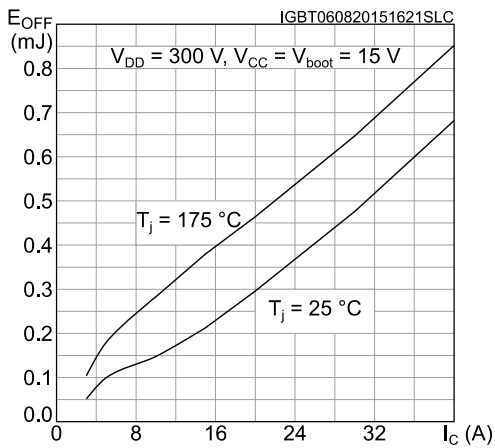
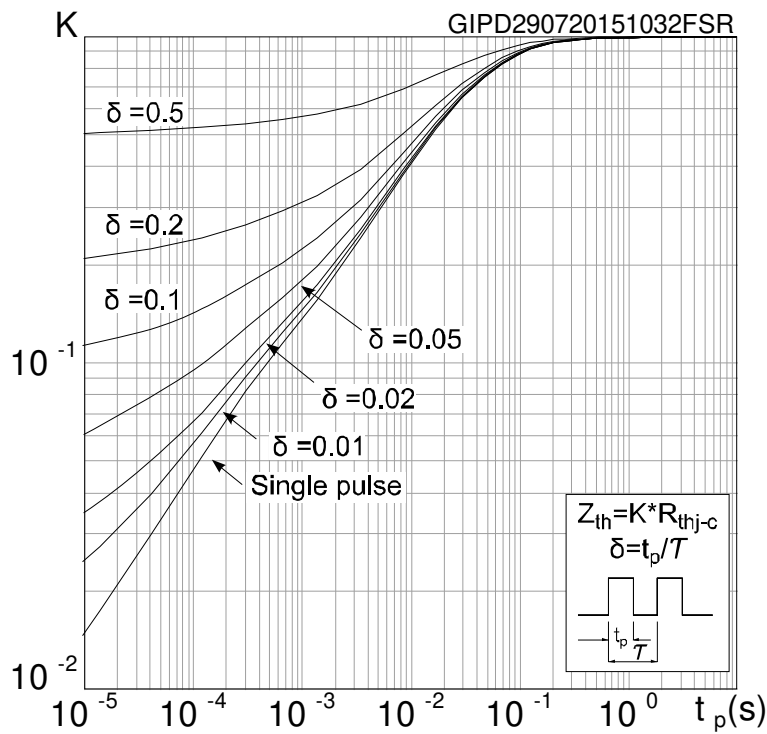Figure 16: Thermal impedance for the SDIP2B-26L IGBT

$$Z_{th}=K*R_{thj-c}$$
$$\delta=t_p/T$$

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

8.1 SDIP2B-26L type L package information
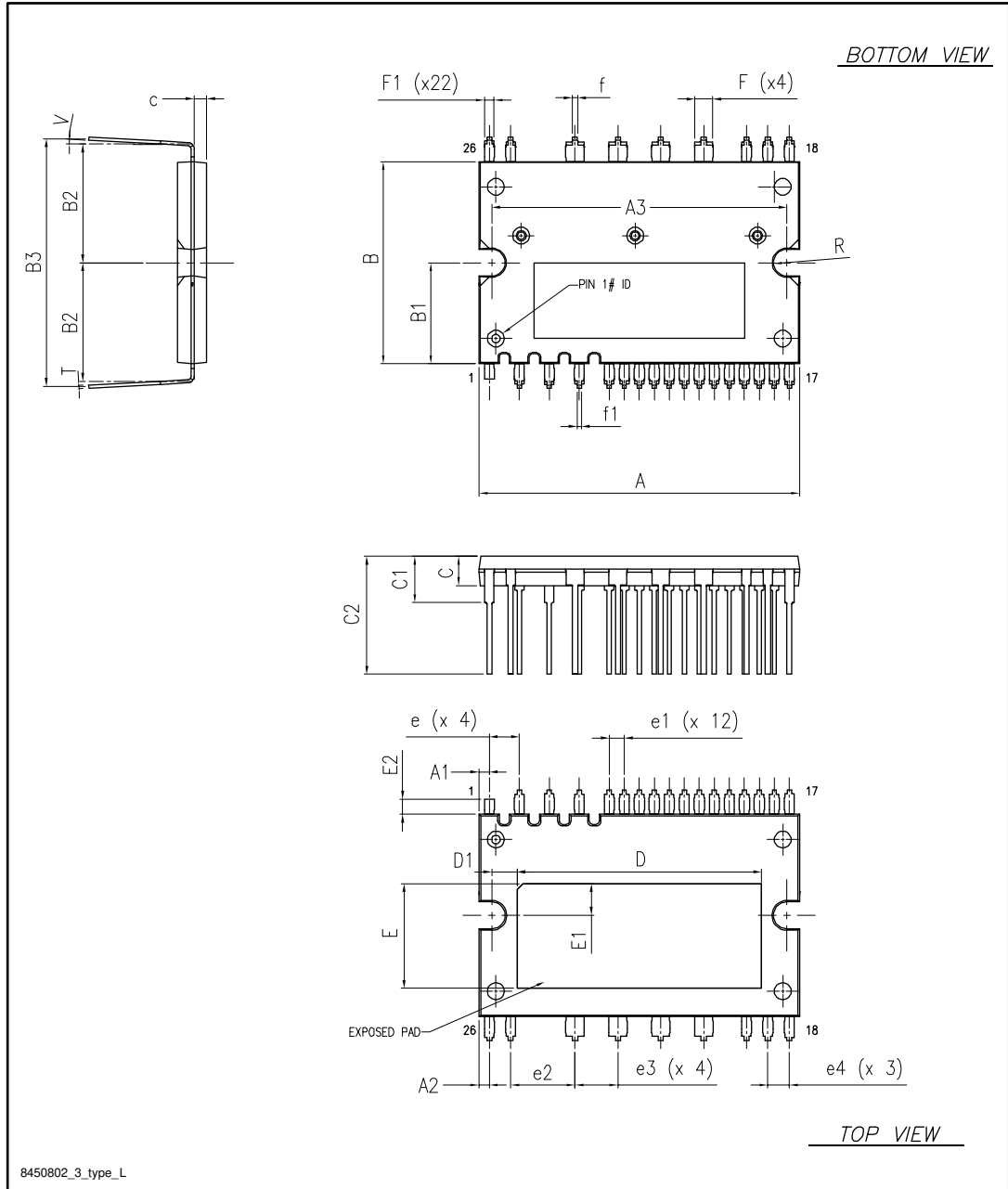
Figure 17: SDIP2B-26L type L package outline

Table 15: SDIP2B-26L type L package mechanical data (dimensions are in mm)

Ref.	Dimensions
A	38.00 ± 0.50
A1	1.22 ± 0.25
A2	1.22 ± 0.25
A3	35.00 ± 0.30
c	1.50 ± 0.05
B	24.00 ± 0.50
B1	12.00
B2	14.40 ± 0.50
B3	29.40 ± 0.50
C	3.50 ± 0.20
C1	5.50 ± 0.50
C2	14.00 ± 0.50
e	3.556 ± 0.200
e1	1.778 ± 0.200
e2	7.62 ± 0.20
e3	5.08 ± 0.20
e4	2.54 ± 0.20
D	28.95 ± 0.50
D1	3.025 ± 0.300
E	12.40 ± 0.50
E1	3.75 ± 0.30
E2	1.80
f	0.60 ± 0.15
f1	0.50 ± 0.15
F	2.10 ± 0.15
F1	1.10 ± 0.15
R	1.60 ± 0.20
T	0.400 ± 0.025
V	0° / 5°

9   Revision history

Table 16: Document revision history

Date	Revision	Changes
23-Jun-2014	1	Initial release.
27-Aug-2014	2	Updated *Table 1: Device summary*.
06-Aug-2015	3	Text and formatting changes throughout document. Updated *cover page title* and *features.* Updated *Section 2: Absolute maximum ratings*. Updated *Section 3: Electrical characteristics*. Updated *Section 6: Recommendations*. Added *Section 8: Electrical characteristics (curves)*.
09-Sep-2015	4	Modified: *Features* Modified: *Figure 1, 6* and *7* Datasheet promoted to preliminary data to production data Minor text changes
12-Oct-2016	5	Modified *Table 7: "Static"*, *Table 9: " High and low side drivers"* and *Table 11: "Sense comparator (VCC = 15 V, unless otherwise is specified)"* Modified *Section 5.1: "Guidelines"* Modified *Figure 11: "VCE(sat) vs. collector current"*, *Figure 12: "Diode VF vs. forward current"* and *Figure 15: "VTSO output characteristics vs. LVIC temperature"* Updated *Section 8.1: "SDIP2B-26L type L package information"* Minor text changes
18-Nov-2016	6	Updated *Table 7: "Static"*.

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