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# STK672-440BN-E

Thick-Film Hybrid IC

## 2-phase Stepper Motor Driver

ON Semiconductor®

<http://onsemi.com>

### Overview

The STK672-440BN-E is a hybrid IC for use as a unipolar, 2-phase stepper motor driver with PWM current control.

### Applications

- Office photocopiers, printers, etc.

### Features

- Built-in motor terminal open detection function, overcurrent detection function, overheat detection function (output current OFF).
- FAULT1 signal (active low) is output when any of motor terminal open, overcurrent or overheat is detected. The FAULT2 signal is used to output the result of activation of protection circuit detection at 3 levels.
- Built-in power on reset function.
- A micro-step sine wave-driven driver can be activated merely by inputting an external clock.
- External pins can be used to select 2, 1-2 (including pseudo-micro), W1-2, 2 W1-2, or 4W1-2 excitation.
- The switch timing of the 4-phase distributor can be switched by setting an external pin (MODE3) to detect either the rise and fall, or rise only, of CLOCK input.
- Phase is maintained even when the excitation mode is switched. Rotational direction switching function.
- Supports schmitt input for 2.5V high level input.
- Incorporating a current detection resistor (0.122Ω: resistor tolerance  $\pm 2\%$ ), motor current can be set using two external resistors.
- The ENABLE pin can be used to cut output current while maintaining the excitation mode.
- With a wide current setting range, power consumption can be reduced during standby.
- No motor sound is generated during hold mode due to external excitation current control.
- PWM operation is separately excited system. As for PWM phase the constant current control which shifts the phase of Ach Beh.
- Supports compatible pins with STK672-432BN/-442BN-E.

### Specifications

#### Absolute Maximum Ratings at $T_c = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	Vcc max	No signal	50	V
Maximum supply voltage 2	VDD max	No signal	-0.3 to 6.0	V
Input voltage	Vin max	Logic input pins	-0.3 to 6.0	V
Output current 1	IOP max	10μs 1 pulse (resistance load)	20	A
Output current 2	IOH max	VDD = 5V, CLOCK $\geq$ 200Hz	3.5	A
Output current 3	IOF max	16pin Output current	10	mA
Allowable power dissipation 1	PdMF max	With an arbitrarily large heat sink. Per MOSFET	8.3	W
Allowable power dissipation 2	PdPK max	No heat sink	3.1	W
Operating substrate temperature	Tcmax		105	$^\circ\text{C}$
Junction temperature	Tjmax		150	$^\circ\text{C}$
Storage temperature	Tstg		-40 to 125	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 28 of this data sheet.

# STK672-440BN-E

## Allowable Operating Ranges at Tc=25°C

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage 1	V <sub>CC</sub>	With signals applied	0 to 46	V
Operating supply voltage 2	V <sub>DD</sub>	With signals applied	5±5%	V
Input high voltage	V <sub>IH</sub>	Pins 10, 11, 12, 13, 14, 15, 17, V <sub>DD</sub> =5±5%	2.5 to V <sub>DD</sub>	V
Input low voltage	V <sub>IL</sub>	Pins 10, 11, 12, 13, 14, 15, 17, V <sub>DD</sub> =5±5%	0 to 0.8	V
CLOCK frequency	f <sub>CL</sub>	Minimum pulse width: at least 10μs	0 to 50	kHz
Output current	I <sub>OH</sub>	Tc=105°C, CLOCK≥200Hz	3.0	A
Recommended operating substrate temperature	Tc	No condensation	0 to 105	°C
Recommended Vref range	Vref	Tc=105°C	0.2 to 1.8	V

## Electrical Characteristics at Tc=25°C, V<sub>CC</sub>=24V, V<sub>DD</sub>=5.0V \*1

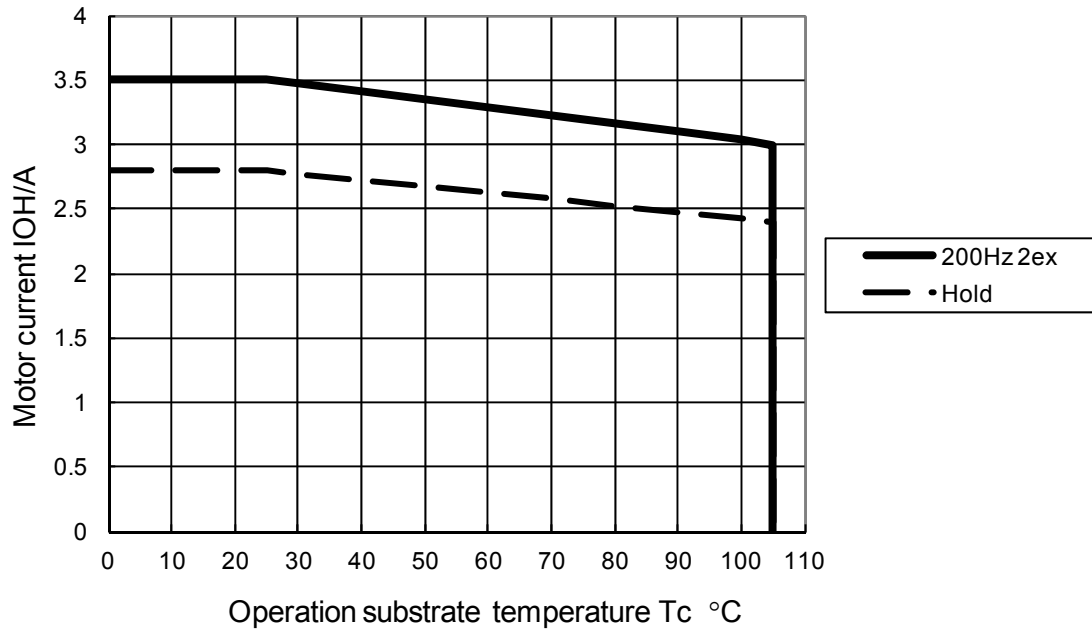
Parameter		Symbol	Conditions	min	typ	max	unit			
V <sub>DD</sub> supply current		I <sub>CCO</sub>	V <sub>DD</sub> =5.0V, ENABLE=Low		7.2	8.5	mA			
Output average current *2		I <sub>oave</sub>	R/L=1Ω/0.62mH in each phase	0.27	0.32	0.37	A			
FET diode forward voltage		V <sub>df</sub>	I <sub>f</sub> =1A (R <sub>L</sub> =23Ω)		1	1.6	V			
Output saturation voltage		V <sub>sat</sub>	R <sub>L</sub> =23Ω		0.25	0.38	V			
Control input pin	Input voltage	V <sub>IH</sub>	Pins 10, 11, 12, 13, 14, 15, 17	2.5		V <sub>DD</sub>	V			
		V <sub>IL</sub>	Pins 10, 11, 12, 13, 14, 15, 17	-0.3		0.8	V			
	5V level input current	I <sub>I<sub>LH</sub></sub>	Pins 10, 11, 12, 13, 14, 15, 17=5V		50	75	μA			
	GND level input current	I <sub>I<sub>LL</sub></sub>	Pins 10, 11, 12, 13, 14, 15, 17=GND			10	μA			
Vref input bias current		I <sub>IB</sub>	Pin 19 =1.0V			1	μA			
FAULT1 pin	Output low voltage	V <sub>OLF</sub>	Pin 16 (I <sub>O</sub> =5mA)		0.25	0.5	V			
	5V level leakage current	I <sub>I<sub>LF</sub></sub>	Pin 16 =5V			10	μA			
FAULT2 pin	Motor terminal open detection output voltage	V <sub>OF1</sub>	Pin 8 (when all protection functions have been activated)	0.0	0.01	0.2	V			
	Overcurrent detection output voltage	V <sub>OF2</sub>		2.4	2.5	2.6				
	Overheat detection output voltage	V <sub>OF3</sub>		3.1	3.3	3.5				
Overheat detection temperature		TSD	Design guarantee		144		°C			
PWM frequency		f <sub>c</sub>		41	48	55	kHz			
Drain-source cut-off current		I <sub>DSS</sub>	V <sub>DS</sub> =100V, Pins 2, 6, 9, 18=GND			1	μA			
A•B Chopper Current Ratio	4W1-2	2W1-2	W1-2	1-2	Vref *3	0=15/16, 16/16	100	%		
	4W1-2	2W1-2				0=14/16	97			
	4W1-2					0=13/16	95			
	4W1-2	2W1-2	W1-2			0=12/16	93			
	4W1-2					0=11/16	87			
	4W1-2	2W1-2				0=10/16	83			
	4W1-2					0=9/16	77			
	4W1-2	2W1-2	W1-2	1-2		0=8/16	71			
	4W1-2					0=7/16	64			
	4W1-2	2W1-2				0=6/16	55			
	4W1-2					0=5/16	47			
	4W1-2	2W1-2	W1-2			0=4/16	40			
	4W1-2					0=3/16	30			
	4W1-2	2W1-2				0=2/16	20			
	4W1-2					0=1/16	11			
	2								100	

### Notes

- \*1: A fixed-voltage power supply must be used.
- \*2: The value for I<sub>oave</sub> assumes that the lead frame of the product is soldered to the mounting circuit board.
- \*3: The values given for Vref are design targets, no measurement is performed.

# STK672-440BN-E

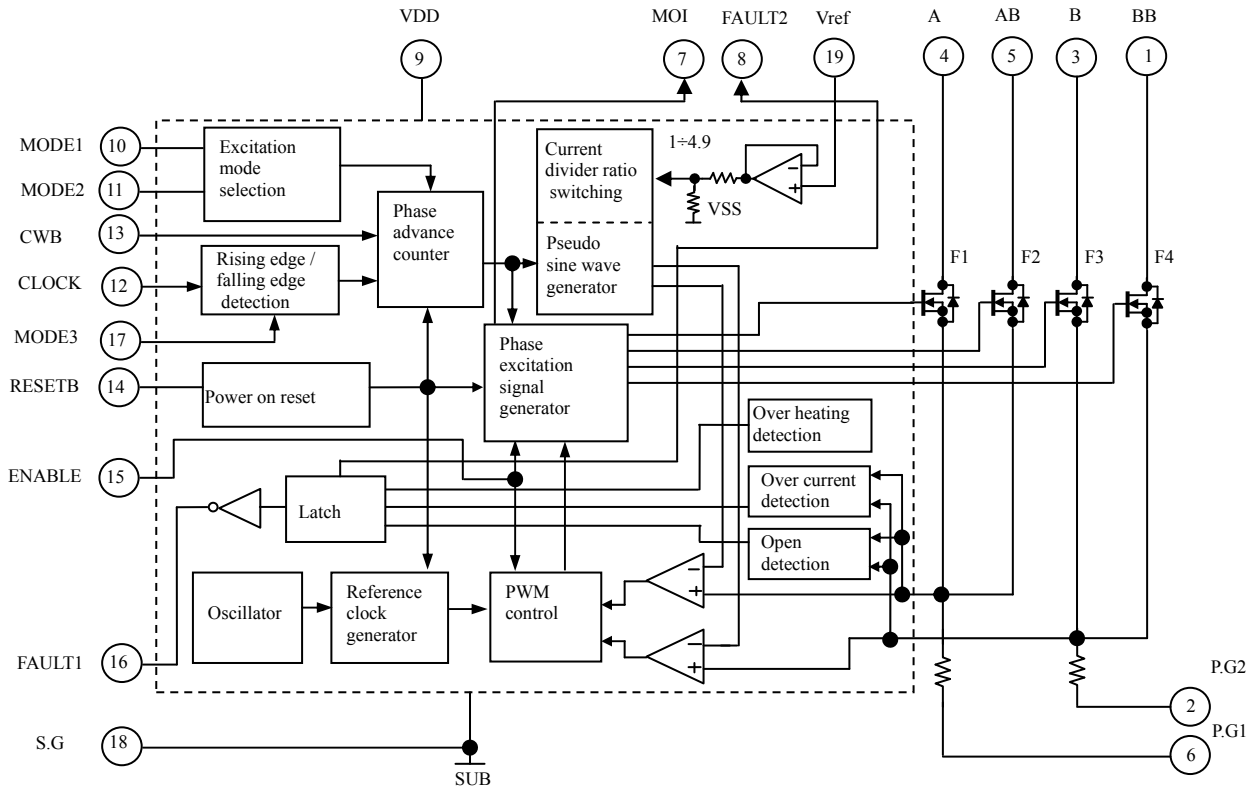
Derating Curve of Motor Current,  $I_{OH}$ , vs. STK672-440BN-E Operating Substrate Temperature,  $T_c$



## Notes

- The current range given above represents conditions when output voltage is not in the avalanche state.
- If the output voltage is in the avalanche state, see the allowable avalanche energy for STK672-4\*\* series hybrid ICs given in a separate document.
- The operating substrate temperature,  $T_c$ , given above is measured while the motor is operating. Because  $T_c$  varies depending on the ambient temperature,  $T_a$ , the value of  $I_{OH}$ , and the continuous or intermittent operation of  $I_{OH}$ , always verify this value using an actual set.
- The  $T_c$  temperature should be checked in the center of the metal surface of the product package.

Block Diagram

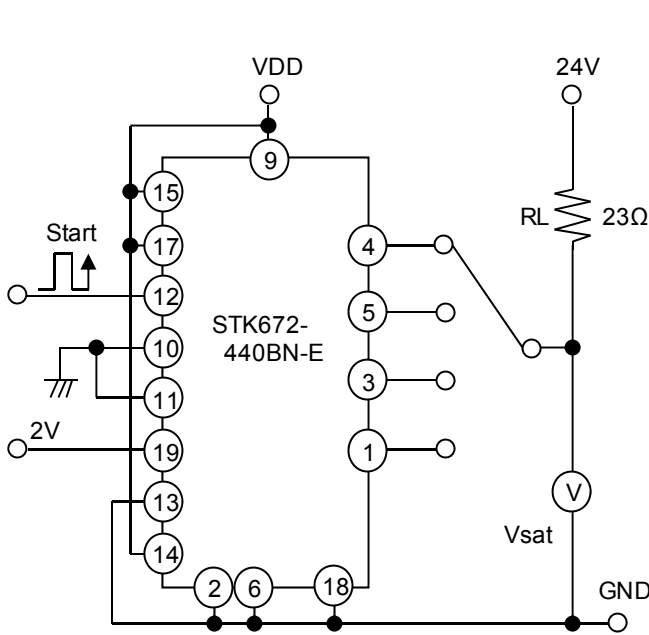


# STK672-440BN-E

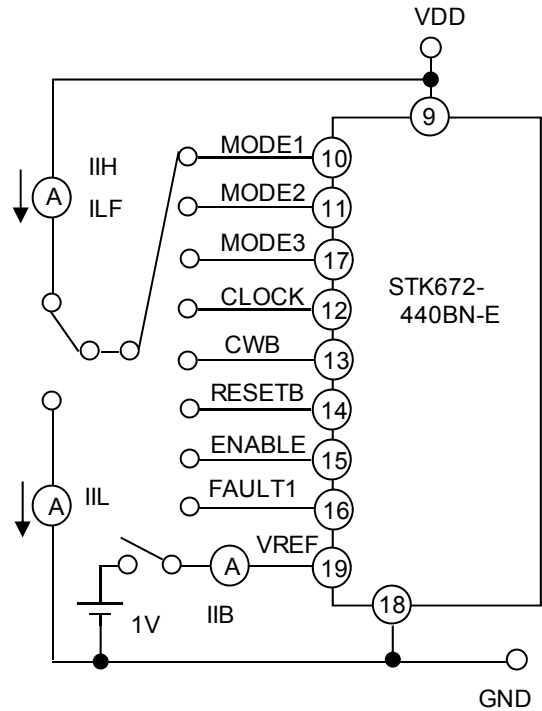
## Measurement Circuit

(The terminal which is not appointed is open. The measurement circuit of STK672-440BN-E is the same as STK672-442BN-E.)

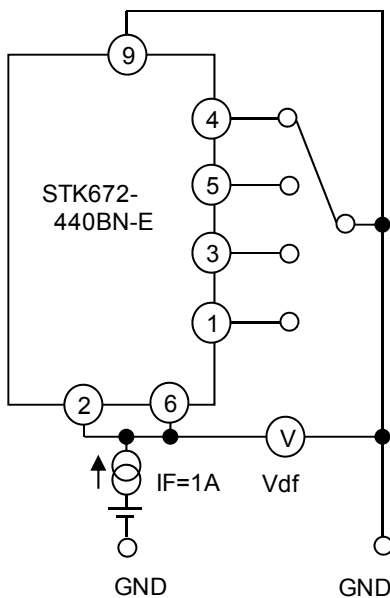
### ◆ Vsat



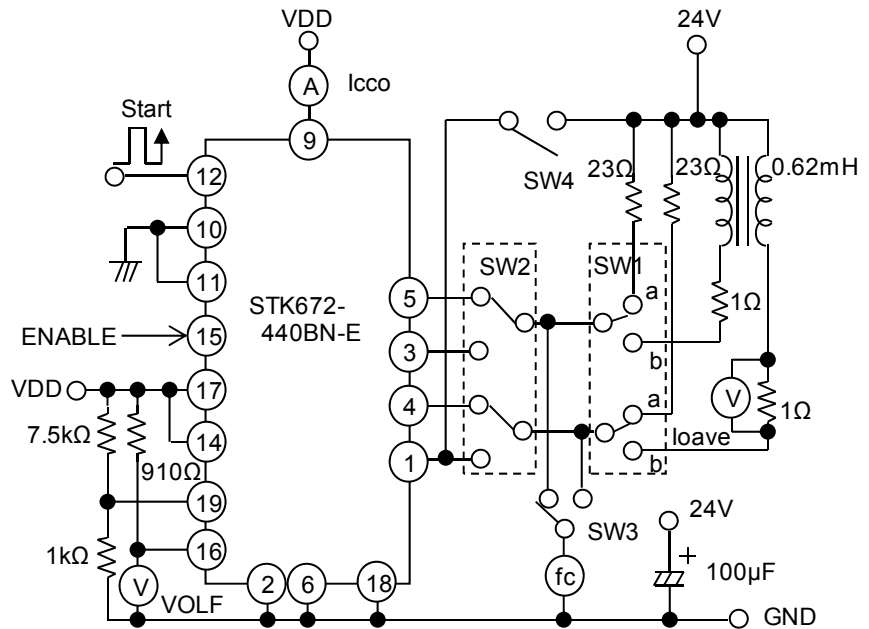
### ◆ I<sub>IH</sub>, I<sub>IL</sub>, I<sub>IB</sub>, I<sub>LF</sub>



### ◆ V<sub>df</sub>



### ◆ I<sub>cco</sub>, I<sub>oave</sub>, f<sub>c</sub>, V<sub>OLF</sub>



I<sub>oave</sub> measurement : Set switch SW2 in the setting SW1 to 'b'.

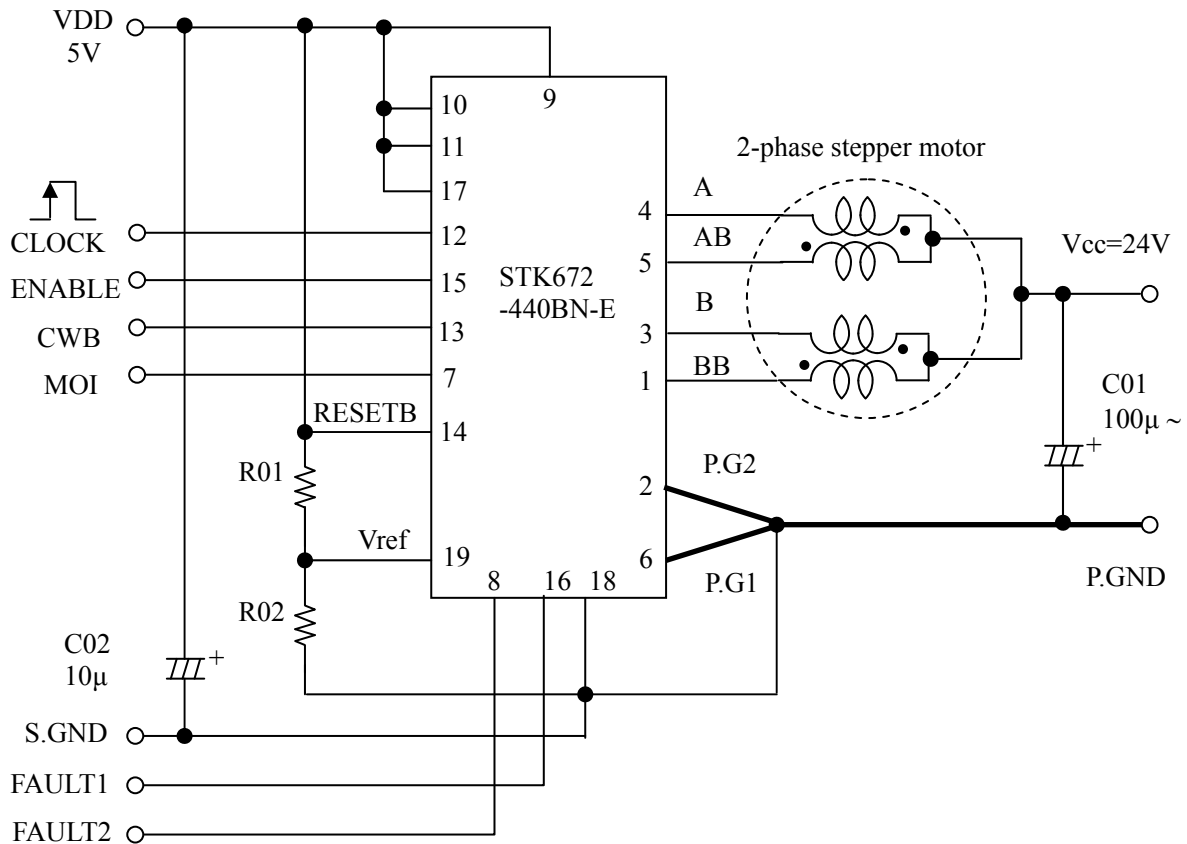
f<sub>c</sub> measurement : Set switch SW3 in the setting SW1 to 'a'.

I<sub>cco</sub> measurement : Set ENABLE low.

V<sub>OLF</sub> measurement : Set SW4 'on' in the I<sub>oave</sub> measurement condition.

## Sample Application Circuit

(2W1-2 Phase Excitation Drive /micro stepping operation)



## Precautions

[GND wiring]

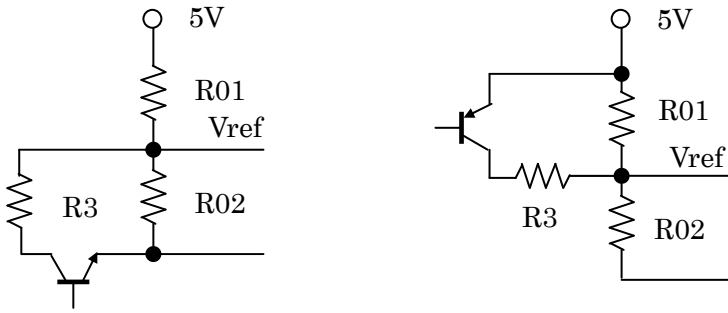
- To reduce noise on the 5V/24V system, be sure to place the GND of C01 in the circuit given above as close as possible to Pin 2 and Pin 6 of the hybrid IC.  
In addition, in order to set the current accurately, the GND side of RO2 of Vref must be connected to the shared ground terminal used by the Pin 18 (S.G) GND, P.G1 and P.G2.

[Input pins]

- If VDD is being applied, use care that each input pin does not apply a negative voltage less than -0.3V to S. GND, Pin 18. Measures must also be taken so that a voltage equal to or greater than VDD is not input.
- High voltage input other than VDD, MOI, FAULT1, and FAULT2 is 2.5V.
- Pull-up resistors are not connected to input pins. Pull-down resistors are attached. When controlling the input to the hybrid IC with the open collector type, be sure to connect a pull-up resistor (1 to 20kΩ).  
Be sure to use a device (0.8V or less, low level, when I<sub>OL</sub>=5mA) for the open collector driver at this time that has an output voltage specification such that voltage is pulled to less than 0.8V at low level.
- When using the power on reset function built into the hybrid IC, be sure to directly connect Pin 14 to VDD.
- We recommend attaching a 1,000pF capacitor to each input to prevent malfunction during high-impedance input. Be sure to connect the capacitor near the hybrid IC, between Pin 18 (S, G).  
When input is fixed low, directly connect to Pin 18. When input is fixed high, directly connect to VDD.

[Current setting Vref]

If the motor current is temporarily reduced, the circuit given below is recommended.  
The variable voltage range of Vref input is 0.2 to 1.8V.



[Setting the motor current]

The motor current,  $I_{OH}$ , is set using the Pin 19 voltage,  $V_{ref}$ , of the hybrid IC.

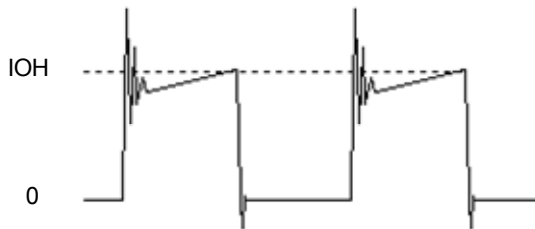
Equations related to  $I_{OH}$  and  $V_{ref}$  are given below.

$$V_{ref} \approx (R02 \div (R02+R01)) \times V_{DD}(5V) \dots\dots\dots (1)$$

$$I_{OH} \approx (V_{ref} \div 4.9) \div R_s \dots\dots\dots (2)$$

The value of 4.9 in Equation (2) above represents the  $V_{ref}$  voltage as divided by a circuit inside the control IC.

$R_s$ : 0.122Ω (Current detection resistor inside the hybrid IC)



[Smoke Emission Precautions]

If Pin 18 (S.G terminal) is attached to the board without using solder, overcurrent may flow into the MOSFET at  $V_{CCON}$  (24V ON), causing the STK672-440B-E to emit smoke because 5V circuits cannot be controlled.

**Function Table**

M2	0	0	1	1	CLOCK Edge Timing for Phase Switching	
M1	0	1	0	1		
M3	1	2-phase excitation selection	1-2-phase excitation ( $I_{OH}=100\%$ )	W1-2 phase excitation	2W1-2 phase excitation	CLOCK rising edge
	0	1-2 phase excitation ( $I_{OH}=100\%$ , 71%)	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	CLOCK both edges

$I_{OH}=100\%$  results in the  $V_{ref}$  voltage setting,  $I_{OH}$ .

During 1-2 phase excitation, the hybrid IC operates at a current setting of  $I_{OH}=100\%$  when the CLOCK signal rises. Conversely, pseudo micro current control is performed to control current at  $I_{OH}=100\%$  or 71% at both edges of the CLOCK signal.

**WB pin**

Forward/CW	0
Reverse/CCW	1

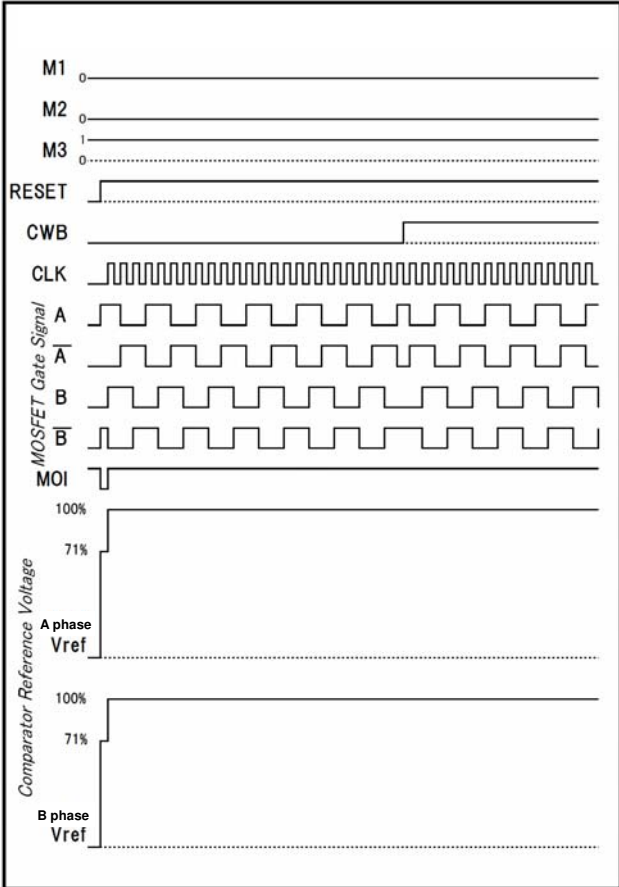
**ENABLE • RESETB pin**

ENABLE	Motor current cut: Low
RESETB	Active Low

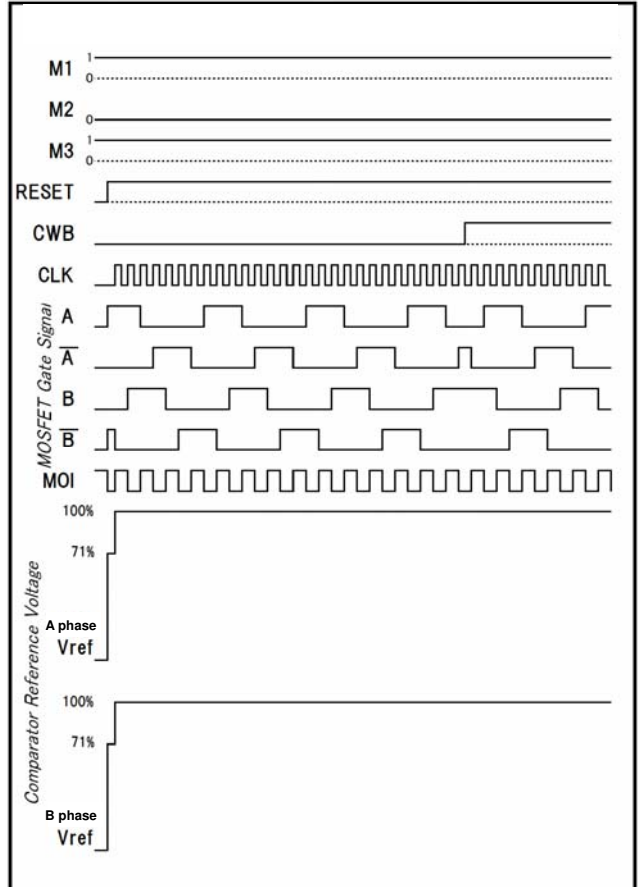


Timing Charts

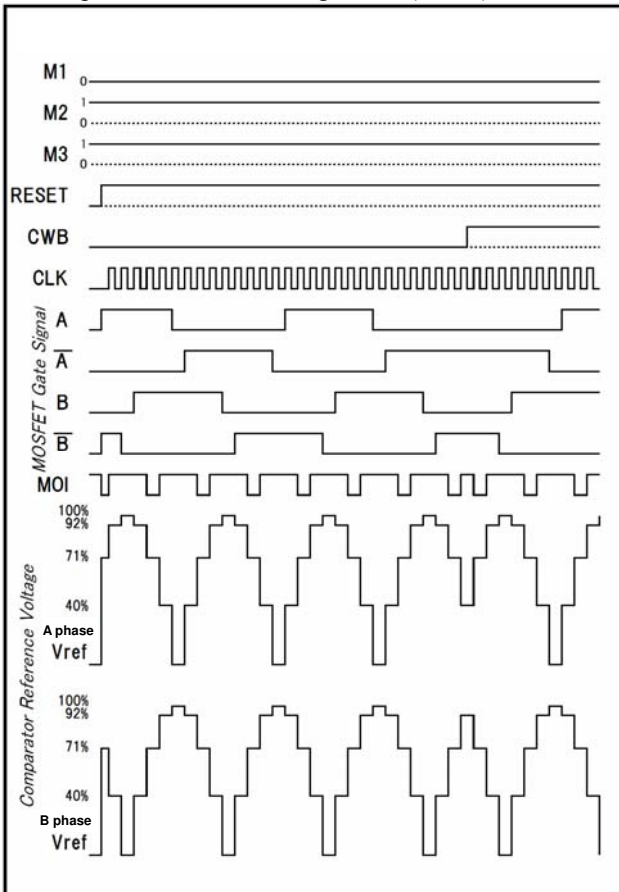
2-phase excitation timing charts (M3=1)



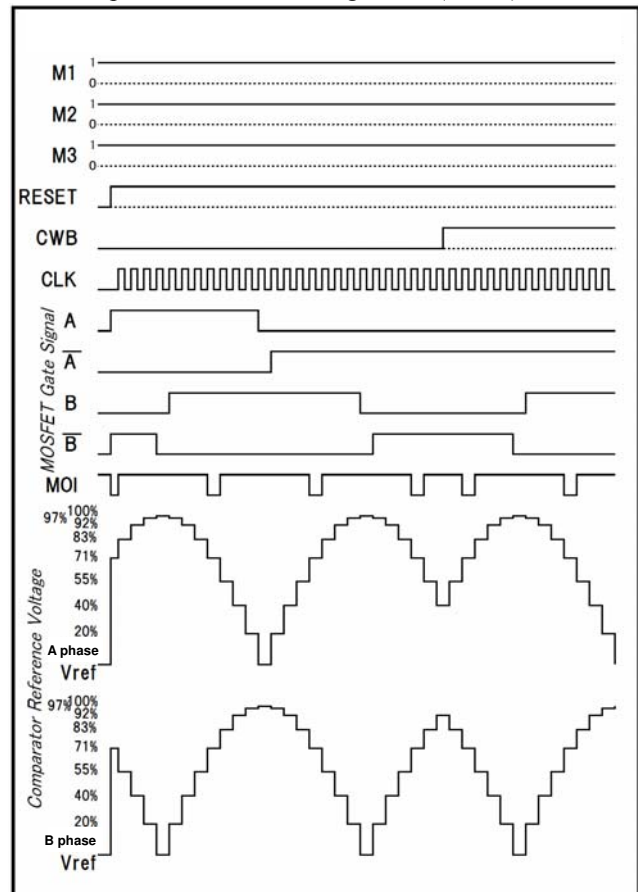
1-2-phase excitation timing charts (M3=1)



W1-2-phase excitation timing charts (M3=1)

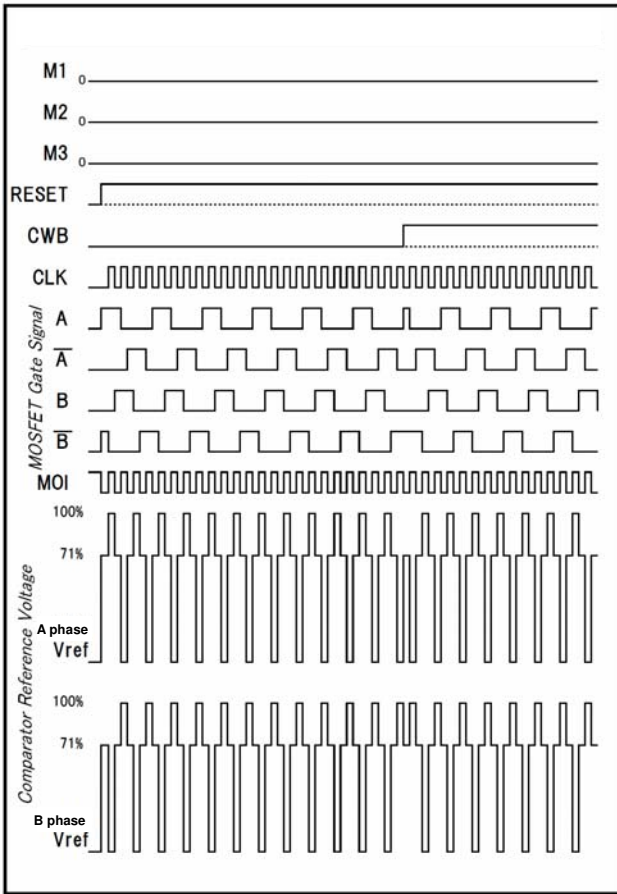


2W1-2-phase excitation timing charts (M3=1)

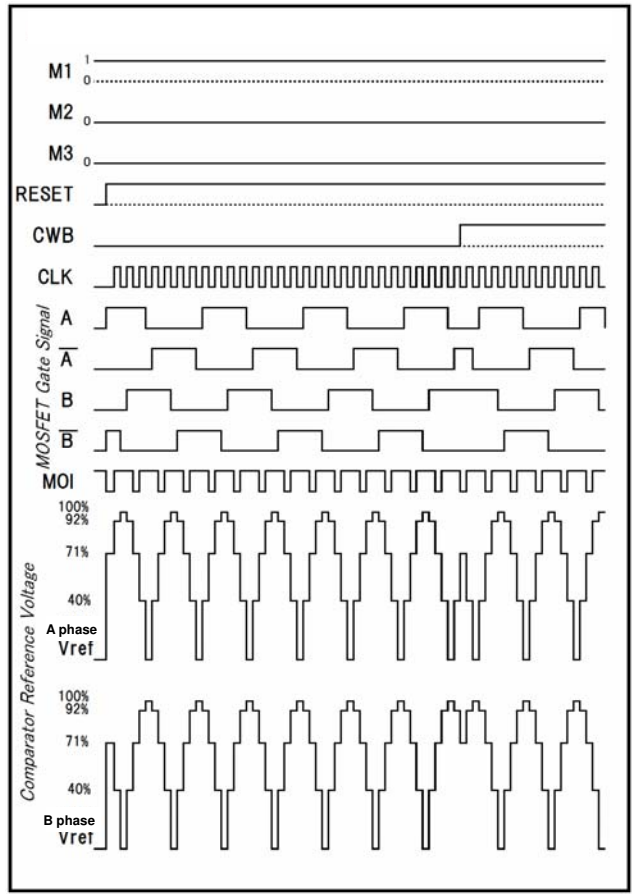


# STK672-440BN-E

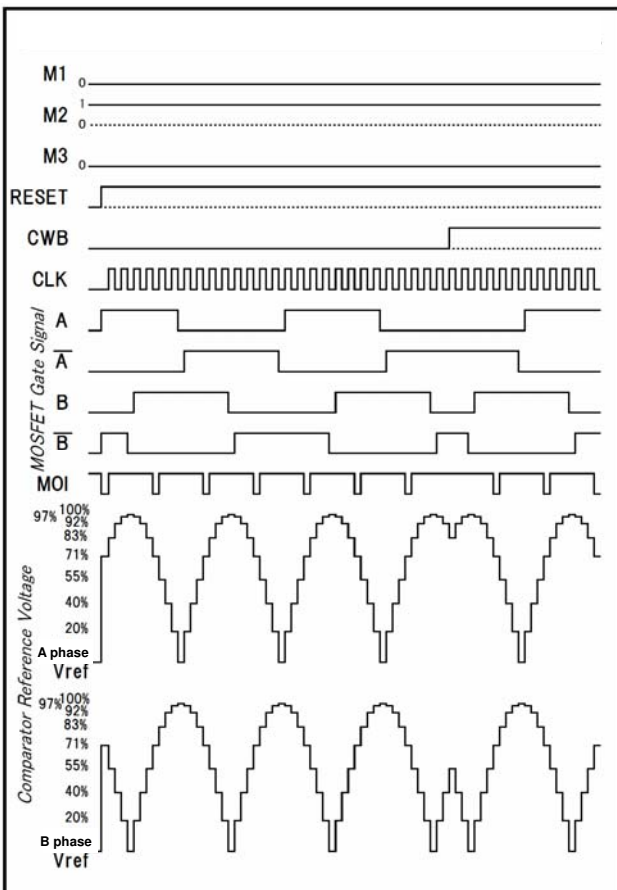
1-2-phase excitation timing charts (M3=0)



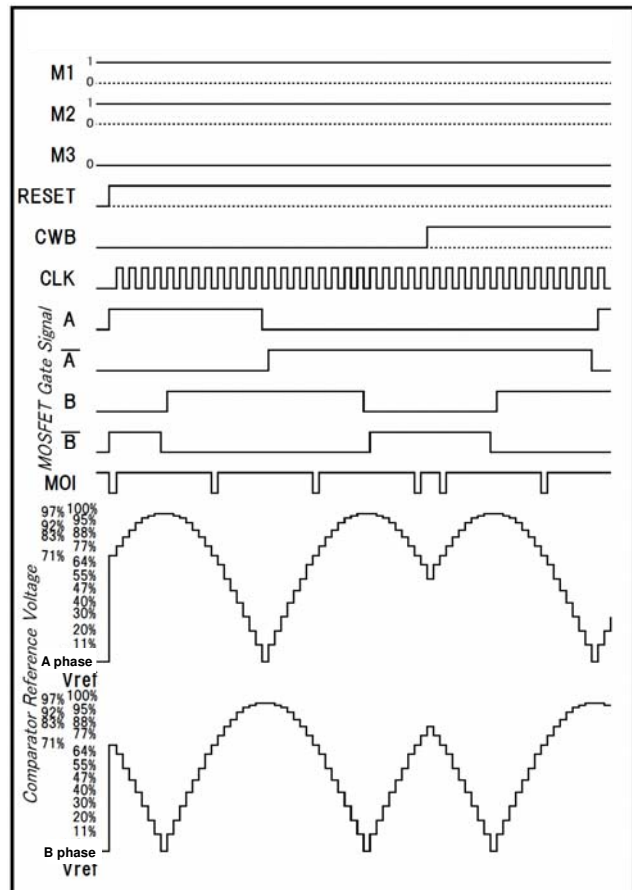
W1-2-phase excitation timing charts (M3=0)



2W1-2-phase excitation timing charts (M3=0)



4W1-2-phase excitation timing charts (M3=0)



# STK672-440BN-E

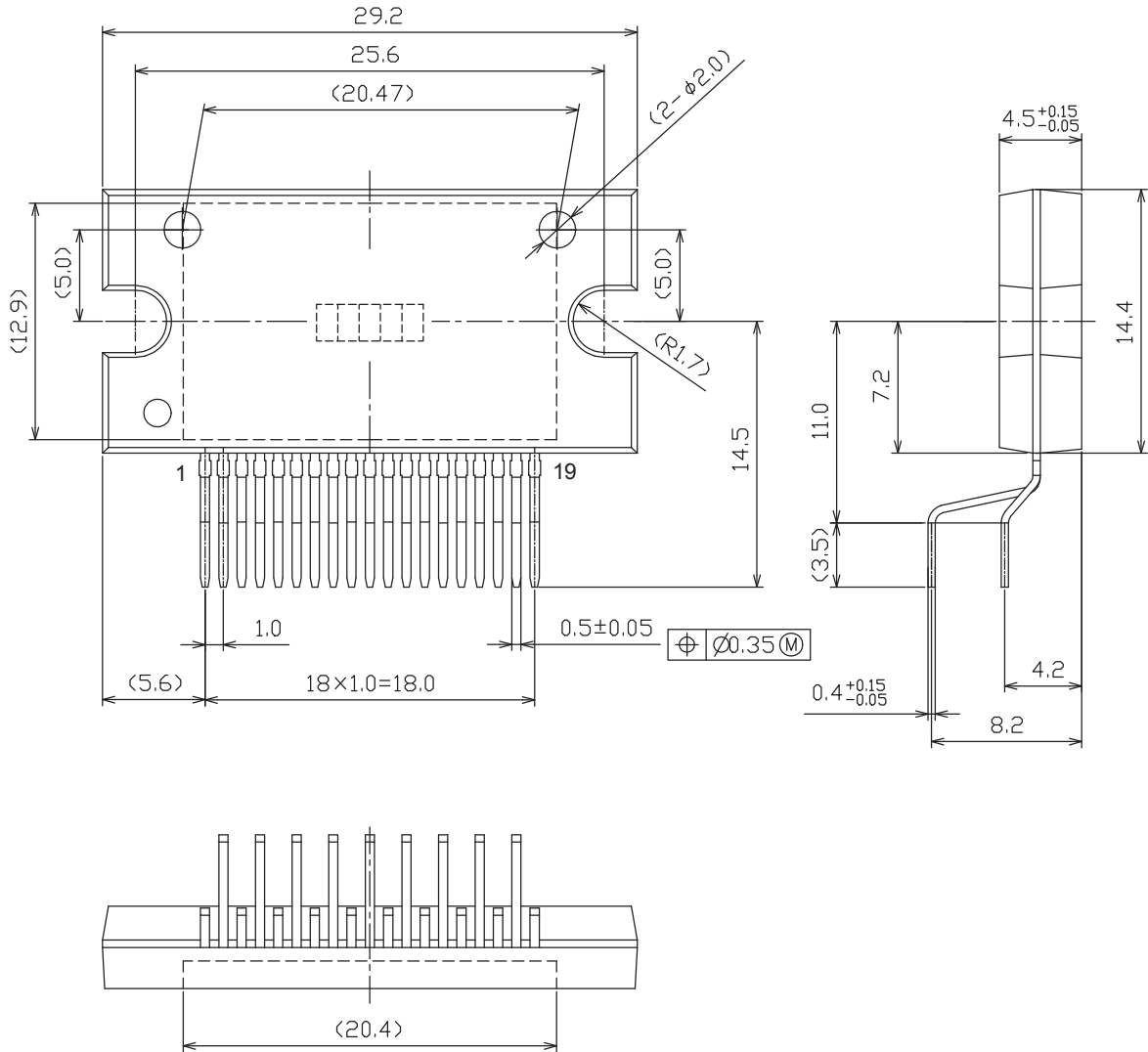
## Package Dimensions

unit : mm

SIP19 29.2x14.4

CASE 127CF

ISSUE 0



STK672-440BN-E  
**Technical data**

1. Input Pins and Functional Overview
2. STK672-440BN-E output pins open detection, over current detection, thermal shutdown detection.
3. STK672-440BN-E Allowable Avalanche Energy
4. STK672-440BN-E Internal Loss Calculation
5. Thermal Design
6. Package Power Loss PdPK Derating Curve for the Ambient Temperature Ta
7. Other usage notes

# STK672-440BN-E

## 1.I/O Pins and Functions of the Control Block

[Pin description]

HIC pin	Pin Name	Function
7	MOI	Output pin for the excitation monitor
19	Vref	Current value setting
10	MODE1	Excitation mode selection
11	MODE2	
17	MODE3	
12	CLOCK	External CLOCK (motor rotation instruction)
13	CWB	Sets the direction of rotation of the motor axis
14	RESETB	System reset
15	ENABLE	Motor current OFF
16	FAULT1	Motor terminal open/Overcurrent/over-heat detection output
8	FAULT2	

### Description of each pin

#### 1-1.[CLOCK (Phase switching clock)]

Input frequency: DC-20kHz (when using both edges) or DC-50kHz (when using one edge)

Minimum pulse width: 20 $\mu$ s (when using both edges) or 10 $\mu$ s (when using one edge)

Pulse width duty: 40% to 50% (when using both edges)

Both edge, single edge operation

M3:1 The excitation phase moves one step at a time at the rising edge of the CLOCK pulse.

M3:0 The excitation phase moves alternately one step at a time at the rising and falling edges of the CLOCK pulse.

#### 1-2.[CWB (Motor direction setting)]

When CWB=0: The motor rotates in the clockwise direction.

When CWB=1: The motor rotates in the counterclockwise direction.

Do not allow CWB input to vary during the 7 $\mu$ s interval before and after the rising and falling edges of CLOCK input.

#### 1-3. [ENABLE (Forcible OFF control of excitation drive output A, AB, B, and BB, and selecting operation/hold status inside the HIC)]

ENABLE=1: Normal operation

When ENABLE=0: Motor current goes OFF, and excitation drive output is forcibly turned OFF.

The system clock inside the HIC stops at this time, with no effect on the HIC even if input pins other than RESET input vary. In addition, since current does not flow to the motor, the motor shaft becomes free.

If the CLOCK signal used for motor rotation suddenly stops, the motor shaft may advance beyond the control position due to inertia. A SLOW DOWN setting where the CLOCK cycle gradually decreases is required in order to stop at the control position.

#### 1-4. [MODE1, MODE2, and MODE3 (Selecting the excitation mode, and selecting one edge or both edges of the CLOCK)]

Excitation select mode terminal (See the sample application circuit for excitation mode selection), selecting the CLOCK input edge(s).

Mode setting active timing

Do not change the mode within 7 $\mu$ s of the input rising or falling edge of the CLOCK signal.

#### 1-5.[RESETB (System-wide reset)]

The reset signal is formed by the power-on reset function built into the HIC and the RESETB terminal.

When activating the internal circuits of the HIC using the power-on reset signal within the HIC, be sure to connect Pin 14 of the HIC to VDD.

#### 1-6.[Vref (Voltage setting to be used for the current setting reference)]

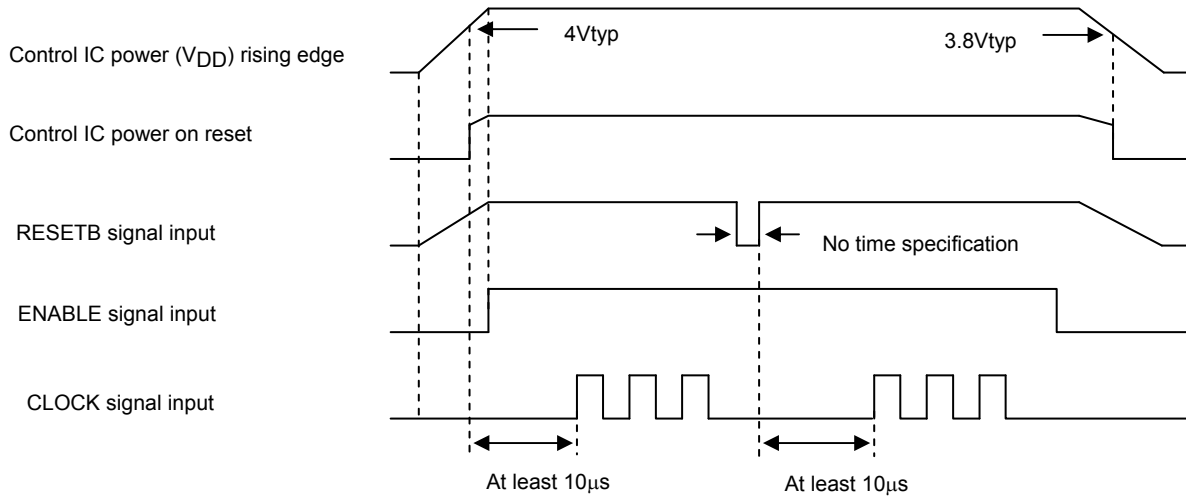
Pin type: Analog input configuration

Input voltage is in the voltage range of 0.2V to 1.8V.

## 1-7. [Input timing]

The control IC of the driver is equipped with a power on reset function capable of initializing internal IC operations when power is supplied. A 4V typ setting is used for power on reset. Because the specification for the MOSFET gate voltage is  $5V \pm 5\%$ , conduction of current to output at the time of power on reset adds electromotive stress to the MOSFET due to lack of gate voltage. To prevent electromotive stress, be sure to set ENABLE=Low while  $V_{DD}$ , which is outside the operating supply voltage, is less than 4.75V.

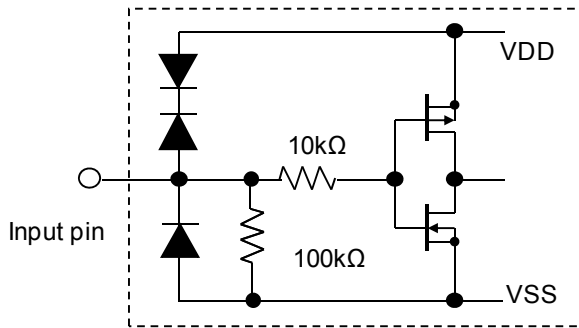
In addition, if the RESETB terminal is used to initialize output timing, be sure to allow at least  $10\mu s$  until CLOCK input.



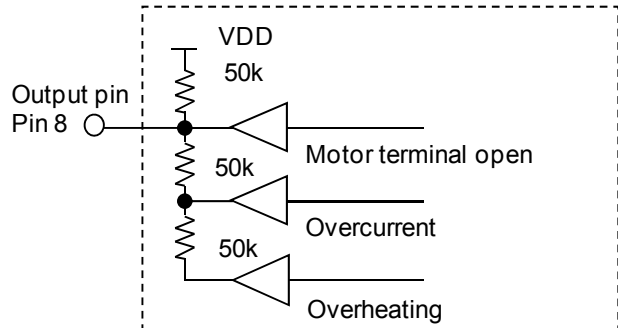
ENABLE, CLOCK, and RESETB Signals Input Timing

## 1-8. [Configuration of control block I/O pins]

<Configuration of the MODE1, MODE2, MODE3, CLOCK, CWB, ENABLE, and RESETB input pins>

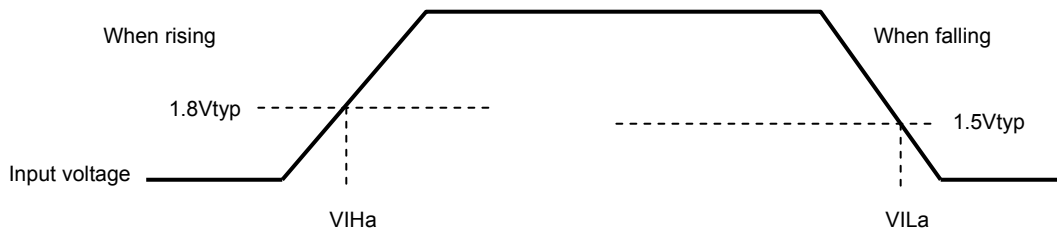


<Configuration of the FAULT2 pin>



(The buffer has an open drain configuration.)

The input pins of this driver all use Schmitt input. Typical specifications at  $T_c=25^\circ C$  are given below. Hysteresis voltage is 0.3V ( $V_{IHa}-V_{ILa}$ ).

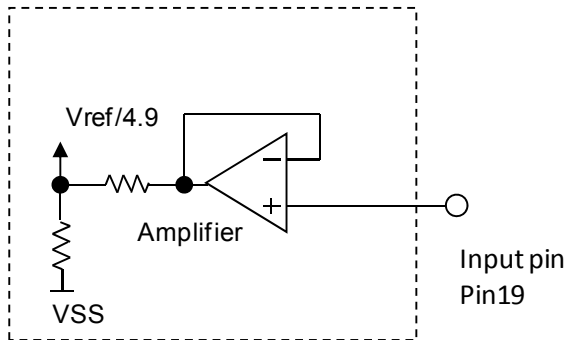


Input voltage specifications are as follows.

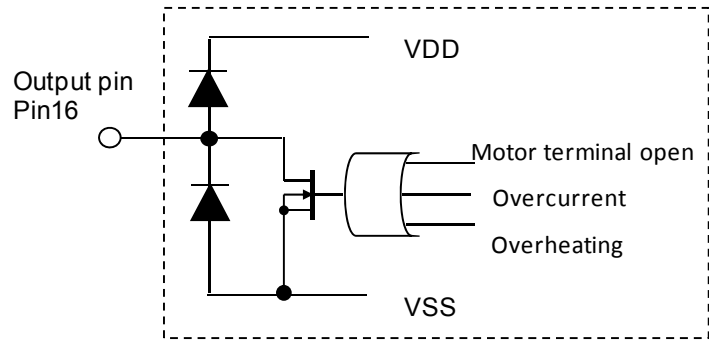
$$V_{IH} = 2.5V_{min}$$

$$V_{IL} = 0.8V_{max}$$

## <Configuration of the Vref input pin>



## <Configuration of the FAULT1 output pin>



## <FAULT1, FAULT2 output>

### FAULT1 Output

FAULT1 is an open drain output. It outputs low level when any of motor terminal open, overcurrent, or overheat is detected.

### FAULT2 output

Output is resistance divided (3 levels) and the type of abnormality detected is converted to the corresponding output voltage.

- Motor terminal open: 10mV (typ)
- Overcurrent: 2.5V (typ)
- Overheat: 3.3V (typ)

Abnormality detection can be released by a RESETB operation or turning V<sub>DD</sub> voltage on/off.

## 1-9. [MOI output]

The output frequency of this excitation monitor pin varies depending on the excitation mode. For output operations, see the timing chart.

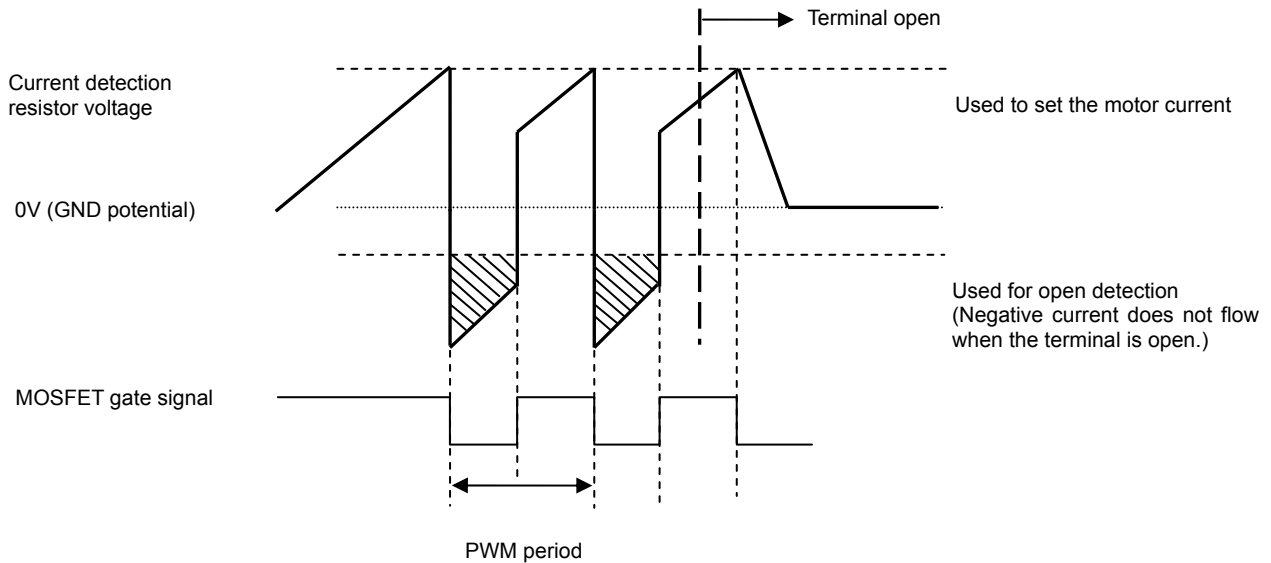
2. Overcurrent detection, overheat detection, and motor terminal open detection functions

Each detection function operates using a latch system and turns output off. Because a RESET signal is required to restore output operations, once the power supply, VDD, is turned off, you must either again apply power on reset with VDDON or apply a RESETB=High→Low→High signal.

2-1. [Motor terminal open detection]

This hybrid IC is equipped with a function for detecting open output terminals to prevent thermal destruction of the MOSFET due to repeated avalanche operation that occurs when an output terminal connected to the motor is open. The open condition is determined by checking the presence or absence of the flyback current that flows in the motor inductance during the off period of the PWM cycle.

Detection is performed by using the fact that the flyback current does not flow when a motor terminal is open.



When the current level drops, the difference with the GND potential decreases, making detection difficult. The motor current that can be detected by motor terminal open detection is 1.1A or more with the STK672-432BN-E and 1.4A or more with the STK672-440BN-E/442BN-E.

<Notes on the ENABLE high edge>

When ENABLE changes from low to high and the STK672-4xxBN-E performs constant-current PWM operation that flows a negative current during the 30μs period after the high edge, open detection may activate and stop the driver. The motor current setting voltage Vref must be set so that PWM operation is not performed within a period of 30μs after the high edge.

If the motor current setup voltage is set for the rated motor current, PWM operation is not performed during this 30μs period after the high edge, so this is not a problem.

In addition, there is no problem with operation that lowers the current setting Vref after the motor rated current is reached as shown in the diagram on the following page.

Whether constant-current PWM operation is performed during the 30μs period after the high edge can be judged by substituting the motor L and R values into the formula on the following page.

$$V_{ref} = (R02 \div (R01 + R02)) \times VDD$$

$$I_{OH1} = (V_{ref} \div 4.9) \div R_s$$

I<sub>OH1</sub>: Motor current value to be set

$$I_{OH2} = (VCC \div R) \times (1 - e^{-tR/L})$$

I<sub>OH2</sub>: Current value 30μs after the ENABLE high edge

⇒ Judgment standard: I<sub>OH1</sub> > I<sub>OH2</sub>

R01, R02, VDD : See the Sample Application Circuit documents.

R<sub>s</sub>: Current detection resistance value (Ω)

V<sub>CC</sub>: Motor supply voltage (V)

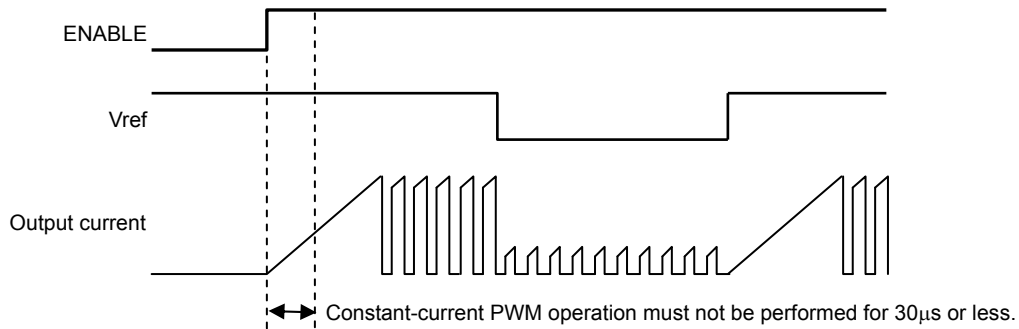
R: Motor winding resistance (Ω)

L: Motor winding inductance (H)

⇒ There is no problem if the I<sub>OH2</sub> obtained by substituting t = 30μs and the motor L and R values is smaller than the current setting value I<sub>OH1</sub>.



# STK672-440BN-E



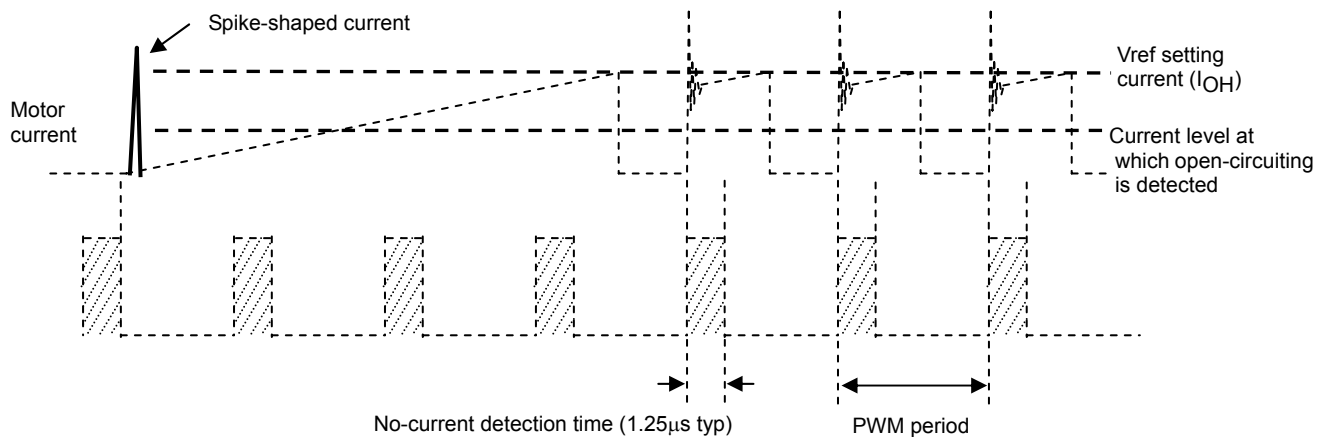
## <Connection of capacitors between output pins and GND prohibited>

Capacitors must not be connected between the phase A (pin 4), phase AB (pin 5), phase B (pin 3) and phase BB (pin 1) outputs and GND. What happens if capacitors are connected is that open-circuit detection may be triggered by the discharge current of the capacitors when the internal MOSFET is set ON. This current is not an inductance current generated by the motor winding but a capacitor current so a negative current will not flow to the other phase in each pair of phases, possibly causing the driver to shut down.

## <Excessive external noise>

If, when the motor current rises prior to the PWM operation, a spike-shaped current exceeding the Vref-setting current is generated by excessive external noise, for instance, before the current level (1.1A for the STK672-432BN-E, 1.4A for the STK672-440BN-E and 442BN-E motor drivers) at which motor pin open-circuiting can be detected is reached, the internal MOSFET is set OFF. Since the MOSFET has been set OFF before the actual motor current reaches 1.1A (or 1.4A), the level of the negative current subsequently flowing to the other phase in each pair of phases is low, and it may be judged that no negative current is flowing, possibly causing open-circuit detection to be triggered.

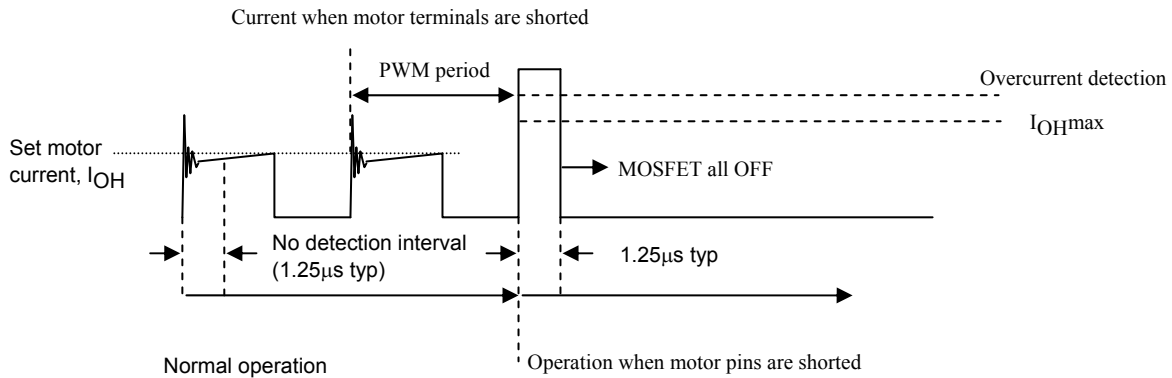
During normal constant-current PWM operation, the duration of 1.25µs, which is equivalent to 6% of the initial operation in the PWM period, corresponds to the section where the current is not detected, and this ensures that no current is detected for the linking part of the current that is generated in this section. The no-current detection section is not synchronized at the current rise prior to the PWM operation so when a spike-shaped current exceeding the Vref-setting current is generated, the MOSFET is set OFF at the stage where the level of the actual motor current is low. As a result, the level of the negative current subsequently flowing to the other phase in each pair of phases is low, and it may be judged that no negative current is flowing, possibly causing open-circuit detection to be triggered.



## 2-2. [Overcurrent detection]

This hybrid IC is equipped with a function for detecting overcurrent that arises when the motor burns out or when there is a short between the motor terminals.

Overcurrent detection occurs at 3.4A typ with the STK672-432BN-E, and 5.0A typ with the STK672-440BN-E/442BN-E.



Overcurrent detection begins after an interval of no detection (a dead time of 1.25 $\mu$ s typ) during the initial ringing part during PWM operations. The no detection interval is a period of time where overcurrent is not detected even if the current exceeds  $I_{OH}$ .

## 2-3. [Overheat detection]

Rather than directly detecting the temperature of the semiconductor device, overheat detection detects the temperature of the aluminum substrate (144 $^{\circ}$ C typ).

Within the allowed operating range recommended in the specification manual, if a heat sink attached for the purpose of reducing the operating substrate temperature,  $T_c$ , comes loose, the semiconductor can operate without breaking.

However, we cannot guarantee operations without breaking in the case of operations other than those recommended, such as operations at a current exceeding  $I_{OHmax}$  that occurs before overcurrent detection is activated.

3. Allowable Avalanche Energy Value

(1) Allowable Range in Avalanche Mode

When driving a 2-phase stepping motor with constant current chopping using an STK672-4\*\* Series hybrid IC, the waveforms shown in Figure 1 below result for the output current,  $I_D$ , and voltage,  $V_{DS}$ .

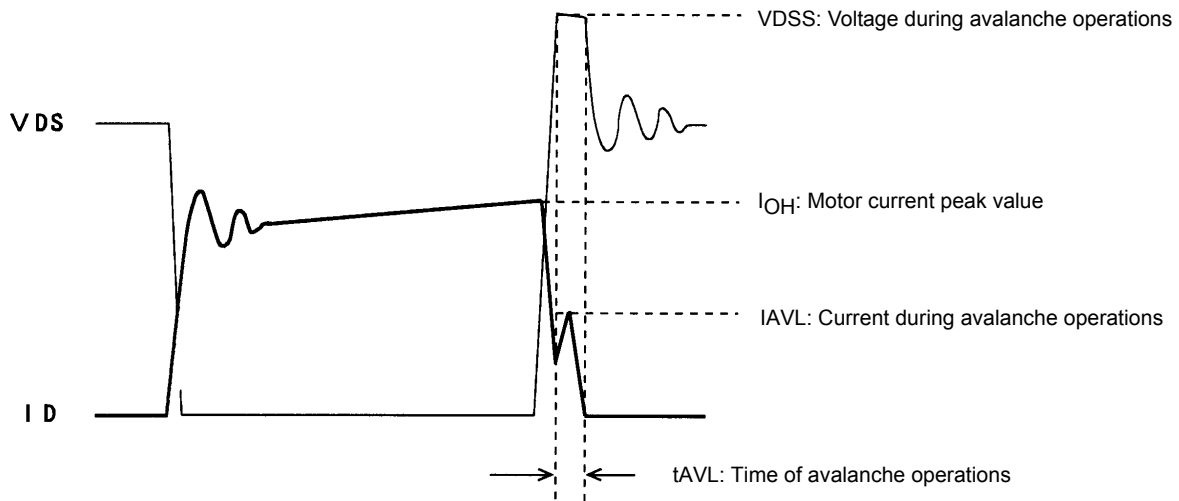


Figure 1 Output Current,  $I_D$ , and Voltage,  $V_{DS}$ , Waveforms 1 of the STK672-4\*\* Series when Driving a 2-Phase Stepper Motor with Constant Current Chopping

When operations of the MOSFET built into STK672-4\*\* Series ICs is turned off for constant current chopping, the  $I_D$  signal falls like the waveform shown in the figure above. At this time, the output voltage,  $V_{DS}$ , suddenly rises due to electromagnetic induction generated by the motor coil.

In the case of voltage that rises suddenly, voltage is restricted by the MOSFET  $V_{DSS}$ . Voltage restriction by  $V_{DSS}$  results in a MOSFET avalanche. During avalanche operations,  $I_D$  flows and the instantaneous energy at this time,  $E_{AVL1}$ , is represented by Equation (3-1).

$$E_{AVL1} = V_{DSS} \times I_{AVL} \times 0.5 \times t_{AVL} \text{ ----- (3-1)}$$

$V_{DSS}$ : V units,  $I_{AVL}$ : A units,  $t_{AVL}$ : sec units

The coefficient 0.5 in Equation (3-1) is a constant required to convert the  $I_{AVL}$  triangle wave to a square wave.

During STK672-4\*\* Series operations, the waveforms in the figure above repeat due to the constant current chopping operation. The allowable avalanche energy,  $E_{AVL}$ , is therefore represented by Equation (3-2) used to find the average power loss,  $P_{AVL}$ , during avalanche mode multiplied by the chopping frequency in Equation (3-1).

$$P_{AVL} = V_{DSS} \times I_{AVL} \times 0.5 \times t_{AVL} \times f_c \text{ ----- (3-2)}$$

$f_c$ : Hz units ( $f_c$  is set to the PWM frequency of 50kHz.)

For  $V_{DSS}$ ,  $I_{AVL}$ , and  $t_{AVL}$ , be sure to actually operate the STK672-4\*\* Series and substitute values when operations are observed using an oscilloscope.

Ex. If  $V_{DSS}=110V$ ,  $I_{AVL}=1A$ ,  $t_{AVL}=0.2\mu s$ , the result is:  
 $P_{AVL}=110 \times 1 \times 0.5 \times 0.2 \times 10^{-6} \times 50 \times 10^3 = 0.55W$   
 $V_{DSS}=110V$  is a value actually measured using an oscilloscope.

The allowable loss range for the allowable avalanche energy value,  $P_{AVL}$ , is shown in the graph in Figure 3. When examining the avalanche energy, be sure to actually drive a motor and observe the  $I_D$ ,  $V_{DSS}$ , and  $t_{AVL}$  waveforms during operation, and then check that the result of calculating Equation (3-2) falls within the allowable range for avalanche operations.

(2)  $I_D$  and  $V_{DS}$  Operating Waveforms in Non-avalanche Mode

Although the waveforms during avalanche mode are given in Figure 1, sometimes an avalanche does not result during actual operations.

Factors causing avalanche are listed below.

- Poor coupling of the motor's phase coils (electromagnetic coupling of A phase and AB phase, B phase and BB phase).
- Increase in the lead inductance of the harness caused by the circuit pattern of the board and motor.
- Increases in  $V_{DS}$ ,  $t_{AVL}$ , and  $I_{AVL}$  in Figure 1 due to an increase in the supply voltage from 24V to 36V.

If the factors above are negligible, the waveforms shown in Figure 1 become waveforms without avalanche as shown in Figure 2.

Under operations shown in Figure 2, avalanche does not occur and there is no need to consider the allowable loss range of  $PAVL$  shown in Figure 3.

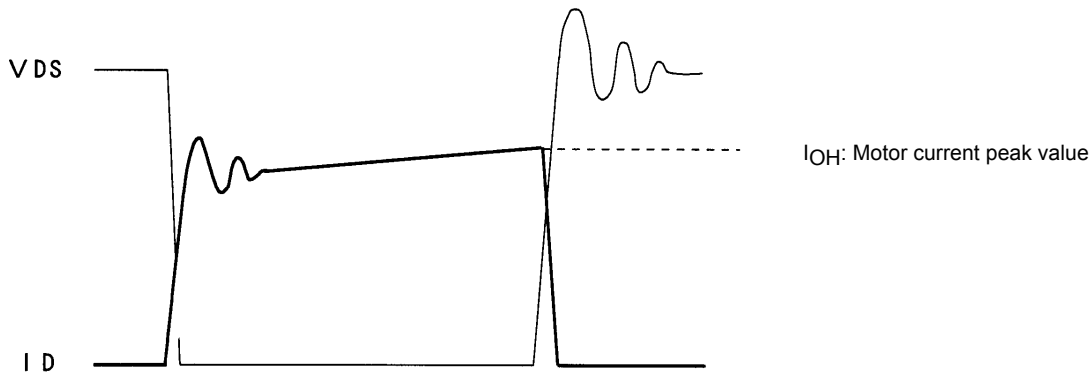
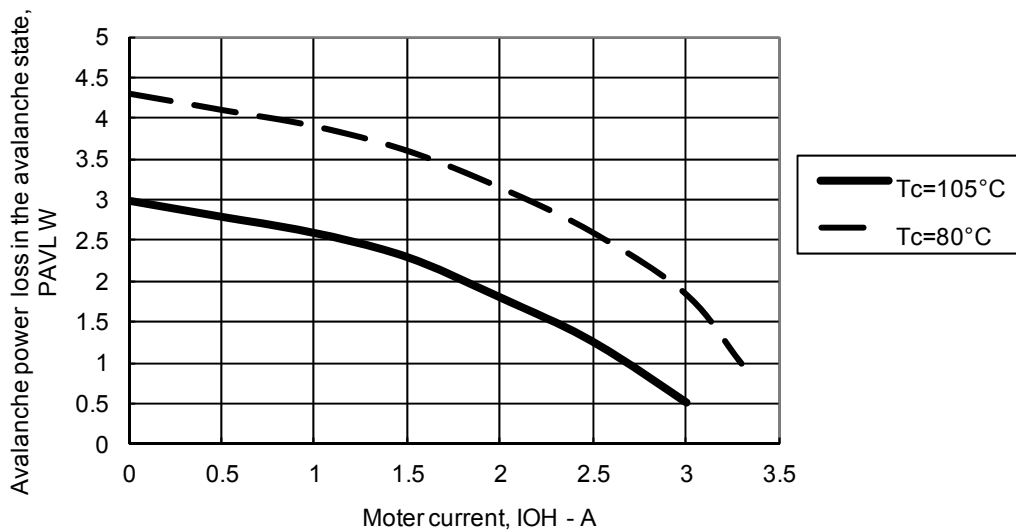


Figure 2 Output Current,  $I_D$ , and Voltage,  $V_{DS}$ , Waveforms 2 of the STK672-4\*\* Series when Driving a 2-Phase Stepper Motor with Constant Current Chopping

Figure 3 Allowable Loss Range,  $PAVL-I_{OH}$  During STK672-440BN-E Avalanche Operations  
 $PAVL-I_{OH}$



Note:

The operating conditions given above represent a loss when driving a 2-phase stepper motor with constant current chopping.

Because it is possible to apply 3W or more at  $I_{OH}=0A$ , be sure to avoid using the MOSFET body diode that is used to drive the motor as a zener diode.

**4. Calculating STK672-440BN-E HIC Internal Power Loss**

The average internal power loss in each excitation mode of the STK672-440B-E can be calculated from the following formulas. \*1

4-1. [Each excitation mode]

2-phase excitation mode

$$2PdAVex = 2 \times V_{sat} \times 0.5 \times CLOCK \times I_{OH} \times t_2 + 0.5 \times CLOCK \times I_{OH} \times (V_{sat} \times t_1 + V_{df} \times t_3) \text{ ----- (4-1)}$$

1-2 Phase excitation mode

$$1-2PdAVex = 2 \times V_{sat} \times 0.25 \times CLOCK \times I_{OH} \times t_2 + 0.25 \times CLOCK \times I_{OH} \times (V_{sat} \times t_1 + V_{df} \times t_3) \text{ ----- (4-2)}$$

W1-2 Phase excitation mode

$$W1-2PdAVex = 0.64 [2 \times V_{sat} \times 0.125 \times CLOCK \times I_{OH} \times t_2 + 0.125 \times CLOCK \times I_{OH} \times (V_{sat} \times t_1 + V_{df} \times t_3)] \text{ ----- (4-3)}$$

2W1-2 Phase excitation mode

$$2W1-2PdAVex = 0.64 [2 \times V_{sat} \times 0.0625 \times CLOCK \times I_{OH} \times t_2 + 0.0625 \times CLOCK \times I_{OH} \times (V_{sat} \times t_1 + V_{df} \times t_3)] \text{ ----- (4-4)}$$

4W1-2 Phase excitation mode

$$4W1-2PdAVex = 0.64 [2 \times V_{sat} \times 0.0625 \times CLOCK \times I_{OH} \times t_2 + 0.0625 \times CLOCK \times I_{OH} \times (V_{sat} \times t_1 + V_{df} \times t_3)] \text{ ----- (4-5)}$$

Motor hold mode

$$HoldPdAVex = 2 \times V_{sat} \times I_{OH} \text{ ----- (4-6)}$$

Note: 2-phase 100% conductance is assumed in Equation (4-6).

V<sub>sat</sub>: Combined voltage of Ron voltage drop + current detection resistance

V<sub>df</sub>: Combined voltage of the FET body diode + current detection resistance

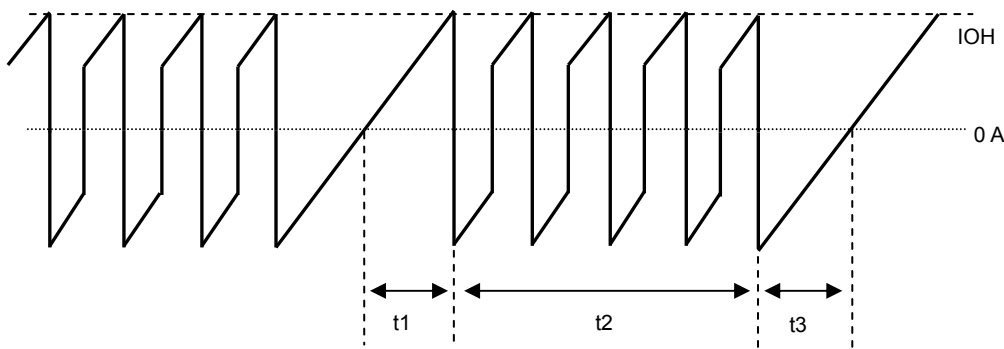
CLOCK: Input CLOCK (HIC: input frequency at Pin 12)

t<sub>1</sub>, t<sub>2</sub>, and t<sub>3</sub> represent the waveforms shown in the figure below.

t<sub>1</sub>: Time required for the winding current to reach the set current (I<sub>OH</sub>)

t<sub>2</sub>: Time in the constant current control (PWM) region

t<sub>3</sub>: Time from end of phase input signal until inverse current regeneration is complete



Motor COM Current Waveform Model

$$t_1 = (-L / (R + 0.25)) \ln (1 - ((R + 0.25) / V_{CC}) \times I_{OH}) \text{ ----- (4-7)}$$

$$t_3 = (-L / R) \ln ((V_{CC} + 0.25) / (I_{OH} \times R + V_{CC} + 0.25)) \text{ ----- (4-8)}$$

V<sub>CC</sub>: Motor supply voltage (V)

L: Motor inductance (H)

R: Motor winding resistance (Ω)

I<sub>OH</sub>: Motor set output current crest value (A)

## STK672-440BN-E

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Fixed current control time,  $t_2$ , for each excitation mode

- |   |   |
|---|---|
| (1) 2-phase excitation                                  | $t_2 = (2 \div \text{CLOCK}) - (t_1 + t_3)$ ..... (4-9) |
| (2) 1-2 phase excitation                                | $t_2 = (3 \div \text{CLOCK}) - t_1$ ..... (4-10)        |
| (3) W1-2 phase excitation                               | $t_2 = (7 \div \text{CLOCK}) - t_1$ ..... (4-11)        |
| (4) 2W1-2 phase excitation (and 4W1-2 phase excitation) | $t_2 = (15 \div \text{CLOCK}) - t_1$ ..... (4-12)       |

For the values of  $V_{sat}$  and  $V_{df}$ , be sure to substitute from  $V_{sat}$  vs  $I_{OH}$  and  $V_{df}$  vs  $I_{OH}$  at the setting current value  $I_{OH}$ . (See pages to follow)

Then, determine if a heat sink is necessary by comparing with the  $\Delta T_c$  vs  $P_d$  graph (see next page) based on the calculated average output loss, HIC.

For heat sink design, be sure to see '5. Thermal Design'.

The HIC average power,  $P_{dAVex}$  described above, represents loss when not in avalanche mode. To add the loss in avalanche mode, be sure to add PAVL (4-13, 14) using the formula (3-2) for average power loss, PAVL, for STK672-4\*\* avalanche mode, described below to  $P_{dAVex}$  described above.

When using this IC without a fin, always check for temperature increases in the set, because the HIC substrate temperature,  $T_c$ , varies due to effects of convection around the HIC.

### 4-2. [Calculating the average power loss, PAVL, during avalanche mode]

The allowable avalanche energy,  $E_{AVL}$ , during fixed current chopping operation is represented by Equation (3-2) used to find the average power loss, PAVL, during avalanche mode that is calculated by multiplying Equation (3-1) by the chopping frequency.

$$PAVL = V_{DSS} \times I_{AVL} \times 0.5 \times t_{AVL} \times f_c \text{ ..... (3-2)}$$

$f_c$ : Hz units ( $f_c$  is set to the PWM frequency of 50kHz.)

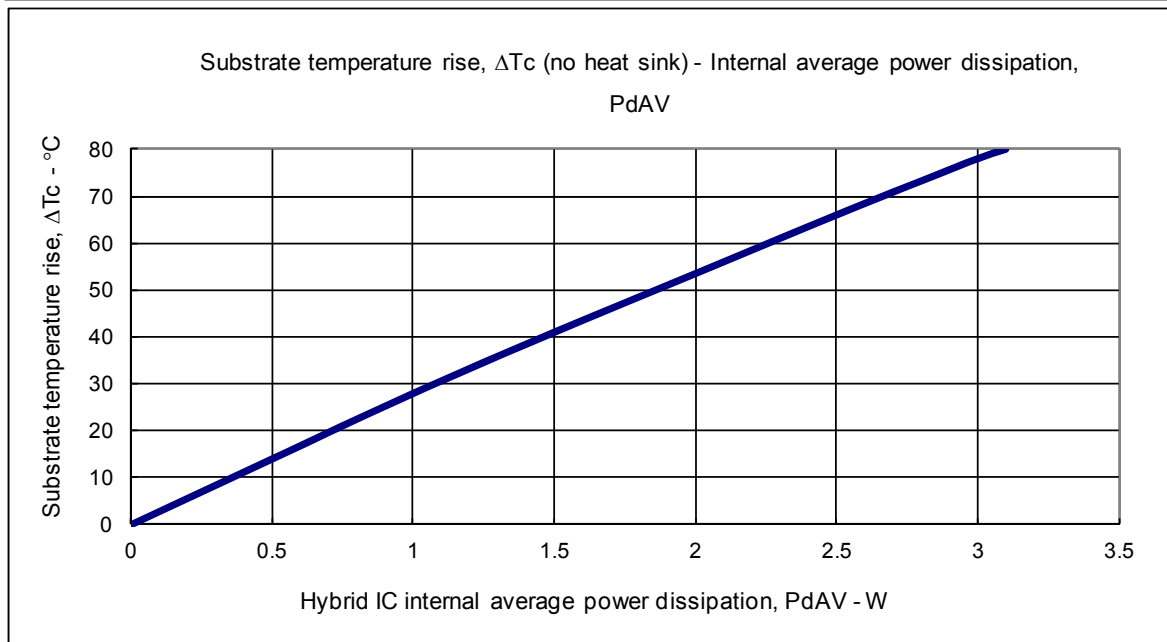
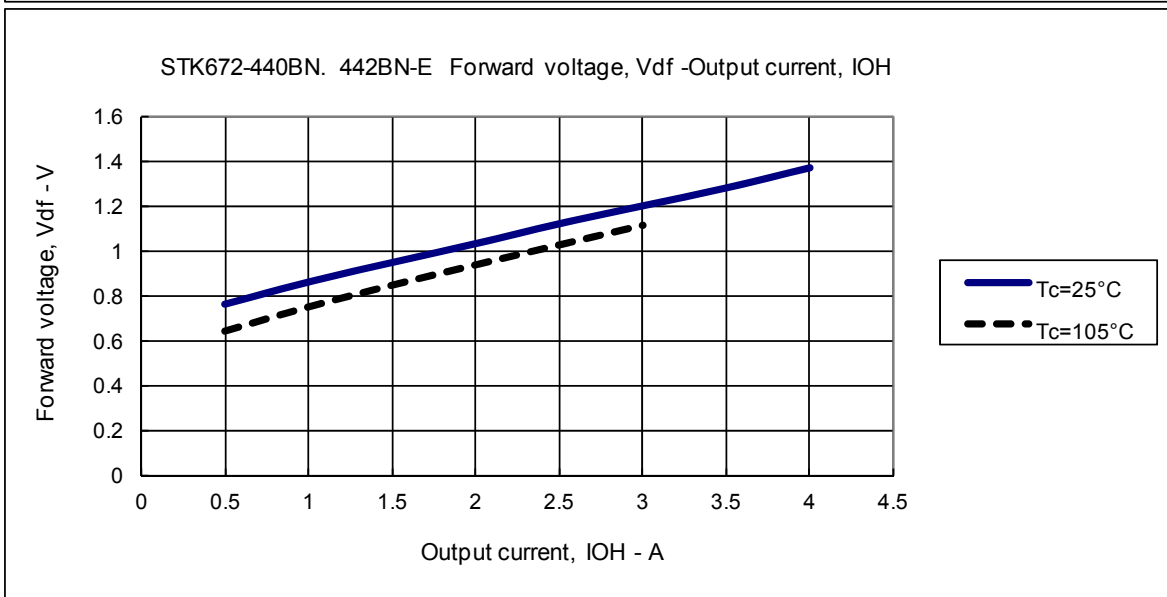
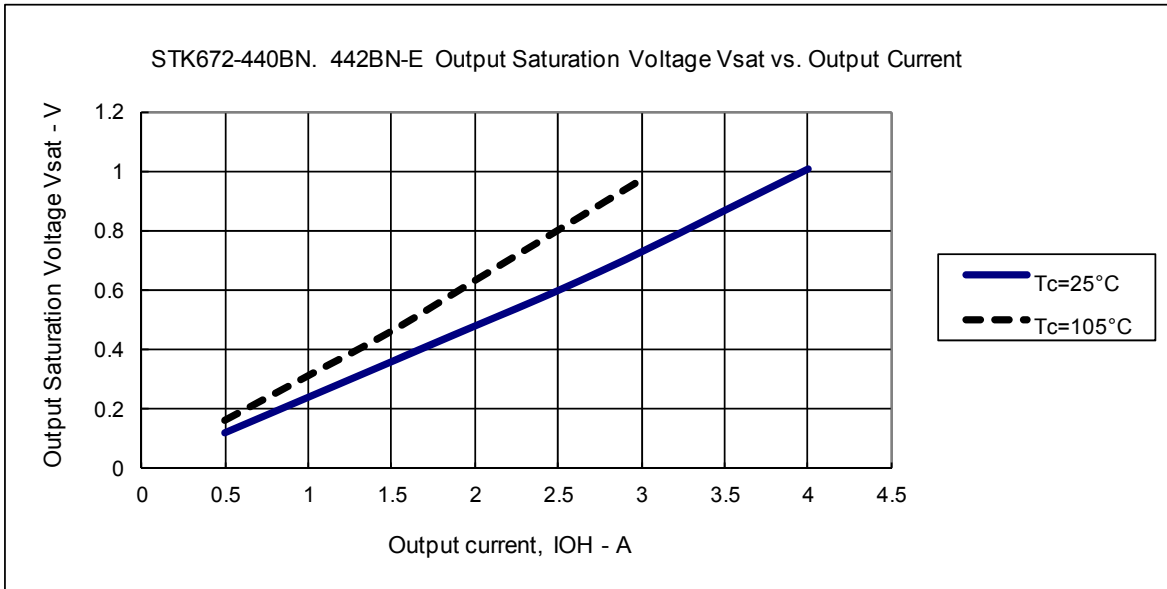
Be sure to actually operate an STK672-4\*\* series and substitute values found when observing operations on an oscilloscope for  $V_{DSS}$ ,  $I_{AVL}$ , and  $t_{AVL}$ .

The sum of PAVL values for each excitation mode is multiplied by the constants given below and added to the average internal HIC loss equation, except in the case of 2-phase excitation.

$$1\text{-}2 \text{ excitation mode and higher: } PAVL(1) = 0.7 \times PAVL \text{ ..... (4-13)}$$

During 2-phase excitation and motor hold:  $PAVL(1) = 1 \times PAVL$  (4-14)

# STK672-440BN-E



5. Thermal design

[Operating range in which a heat sink is not used]

Use of a heat sink to lower the operating substrate temperature of the HIC (Hybrid IC) is effective in increasing the quality of the HIC.

The size of heat sink for the HIC varies depending on the magnitude of the average power loss, PdAV, within the HIC. The value of PdAV increases as the output current increases. To calculate PdAV, refer to “Calculating Internal HIC Loss” in the specification document.

Calculate the internal HIC loss, PdAV, assuming repeat operation such as shown in Figure 1 below, since conduction during motor rotation and off time both exist during actual motor operations,

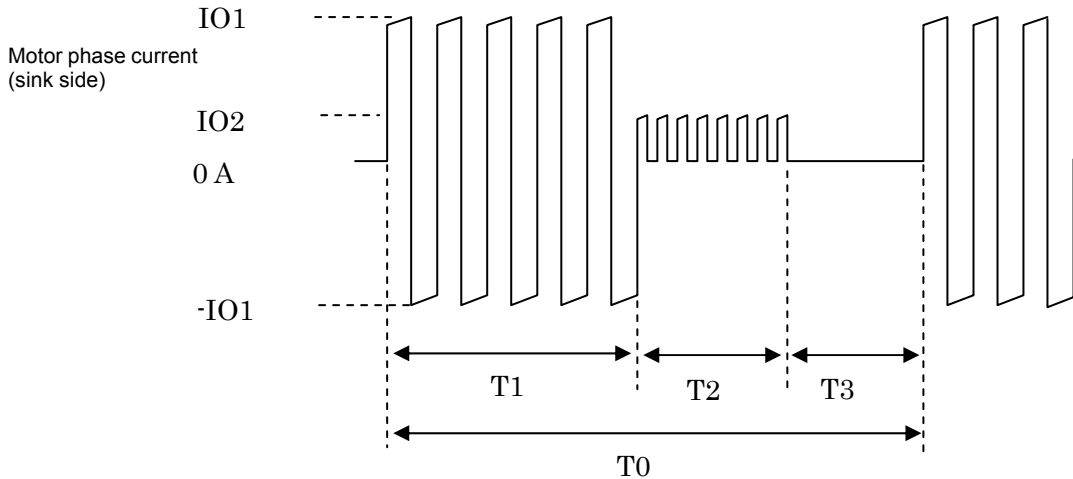


Figure 1 Motor Current Timing

T1: Motor rotation operation time

T2: Motor hold operation time

T3: Motor current off time

T2 may be reduced, depending on the application.

T0: Single repeated motor operating cycle

IO1 and IO2: Motor current peak values

Due to the structure of motor windings, the phase current is a positive and negative current with a pulse form.

Note that figure 1 presents the concepts here, and that the on/off duty of the actual signals will differ.

The hybrid IC internal average power dissipation PdAV can be calculated from the following formula.

$$PdAV = (T1 \times P1 + T2 \times P2 + T3 \times 0) \div T0 \text{ ----- (I)}$$

(Here, P1 is the PdAV for IO1 and P2 is the PdAV for IO2)

If the value calculated using Equation (I) is 1.5W or less, and the ambient temperature, Ta, is 60°C or less, there is no need to attach a heat sink. Refer to Figure 2 for operating substrate temperature data when no heat sink is used.

[Operating range in which a heat sink is used]

Although a heat sink is attached to lower Tc if PdAV increases, the resulting size can be found using the value of θc-a in Equation (II) below and the graph depicted in Figure 3.

$$\theta_{c-a} = (Tc \text{ max} - Ta) \div PdAV \text{ ----- (II)}$$

Tc max: Maximum operating substrate temperature = 105°C

Ta: HIC ambient temperature

Although a heat sink can be designed based on equations (I) and (II) above, be sure to mount the HIC in a set and confirm that the substrate temperature, Tc, is 105°C or less.

The average HIC power loss, PdAV, described above represents the power loss when there is no avalanche operation. To add the loss during avalanche operations, be sure to add Equation (3-2), “Allowable STK672-4\*\* Avalanche Energy Value”, to PdAV.



Figure 2

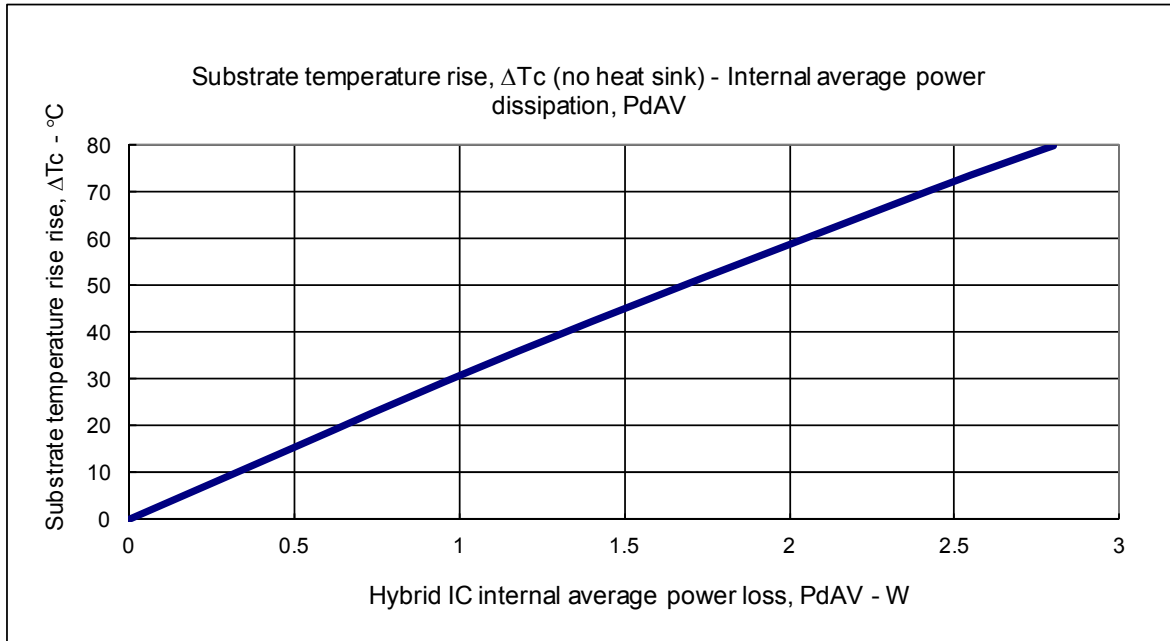
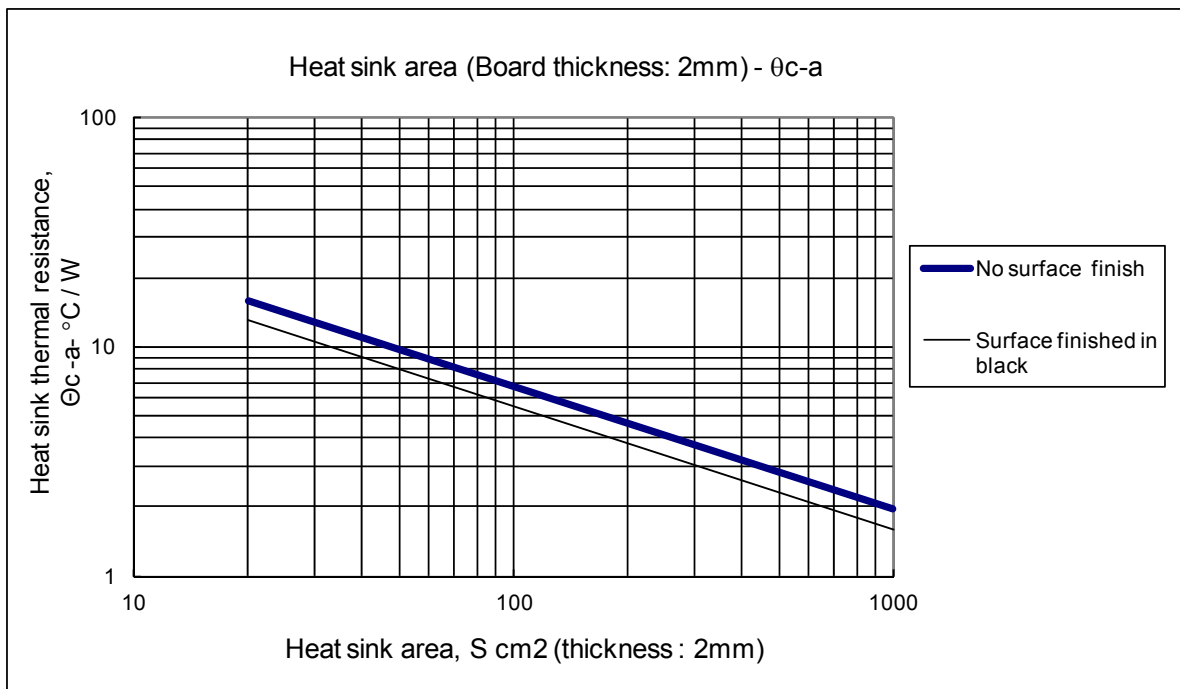


Figure 3



## STK672-440BN-E

### 6. Mitigated Curve of Package Power Loss, PdPK, vs. Ambient Temperature, Ta

Package power loss, PdPK, refers to the average internal power loss, PdAV, allowable without a heat sink. The figure below represents the allowable power loss, PdPK, vs. fluctuations in the ambient temperature, Ta. Power loss of up to 3.1W is allowable at Ta=25°C, and of up to 1.75W at Ta=60°C.

\* The package thermal resistance  $\theta_{c-a}$  is 25.8°C/W.

