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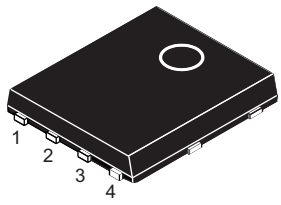
STL110N10F7

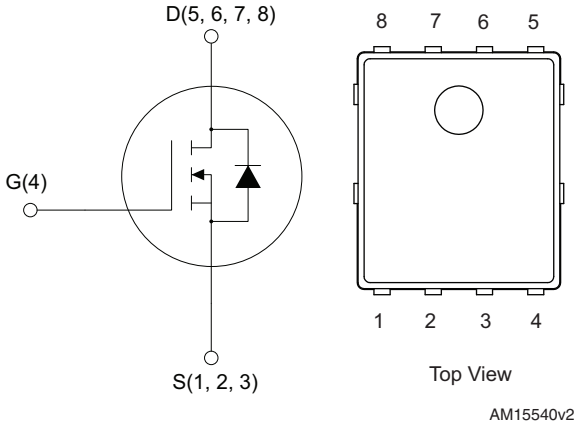
N-channel 100 V, 0.005 Ω typ., 107 A, STripFET™ H7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data



PowerFLAT™5x6

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STL110N10F7	100 V	0.006 Ω (V_{GS}= 10 V)	107 A	136 W

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes the STripFET™ H7 technology with a trench gate structure combined with extremely low on-resistance. The device also offers ultra-low capacitances for higher switching frequency operations.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL110N10F7	110N10F7	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	107	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	75	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	21	A
I_D (2)	Drain current (continuous) at T_{pcb}=100 °C	14	A
I_{DM} (2)(3)	Drain current (pulsed)	84	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	136	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25 °C	4.8	W
E_{AS} (4)	Single pulse avalanche energy	490	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. This value is rated according to $R_{thj\text{-}c}$.
2. This value is rated according to $R_{thj\text{-}pcb}$.
3. Pulse width limited by safe operating area.
4. Starting T_j=25 °C, I_d=18 A, V_{dd}=50 V

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.1	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 100 V			1	µA
		V_{GS} = 0, V_{DS} = 100 V, T_C=125 °C			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 10 A		0.005	0.006	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f=1 MHz, V_{GS}=0	-	5117	-	pF
C_{oss}	Output capacitance		-	992	-	pF
C_{rss}	Reverse transfer capacitance		-	39	-	pF
Q_g	Total gate charge	V_{DD}= 50 V, I_D = 21 A V_{GS} =10 V *Figure 14*	-	72	-	nC
Q_{gs}	Gate-source charge		-	30	-	nC
Q_{gd}	Gate-drain charge		-	17	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=50 V, I_D= 10 A, R_G=4.7 Ω, V_{GS}= 10 V *Figure 13*	-	25	-	ns
t_r	Rise time		-	36	-	ns
$t_{d(off)}$	Turn-off delay time		-	52	-	ns
t_f	Fall time		-	21	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		21	A
I_{SDM}(1)	Source-drain current (pulsed)		-		84	A
V_{SD}(2)	Forward on voltage	V_{GS}=0, I_{SD} = 21 A	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 21 A, di/dt = 100 A/µs, V_{DD}=80 V, T_j=150 °C	-	77		ns
Q_{rr}	Reverse recovery charge		-	150		nC
I_{RRM}	Reverse recovery current		-	4.3		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

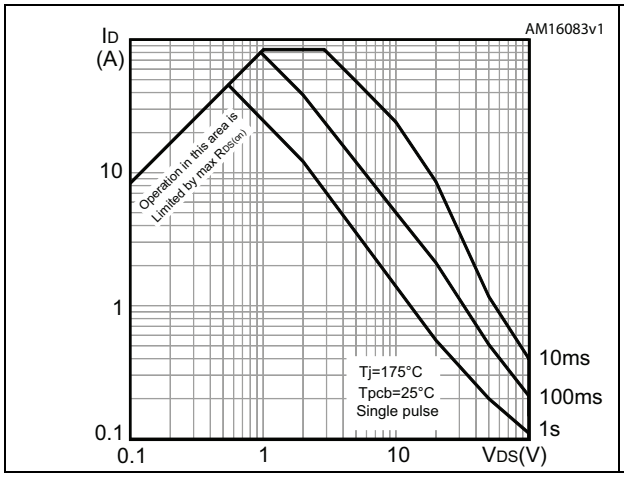


Figure 3. Thermal impedance

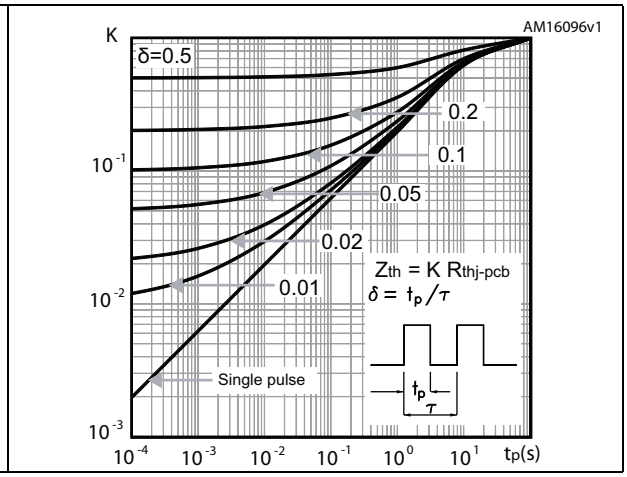


Figure 4. Output characteristics

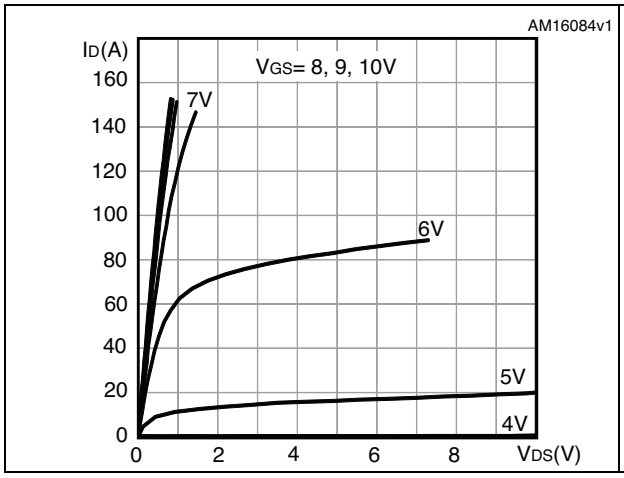


Figure 5. Transfer characteristics

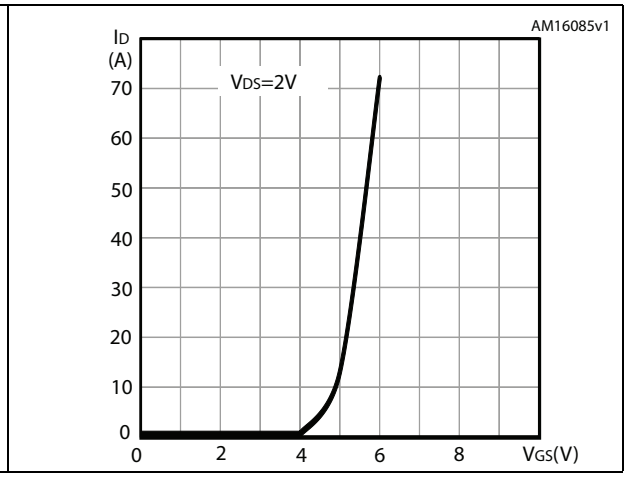


Figure 6. Gate charge vs gate-source voltage

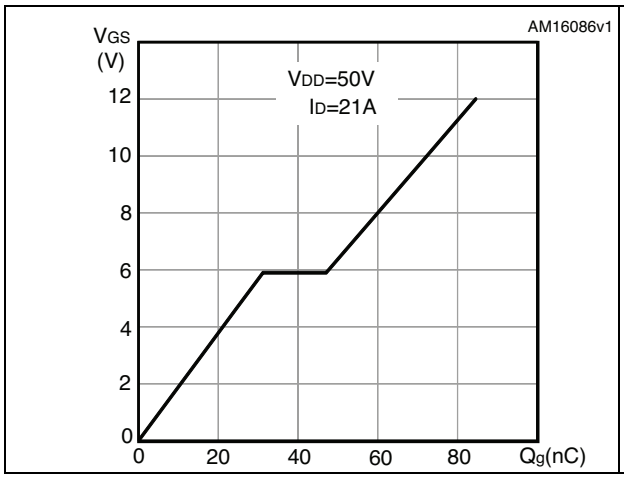


Figure 7. Static drain-source on-resistance

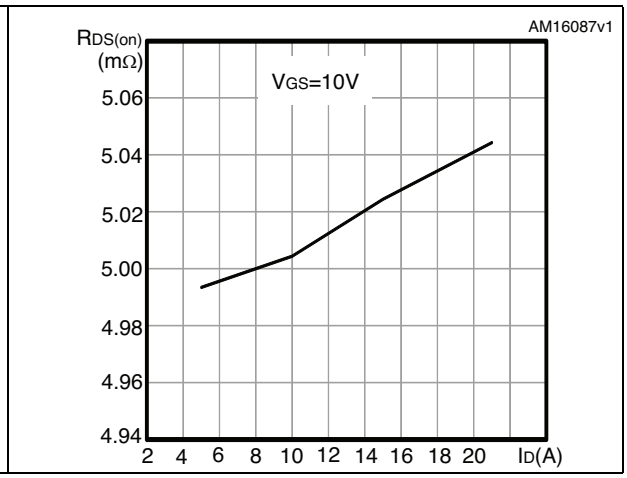


Figure 8. Capacitance variations

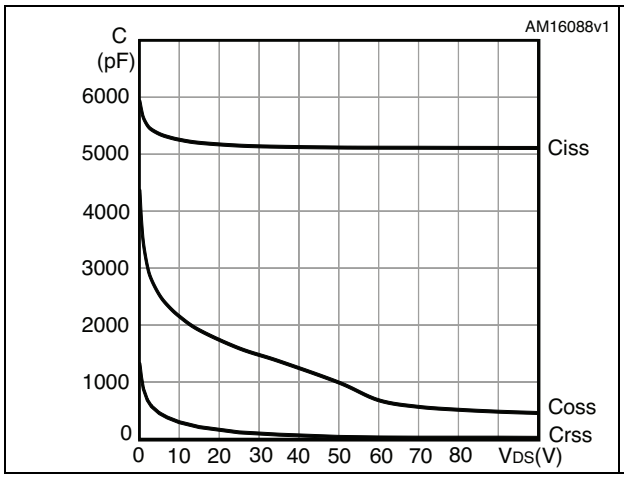


Figure 9. Normalized gate threshold voltage vs temperature

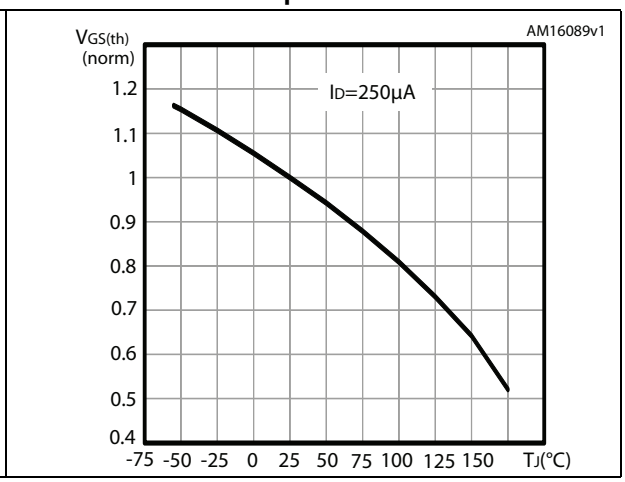


Figure 10. Normalized on-resistance vs temperature

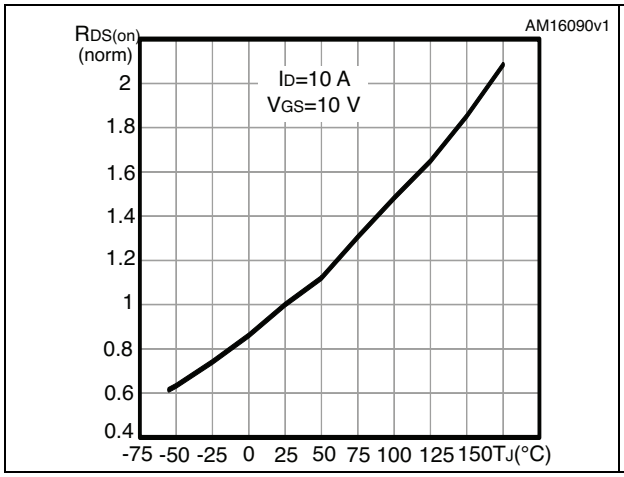


Figure 11. Source-drain diode forward characteristics

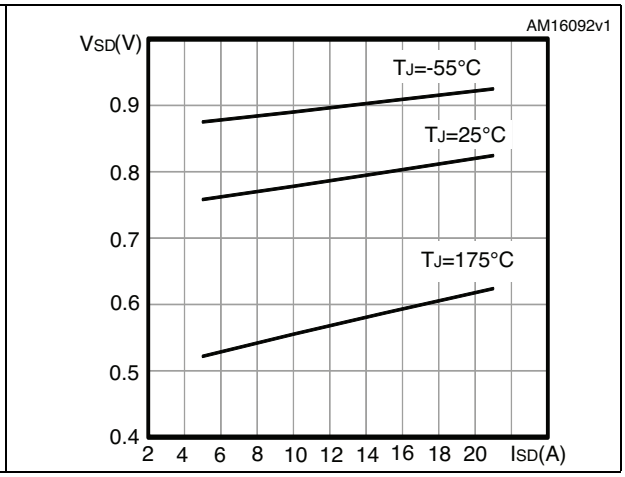
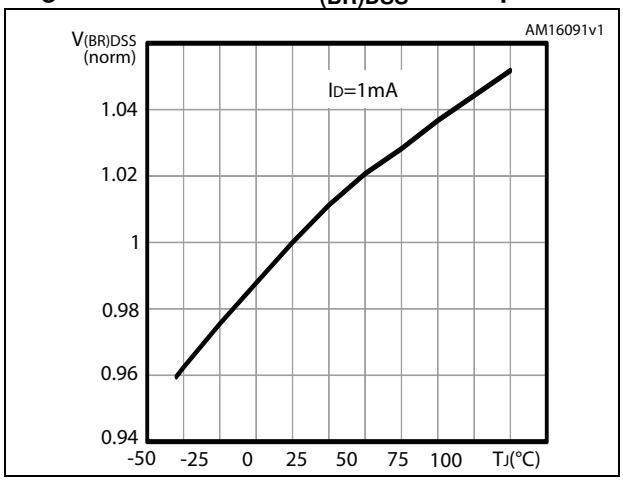


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load

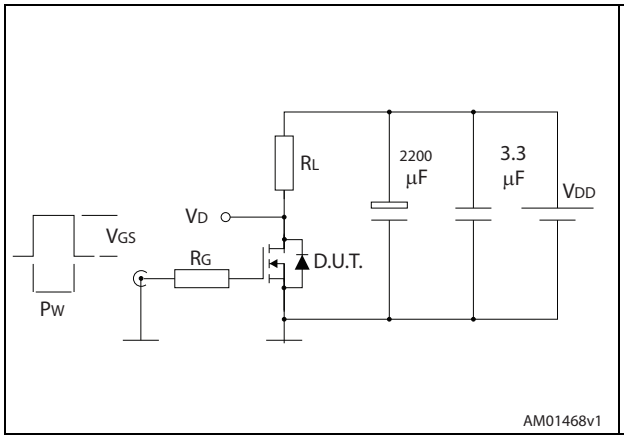


Figure 14. Gate charge test circuit

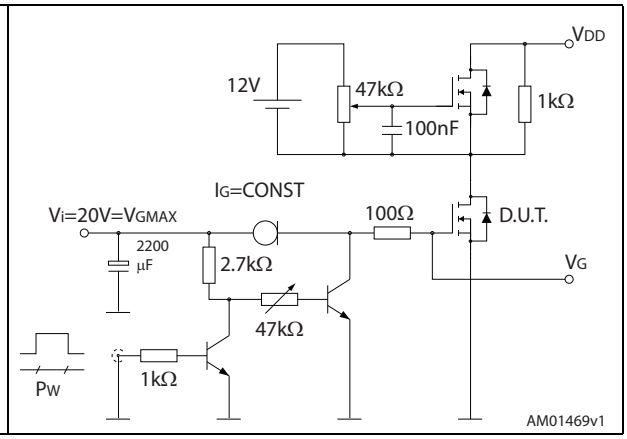


Figure 15. Test circuit for inductive load switching and diode recovery times

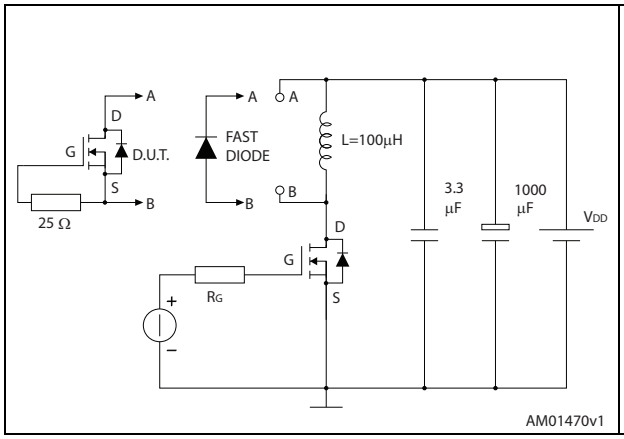


Figure 16. Unclamped inductive load test circuit

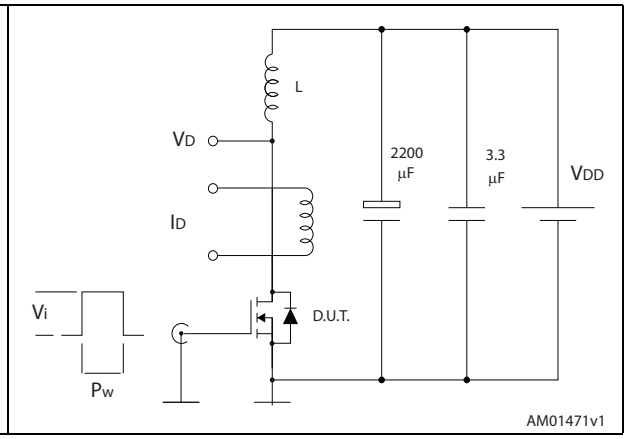


Figure 17. Unclamped inductive waveform

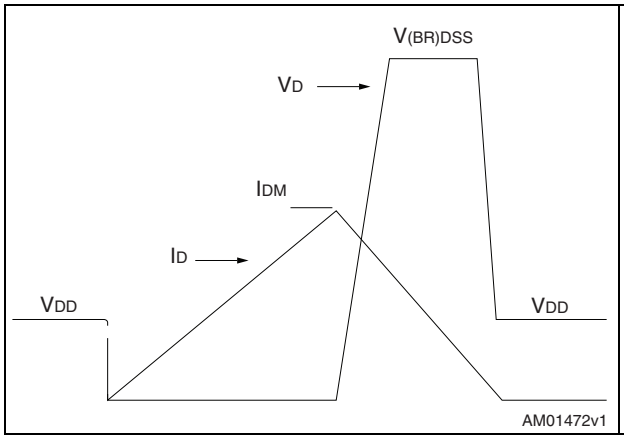
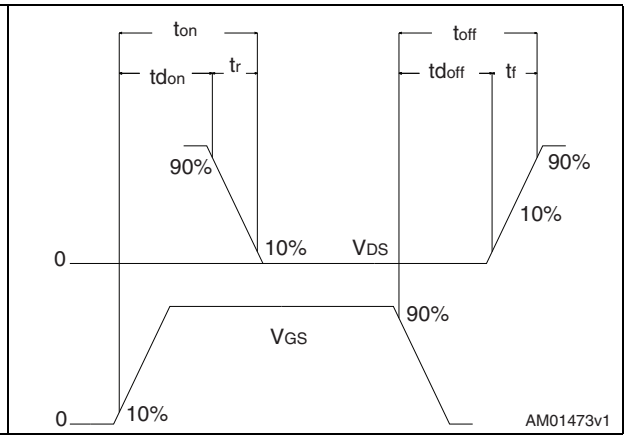


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

Figure 19. PowerFLAT™ 5x6 type S-C mechanical data

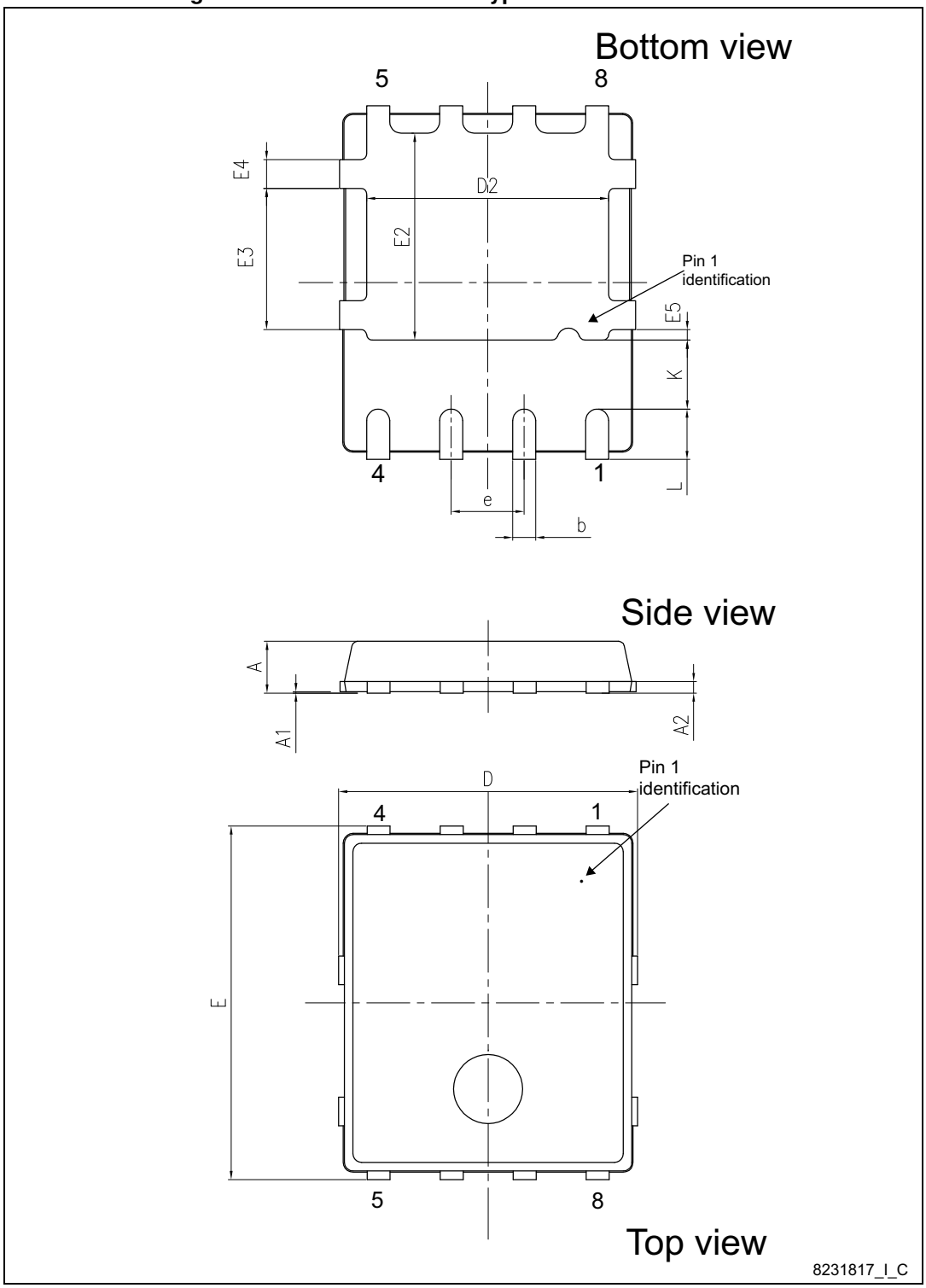
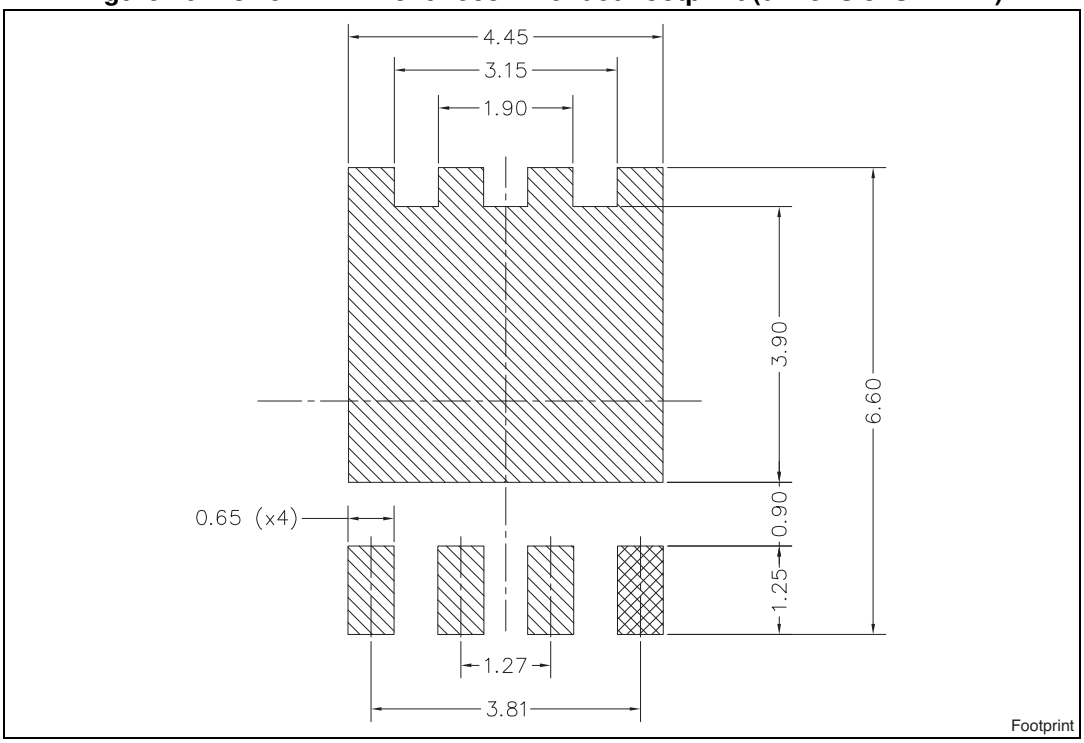


Table 8. PowerFLAT™ 5x6 type S-C mechanical data

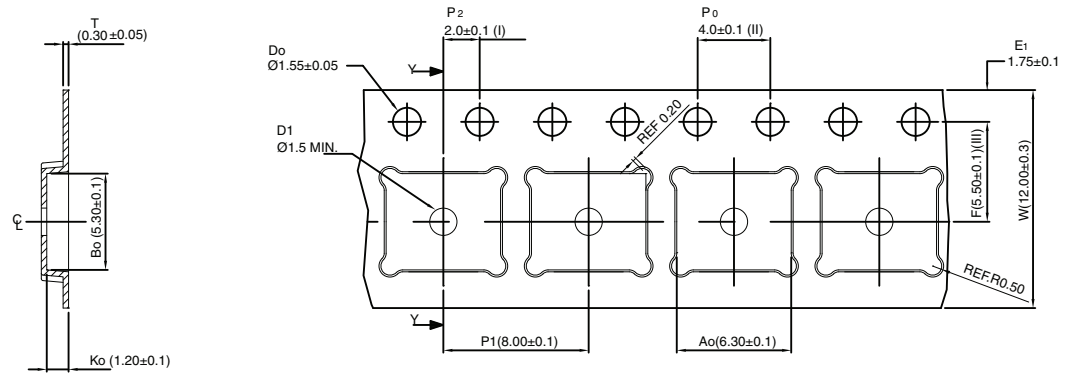
Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
D2	4.11		4.31
E		6.15	
e		1.27	
e1		0.65	
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
K	1.05		1.35
L	0.715		1.015

Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape[a]



(I) Measured from centerline of sprocket hole to centerline of pocket.

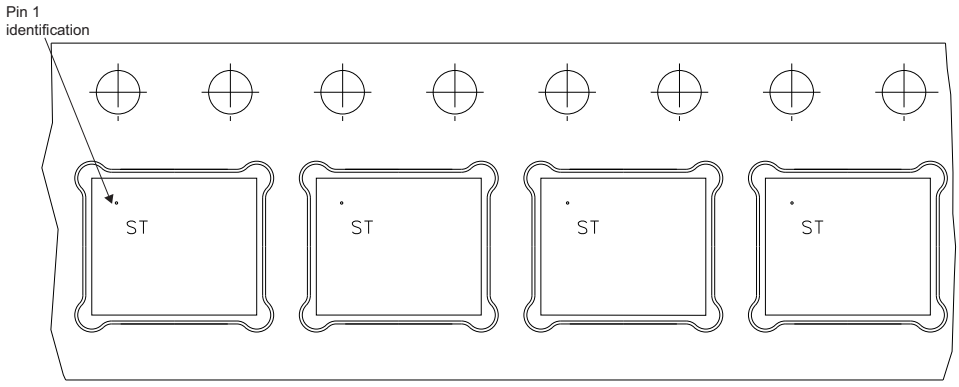
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centerline of sprocket hole to centerline of pocket.

Base and bulk quantity 3000 pcs

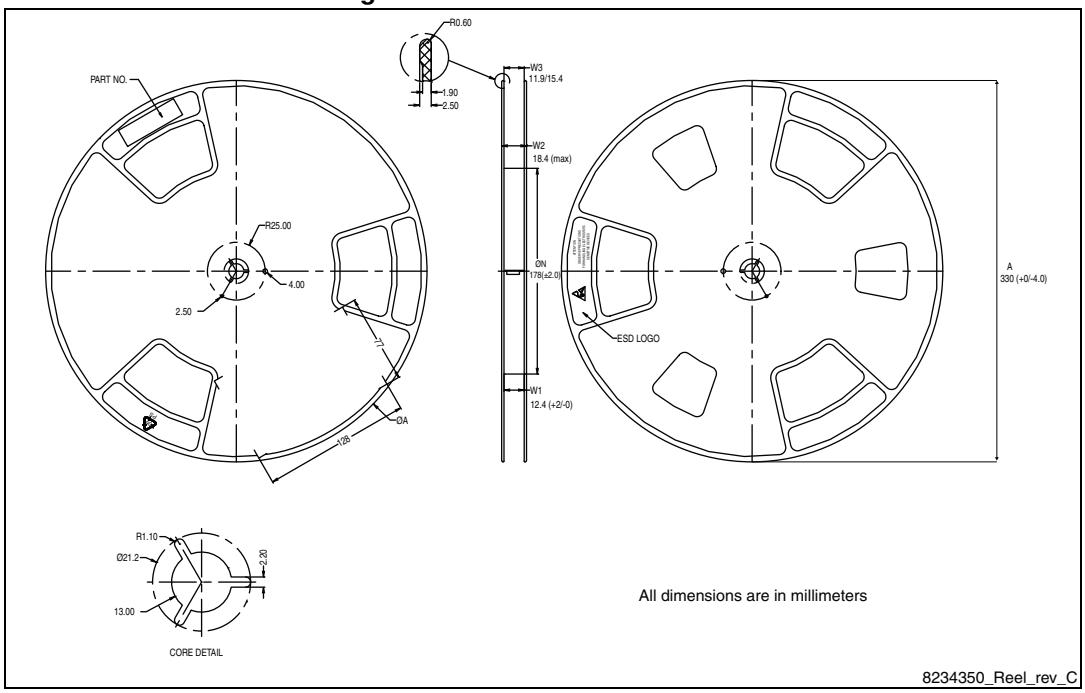
8234350_Tape_rev_C

Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Dec-2012	1	First release.
12-Dec-2013	2	– Modified: P_{TOT} value and *Figure 1* in cover page – Modified: I_D, I_{DM} and P_{TOT} values in *Table 2* – Added: E_{AS} value in *Table 2* – Modified: all values in *Table 3* – Modified: I_{DSS}, I_{GSS} and I_D for $R_{DS(on)}$ – Updated: the entire typical values in *Table 5*, *6* and *7* – Updated: *Figure 13*, *14*, *15* and *16* – Minor text changes
25-Mar-2014	3	– Updated title and features on cover page. – Added P_{TOT} value at T_C = 25 °C in *Table 2: Absolute maximum ratings*. – Updated *Section 4: Package mechanical data*.
20-Aug-2014	4	– Modified: title, features and description – Modified: *Figure 2* and *3* – Updated: *Section 4: Package mechanical data* – Minor text changes