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STL12N3LLH5

N-channel 30 V, 0.0079 Ω , 12 A, PowerFLAT™ (3.3 x 3.3)
STripFET™ V Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on) max}	I _D
STL12N3LLH5	30 V	< 0.009 Ω	12 A ⁽¹⁾

1. The value is rated according Rthj-pcb

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

The STL12N3LLH5 is a 30 V N-channel STripFET™ V. This Power MOSFET technology is among the latest improvements, which have been especially tailored to achieve very low on-state resistance providing also one of the best-in-class figure of merit (FOM).

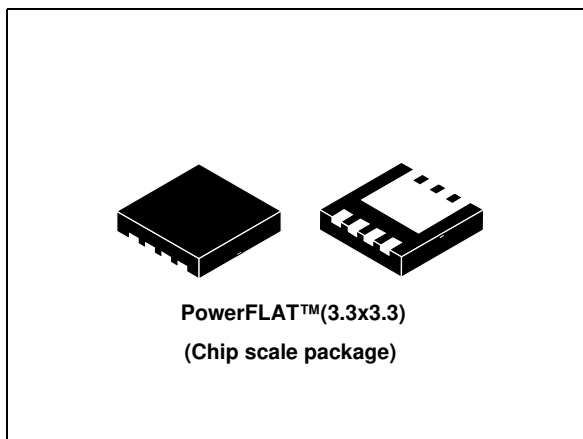


Figure 1. Internal schematic diagram

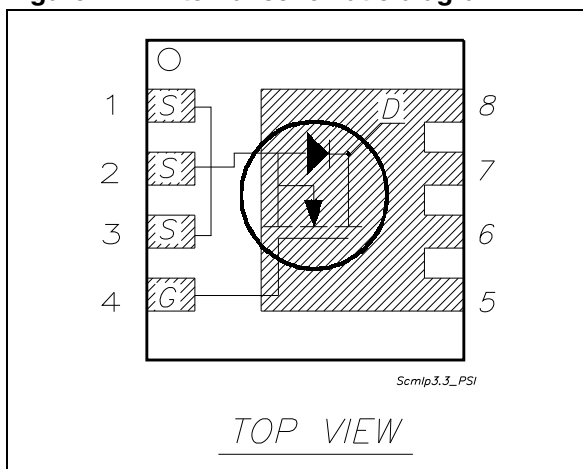


Table 1. Device summary

Order code	Marking	Package	Packaging
STL12N3LLH5	12N3L	PowerFLAT™ (3.3 x 3.3)	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-source voltage	± 22	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	12	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	7.5	A
$I_{DM}^{(2)}$	Drain current (pulsed)	48	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2	W
	Derating factor	0.4	W/ $^\circ\text{C}$
T_J T_{stg}	Operating junction temperature storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according to $R_{thj-pcb}$
2. Pulse width limited by safe operating area
3. The value is rated according to R_{thj-c}

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain)	2.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	42.8	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(2)}$	Thermal resistance junction-pcb	63.5	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch², 2 oz Cu, $t < 10$ sec
2. Steady-state

2 Electrical characteristics

($T_{CASE}=25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D=250\text{ }\mu\text{A}$, $V_{GS}=0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS}=\text{max. rating}$, $V_{DS}=\text{max. rating @ }125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS}=\pm 22\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS}=10\text{ V}$, $I_D=6\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=6\text{ A}$		0.0079 0.0095	0.0090 0.011	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS}=25\text{ V}$, $f=1\text{ MHz}$, $V_{GS}=0$		1500		pF
C_{oss}	Output capacitance			295		pF
C_{rss}	Reverse transfer capacitance			39		pF
Q_g	Total gate charge	$V_{DD}=15\text{ V}$, $I_D=12\text{ A}$		12		nC
Q_{gs}	Gate-source charge	$V_{GS}=4.5\text{ V}$		4		nC
Q_{gd}	Gate-drain charge	(see Figure 14)		4.7		nC
R_G	Gate input resistance	$f=1\text{ MHz}$ gate DC bias=0 Test signal level=20 mV Open drain	0.5	1.5	2.5	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$, $I_D=6\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 13)	-	9.3	-	ns
t_r	Rise time			14.5		ns
$t_{d(off)}$	Turn-off delay time			22.7		ns
t_f	Fall time			4.5		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		15	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		60	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=12\text{ A}$, $V_{GS}=0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD}=12\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ (see Figure 18)	-	25		ns
Q_{rr}	Reverse recovery charge			17.5		nC
I_{RRM}	Reverse recovery current			1.4		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5 %

3 Test circuits

Figure 2. Switching times test circuit for resistive load

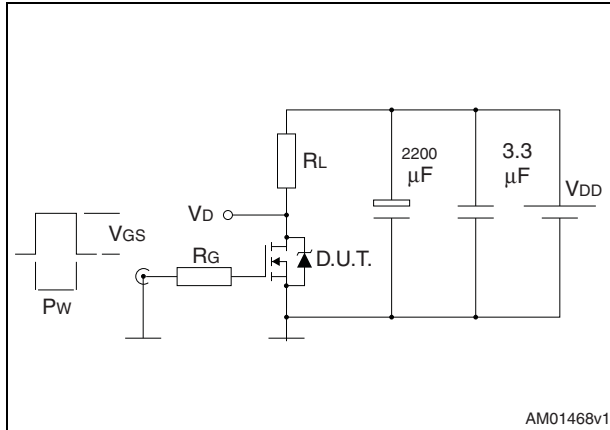


Figure 3. Gate charge test circuit

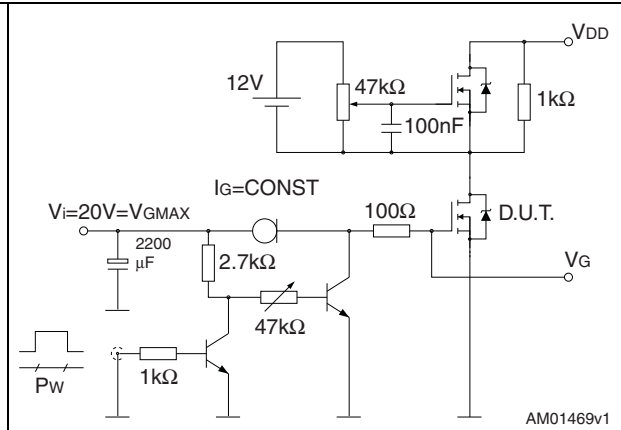


Figure 4. Test circuit for inductive load switching and diode recovery times

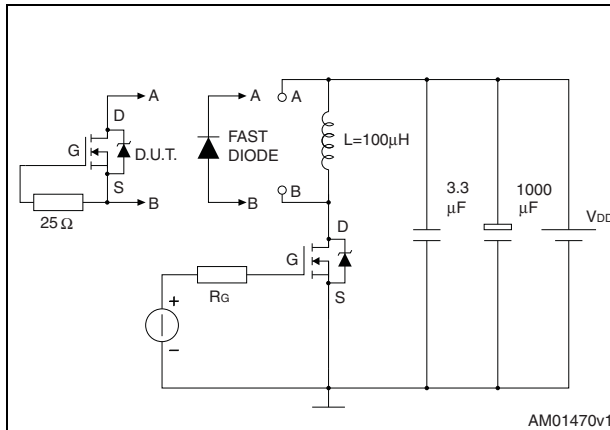


Figure 5. Unclamped inductive load test circuit

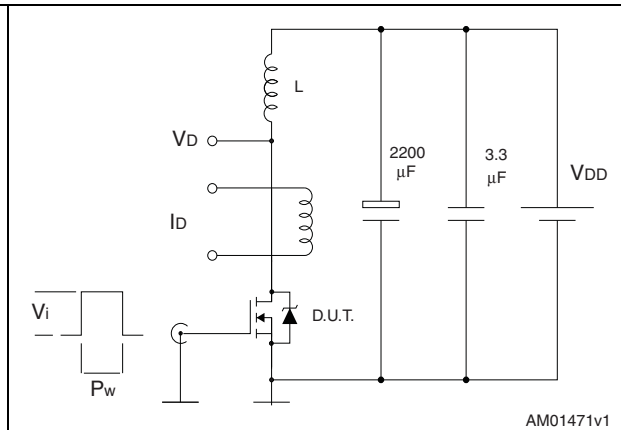


Figure 6. Unclamped inductive waveform

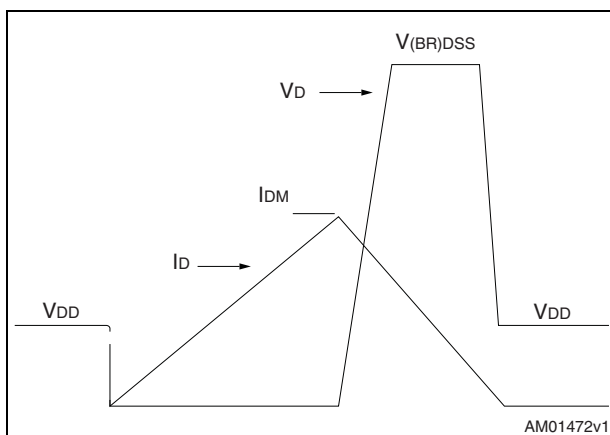
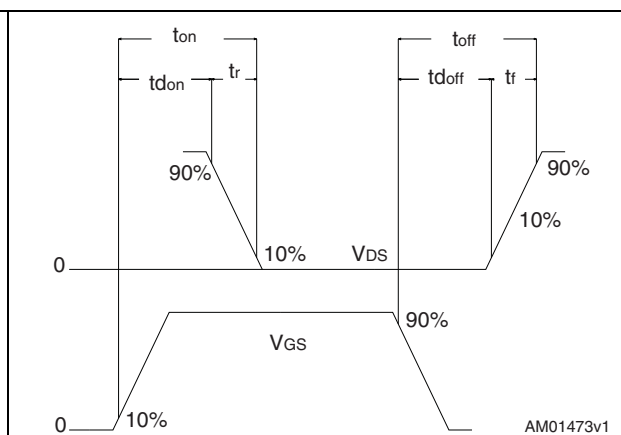


Figure 7. Switching time wave form



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ (3.3 x 3.3) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	
A3		0.20	
b	0.23	0.30	0.38
C		0.328	
C1		0.12	
D		3.30	
D2	2.50	2.65	2.75
E		3.30	
E2	1.25	1.40	1.50
F		1.325	
F1		0.975	
G		0.850	
G1		0.250	

Figure 8. PowerFLAT™ (3.3 x 3.3) drawing

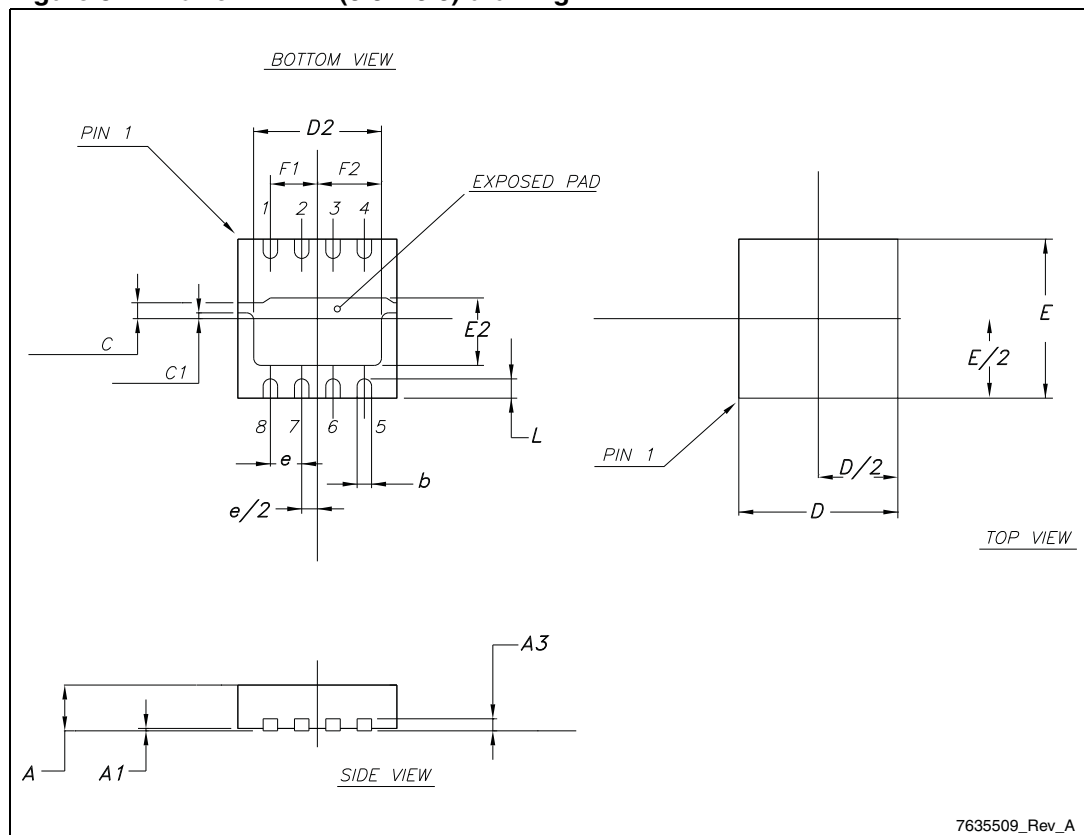
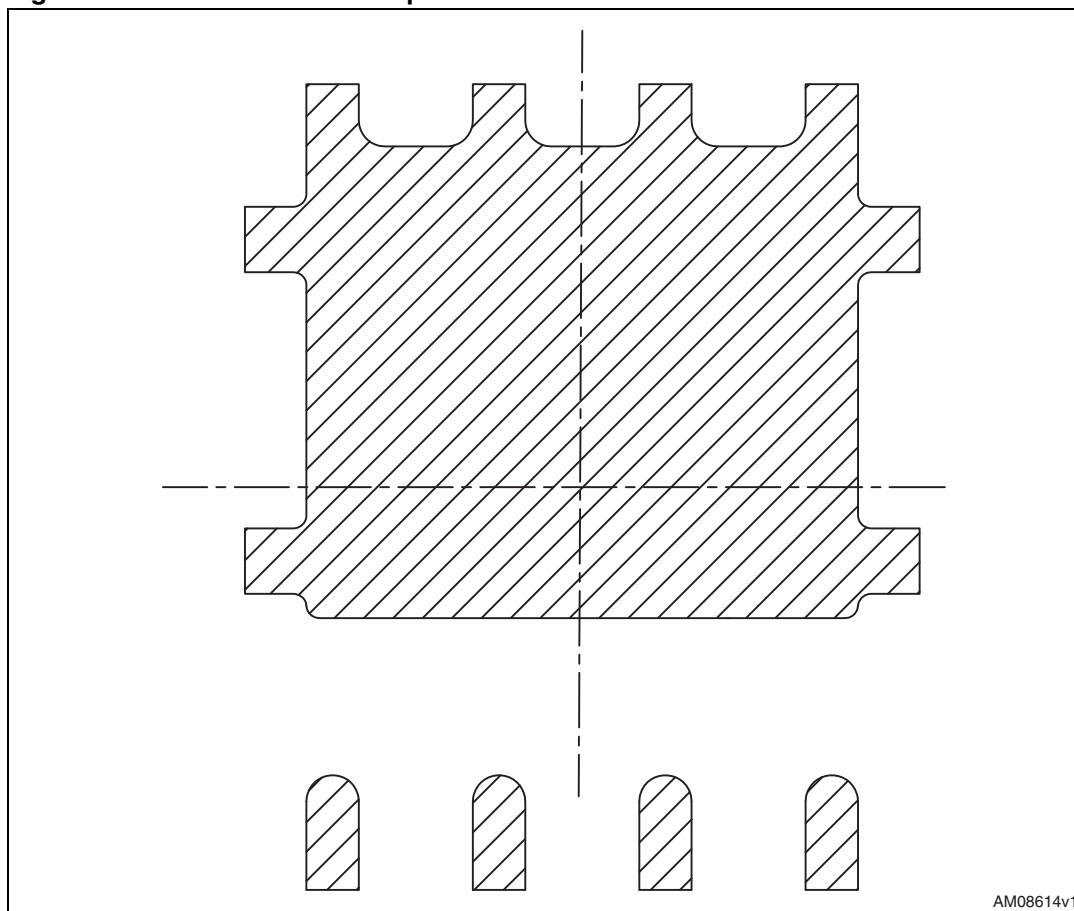


Figure 9. Recommended footprint



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Jun-2011	1	Initial release.

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