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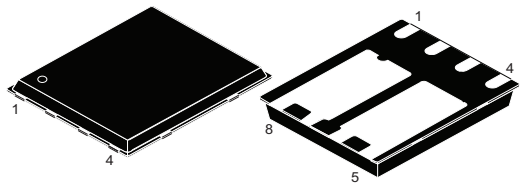
STL13DP10F6

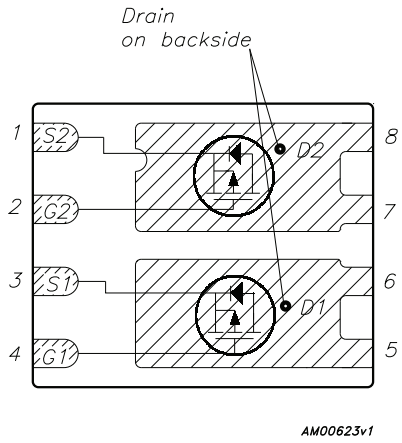
Dual P-channel 100 V, 0.136 Ω typ., 3.3 A STripFET™ VI DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 double island

Datasheet - production data



PowerFLAT™ 5x6 double island

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL13DP10F6	100 V	0.18 Ω	3.3 A

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is a dual P-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STL13DP10F6	13DP10F6	PowerFLAT™ 5x6 double island	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	13	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	7.3	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	3.3	A
I_D (2)	Drain current (continuous) at T_{pcb}=100°C	2	A
I_{DM} (2), (3)	Drain current (pulsed)	13.2	A
P_{TOT} (1)	Total dissipation at T_C = 25°C	62.5	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25°C	4	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. The value is rated according $R_{thj\text{-}c}$
2. The value is rated according $R_{thj\text{-}pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	32	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 100 V			1	µA
		V_{GS} = 0, V_{DS} = 100 V, T_C=125 °C			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS}= 10 V, I_D= 1.7 A		0.136	0.18	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	864	-	pF
C_{oss}	Output capacitance		-	45	-	pF
C_{rss}	Reverse transfer capacitance		-	25	-	pF
Q_g	Total gate charge	V_{DD}=50 V, I_D = 3.3 A V_{GS} =10 V *(see Figure 14)*	-	16.5	-	nC
Q_{gs}	Gate-source charge		-	3.5	-	nC
Q_{gd}	Gate-drain charge		-	3.8	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=50 V, I_D= 1.7 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 13)*	-	10.5	-	ns
t_r	Rise time		-	4.8	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	4.5	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3.3	A
I_{SDM}(1)	Source-drain current (pulsed)		-		13.2	A
V_{SD}(2)	Forward on voltage	I_{SD} = 3.3 A, V_{GS}=0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 3.3 A, di/dt = 100 A/µs, V_{DD}=80 V, T_j=150 °C	-	26.5		ns
Q_{rr}	Reverse recovery charge		-	36.5		nC
I_{RRM}	Reverse recovery current		-	2.7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

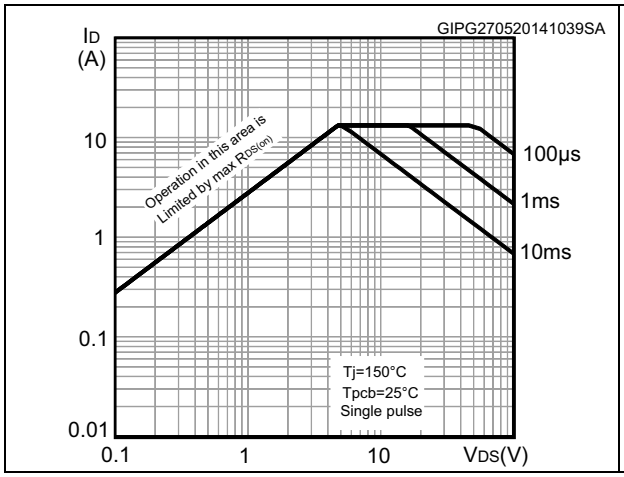


Figure 3. Thermal impedance

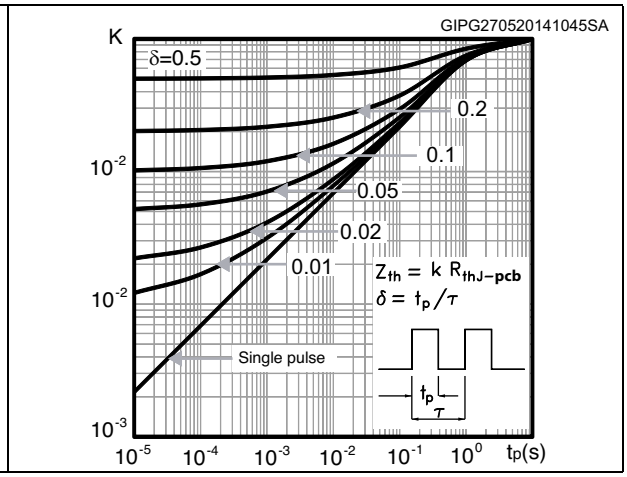


Figure 4. Output characteristics

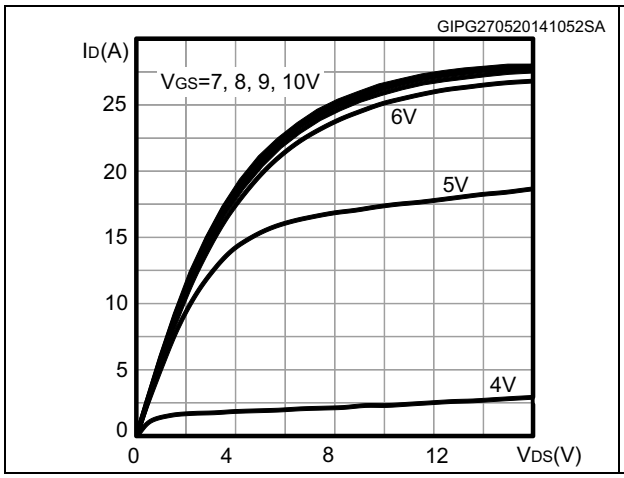


Figure 5. Transfer characteristics

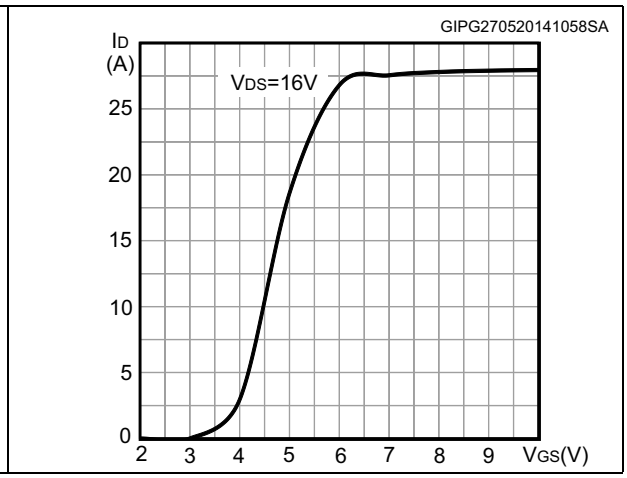


Figure 6. Gate charge vs gate-source voltage

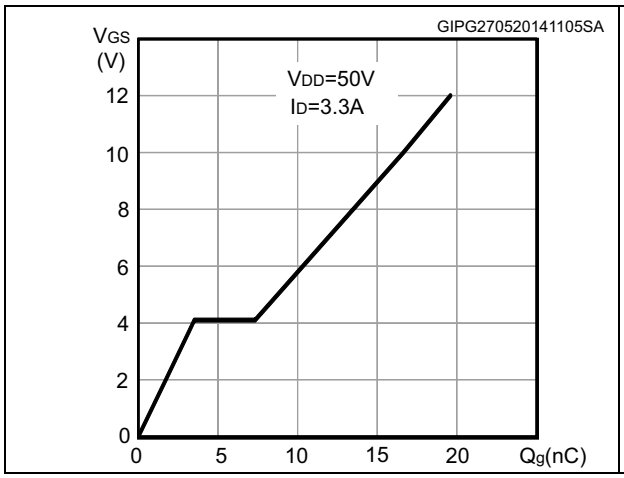


Figure 7. Static drain-source on-resistance

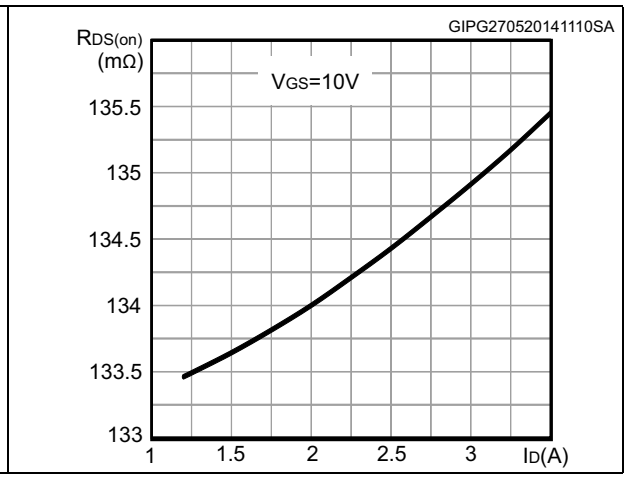


Figure 8. Capacitance variations

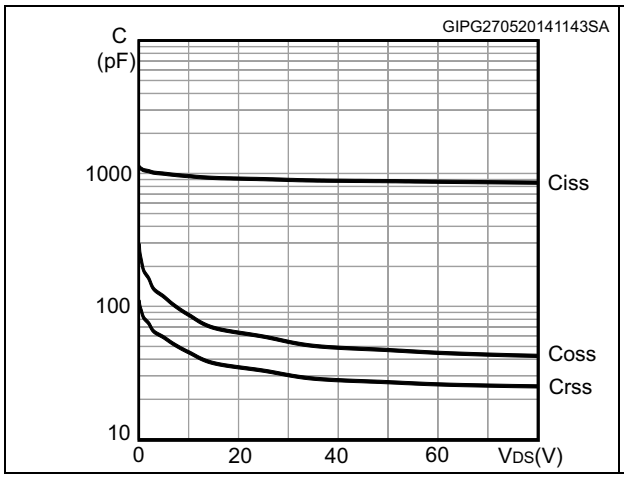


Figure 9. Normalized gate threshold voltage vs temperature

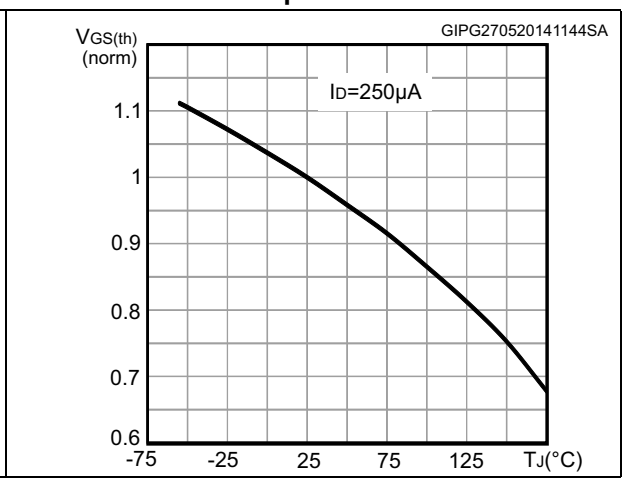


Figure 10. Normalized on-resistance vs temperature

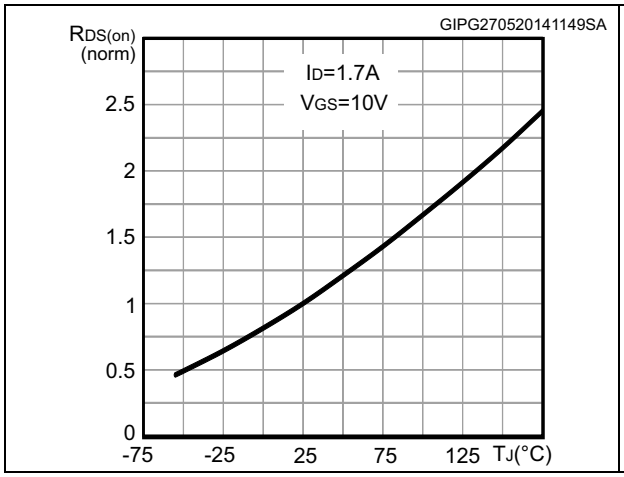


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

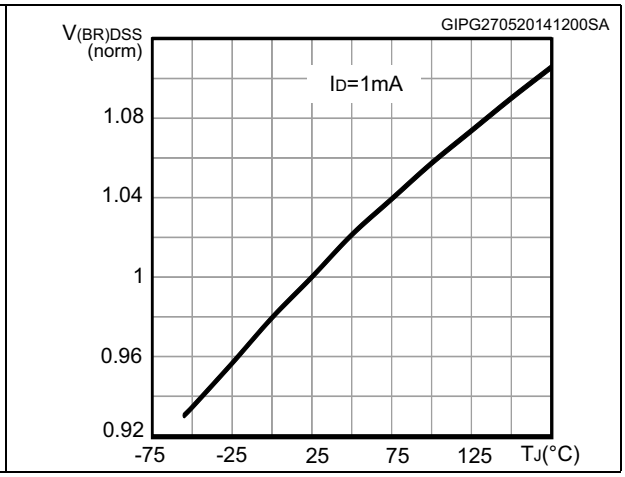
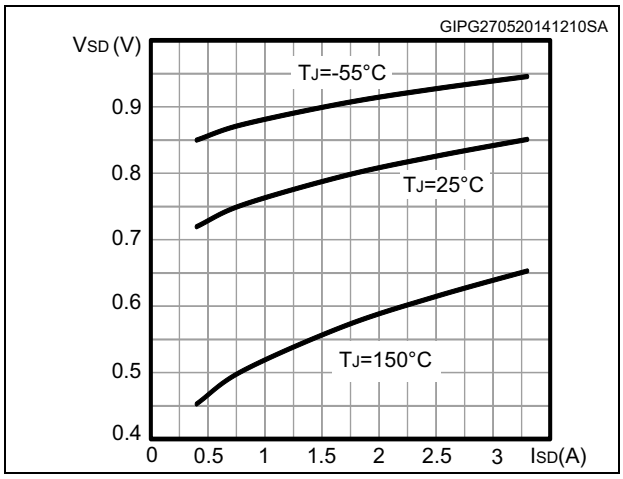


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

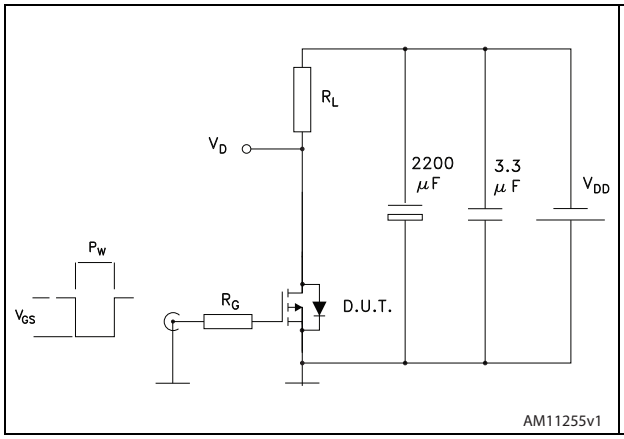


Figure 14. Gate charge test circuit

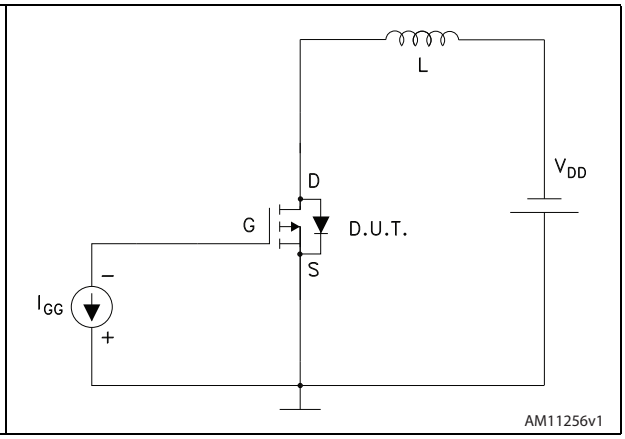
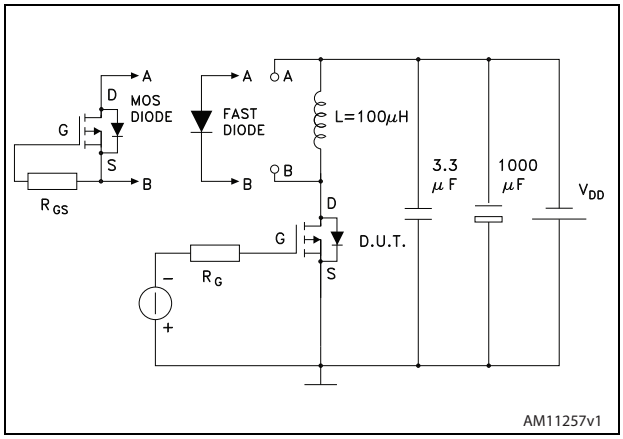


Figure 15. Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

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Figure 16. PowerFLAT™ 5x6 double island type R-A drawing

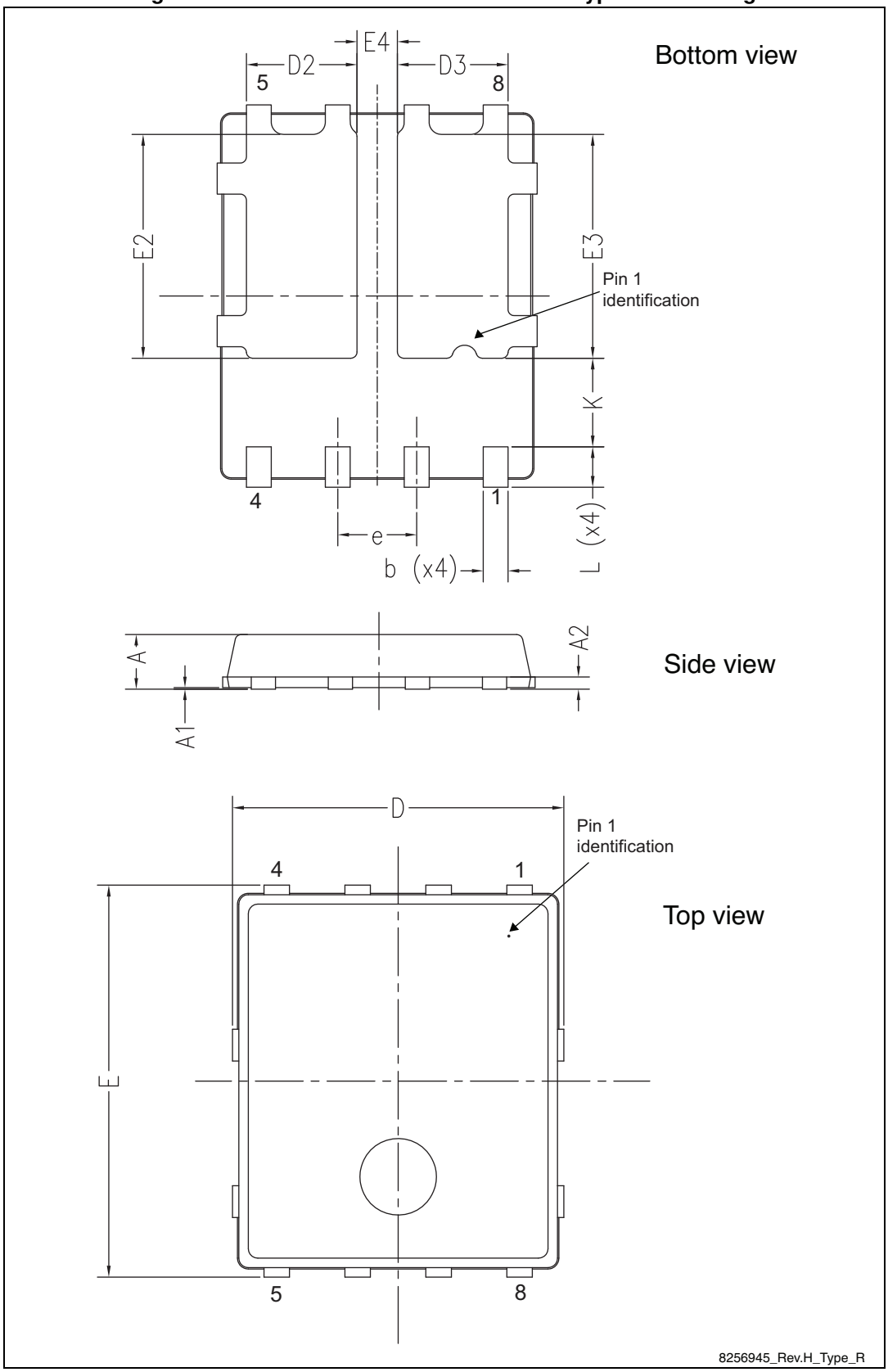
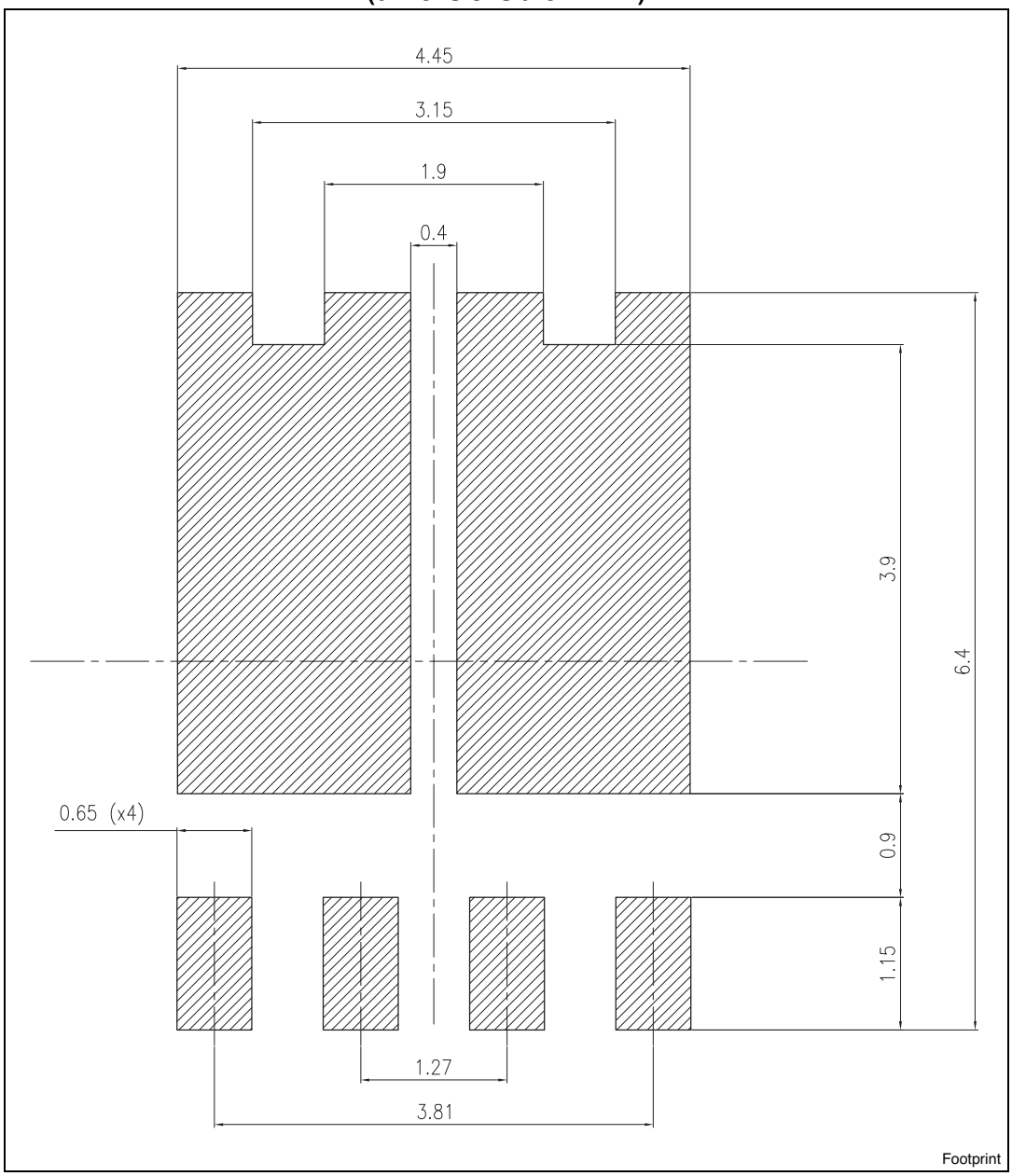


Table 8. PowerFLAT™ 5x6 double island type R-A mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 17. PowerFLAT™ 5x6 double island type R-A drawing recommended footprint (dimensions are in mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Nov-2012	1	First release.
30-May-2014	2	– Document status promoted from target to production data – Modified: title – Modified: $R_{DS(on)}$ typical value in *Table 4*, *5*, *6*, *7* and *8* – Added: *Section 2.1: Electrical characteristics (curves)* – Updated: *Section 4: Package mechanical data* – Minor text changes

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