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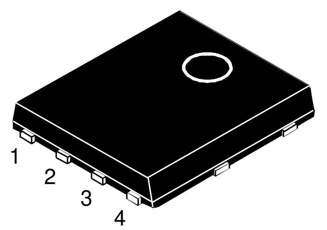
STL13N60DM2

life.augmented

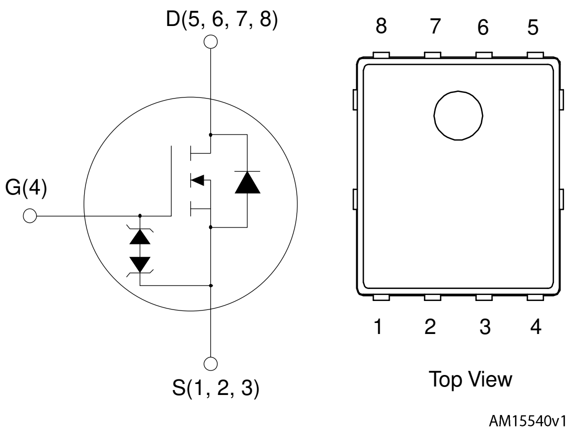
N-channel 600 V, 0.350 Ω typ., 8 A MDmesh™ DM2 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data



PowerFLAT™ 5x6 HV

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL13N60DM2	600 V	0.370 Ω	8 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STL13N60DM2	13N60DM2	PowerFLAT™ 5x6 HV	Tape and reel

This is information on a product in full production.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	8(1)	A
I_D	Drain current (continuous) at T_C= 100 °C	5	A
I_{DM}(2)	Drain current (pulsed)	32	A
P_{TOT}	Total dissipation at T_C = 25 °C	52	W
dv/dt(3)	Peak diode recovery voltage slope	40	V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range	150	

Notes:

(1)The value is limited by package.

(2)Pulse width limited by safe operating area.

(3)I_{SD} ≤ 8 A, di/dt ≤ 400 A/µs; $V_{DS\ peak}$ < $V_{(BR)DSS}$, V_{DD} = 400 V

(4)V_{DS} ≤ 480 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.40	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max(1)	59	°C/W

Notes:

(1)When mounted on 1 inch^2 FR-4, 2 Oz copper board

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T_{jmax})	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	340	mJ

2 Electrical characteristics

(T_C= 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0 V, V_{DS} = 600 V			1.5	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4 A		0.350	0.370	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	730	-	pF
C_{oss}	Output capacitance		-	38	-	pF
C_{rss}	Reverse transfer capacitance		-	0.9	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	70	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0 A	-	5.1	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 11 A, V_{GS} = 10 V (see *Figure 15: "Test circuit for gate charge behavior"*)	-	19	-	nC
Q_{gs}	Gate-source charge		-	4.4	-	nC
Q_{gd}	Gate-drain charge		-	9.9	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 5.5 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Test circuit for resistive load switching times"* and *Figure 19: "Switching time waveform"*)	-	12.3	-	ns
t_r	Rise time		-	4.8	-	ns
$t_{d(off)}$	Turn-off-delay time		-	42.5	-	ns
t_f	Fall time		-	10.6	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
I_{SDM}(1)	Source-drain current (pulsed)		-		32	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 8 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	90		ns
Q_{rr}	Reverse recovery charge		-	252		nC
I_{RRM}	Reverse recovery current		-	5.6		A
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	170		ns
Q_{rr}	Reverse recovery charge		-	667		ns
I_{RRM}	Reverse recovery current		-	8.6		A

Notes:

(1)Pulse width is limited by safe operating area

(2)Pulse test: pulse duration = 300 µs, duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1 mA, I_D = 0 A	±30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

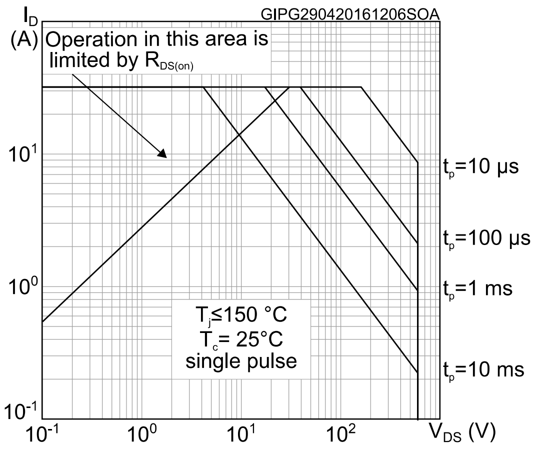


Figure 3: Thermal impedance

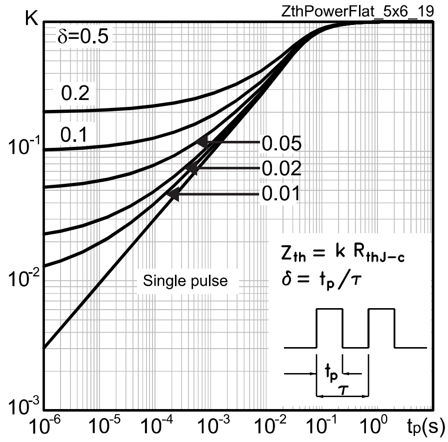


Figure 4: Output characteristics

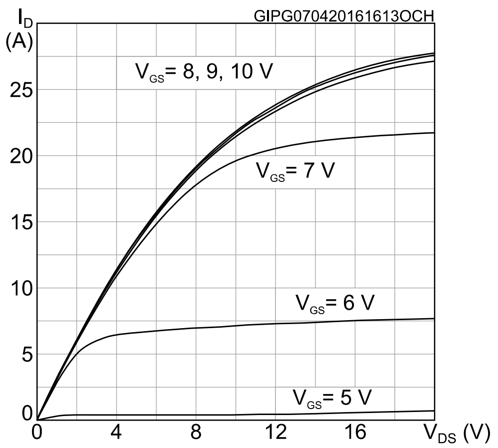


Figure 5: Transfer characteristics

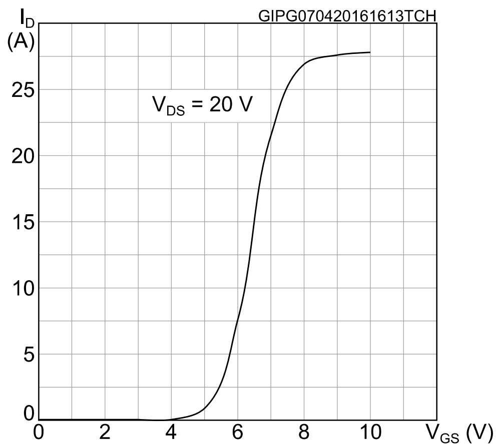


Figure 6: Gate charge vs gate-source voltage

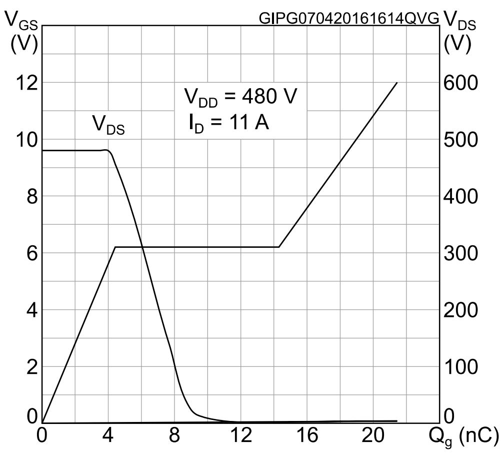


Figure 7: Static drain-source on-resistance

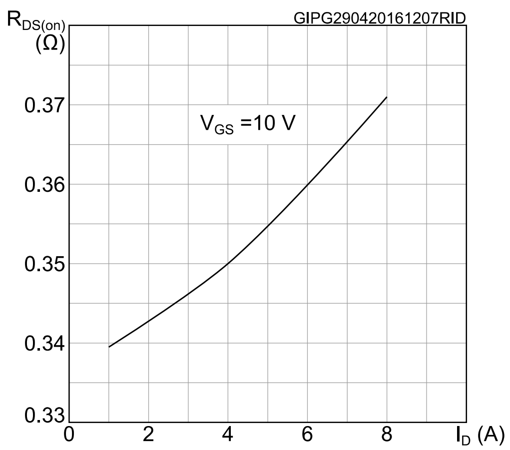


Figure 8: Capacitance variations

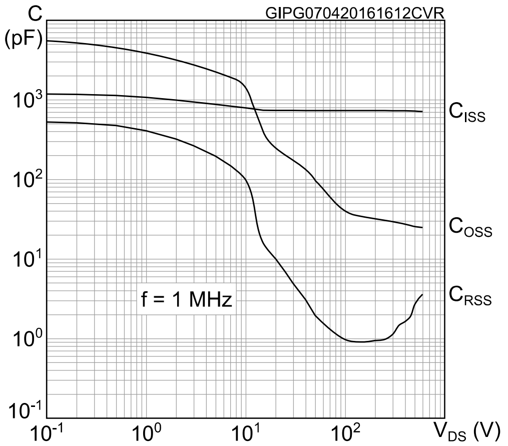


Figure 9: Normalized gate threshold voltage vs temperature

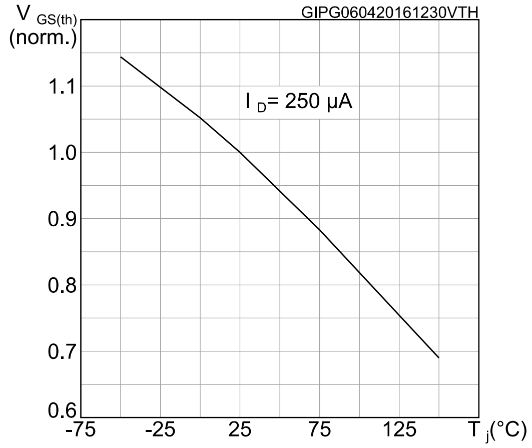


Figure 10: Normalized on-resistance vs temperature

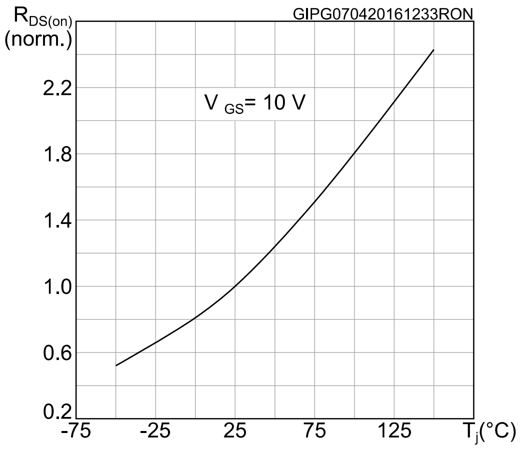


Figure 11: Normalized V(BR)DSS vs temperature

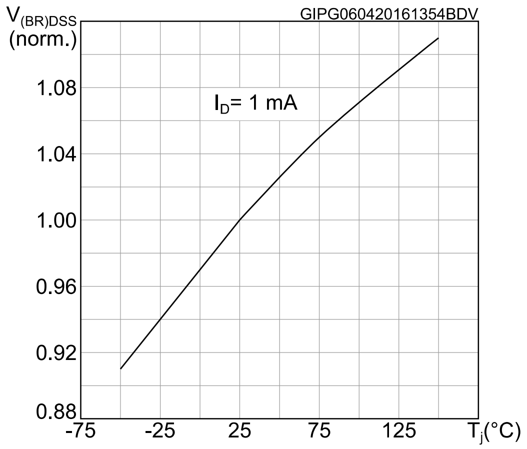


Figure 12: Source-drain diode forward characteristics

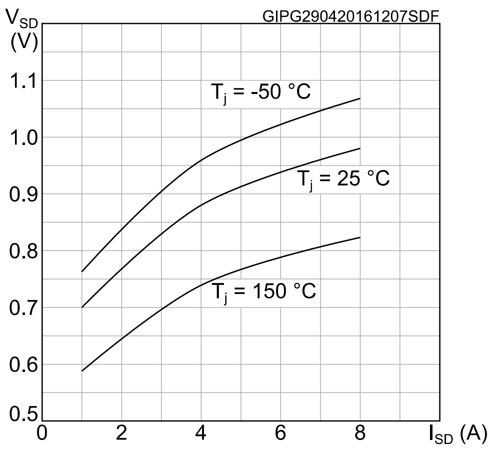
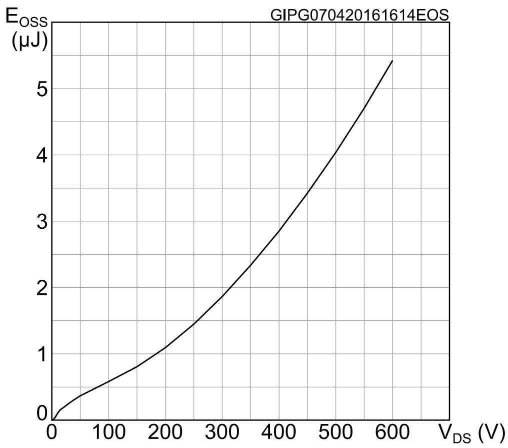


Figure 13: Output capacitance stored energy



3 Test circuits

Figure 14: Test circuit for resistive load switching times

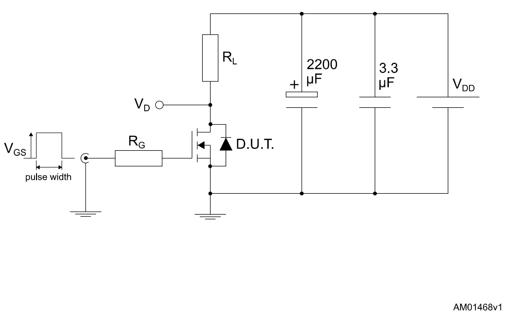


Figure 15: Test circuit for gate charge behavior

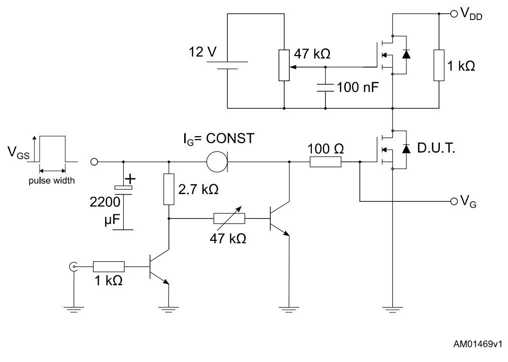


Figure 16: Test circuit for inductive load switching and diode recovery times

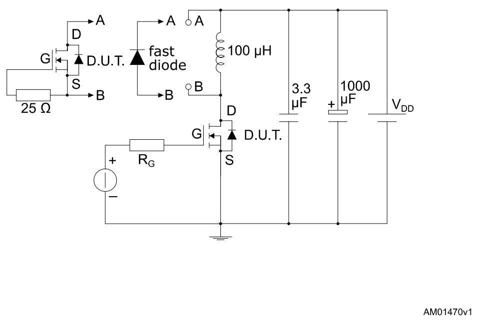


Figure 17: Unclamped inductive load test circuit

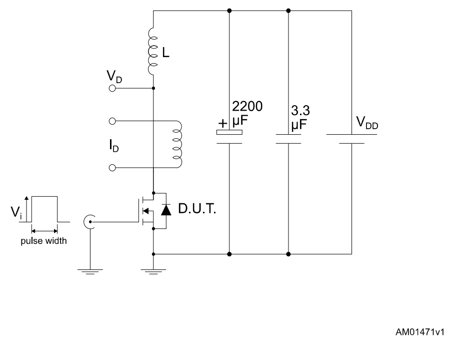


Figure 18: Unclamped inductive waveform

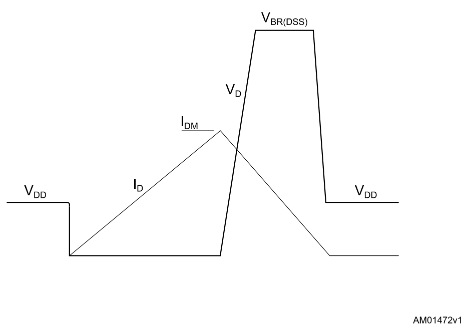
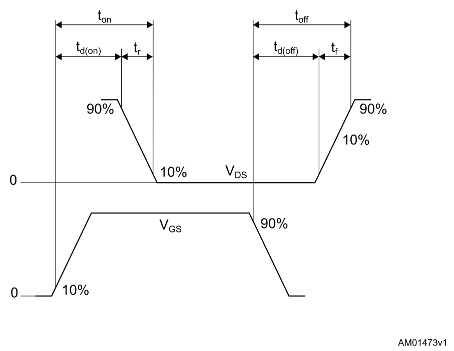


Figure 19: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 HV package information

Figure 20: PowerFLAT™ 5x6 HV package outline

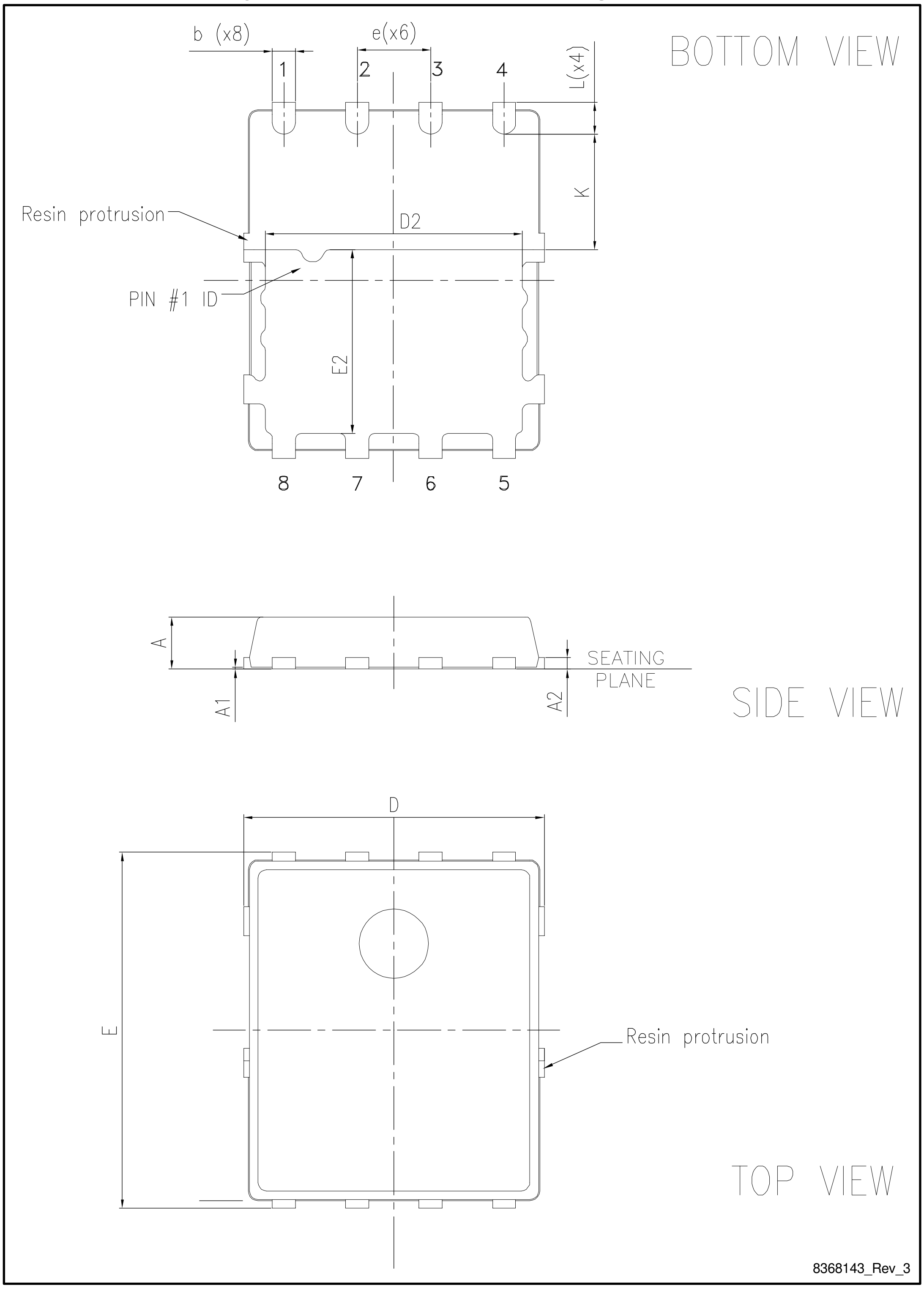
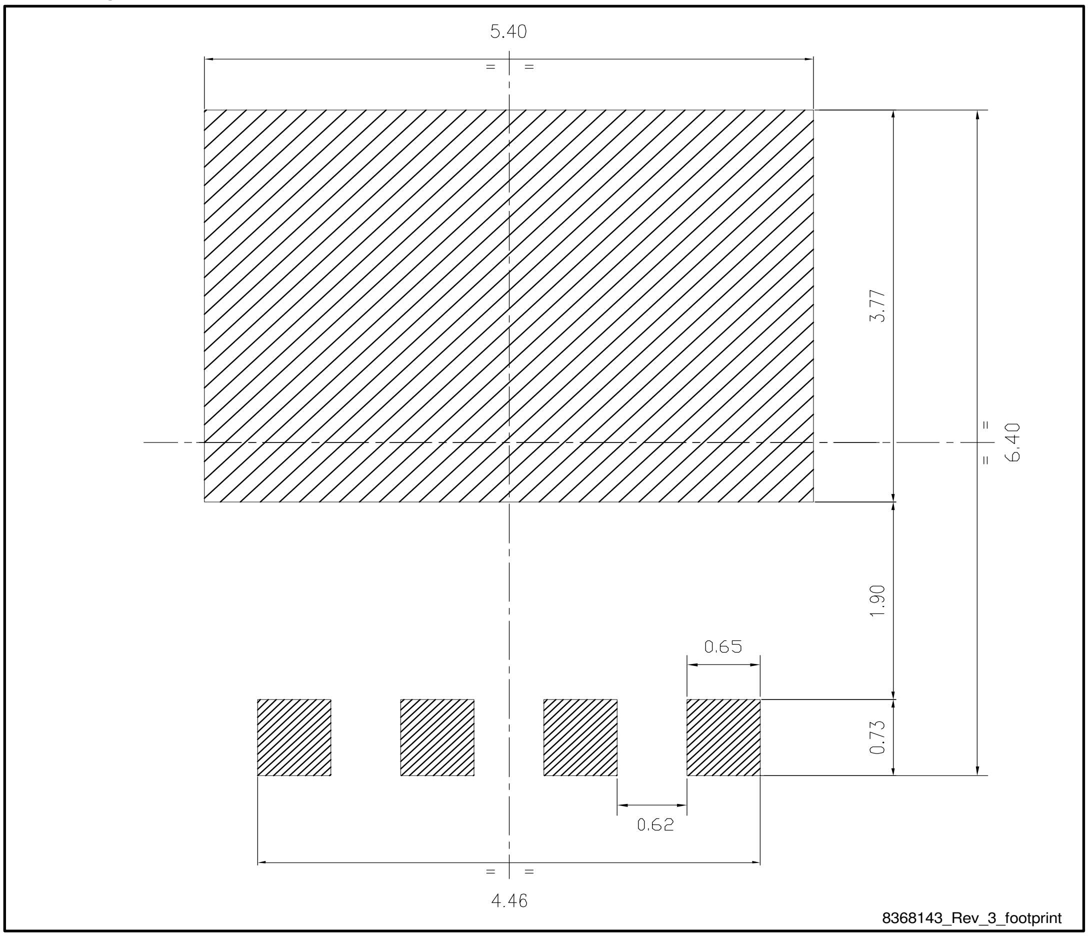


Table 10: PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.10	5.20	5.30
E	6.05	6.15	6.25
E2	3.10	3.20	3.30
D2	4.30	4.40	4.50
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 21: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)

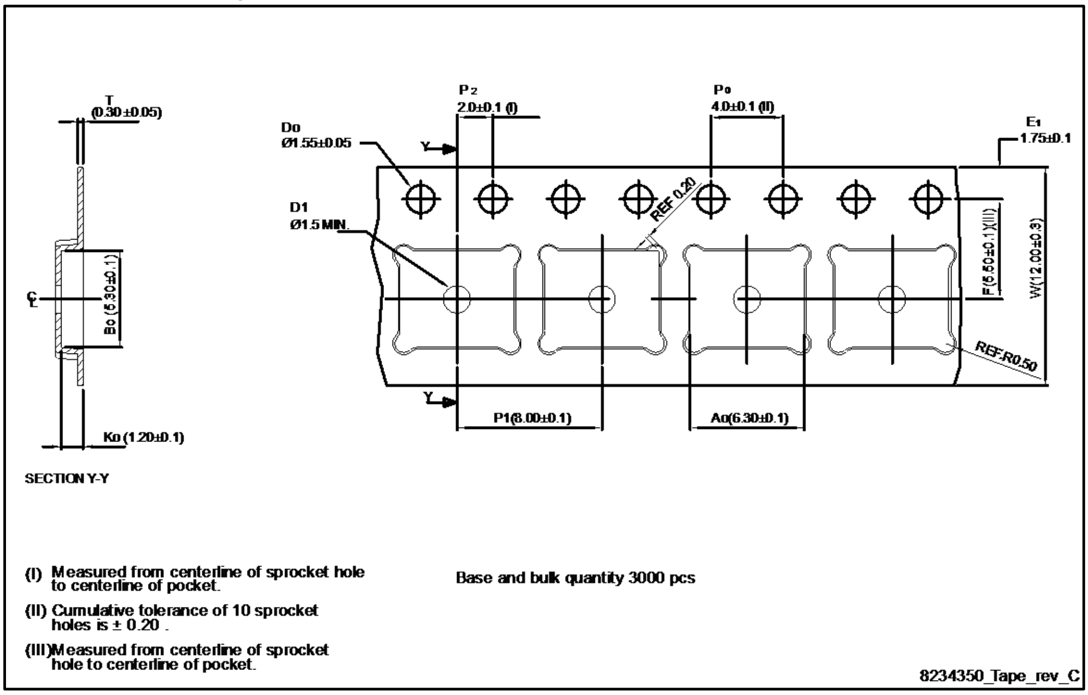


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape

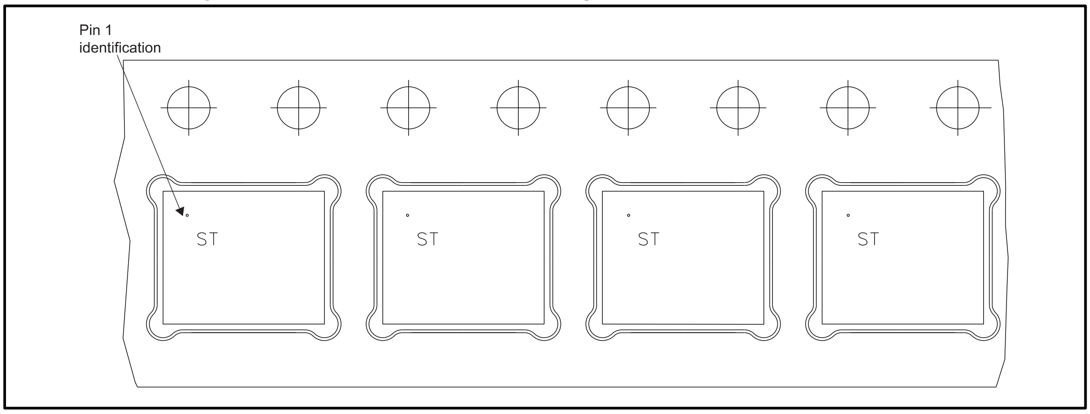
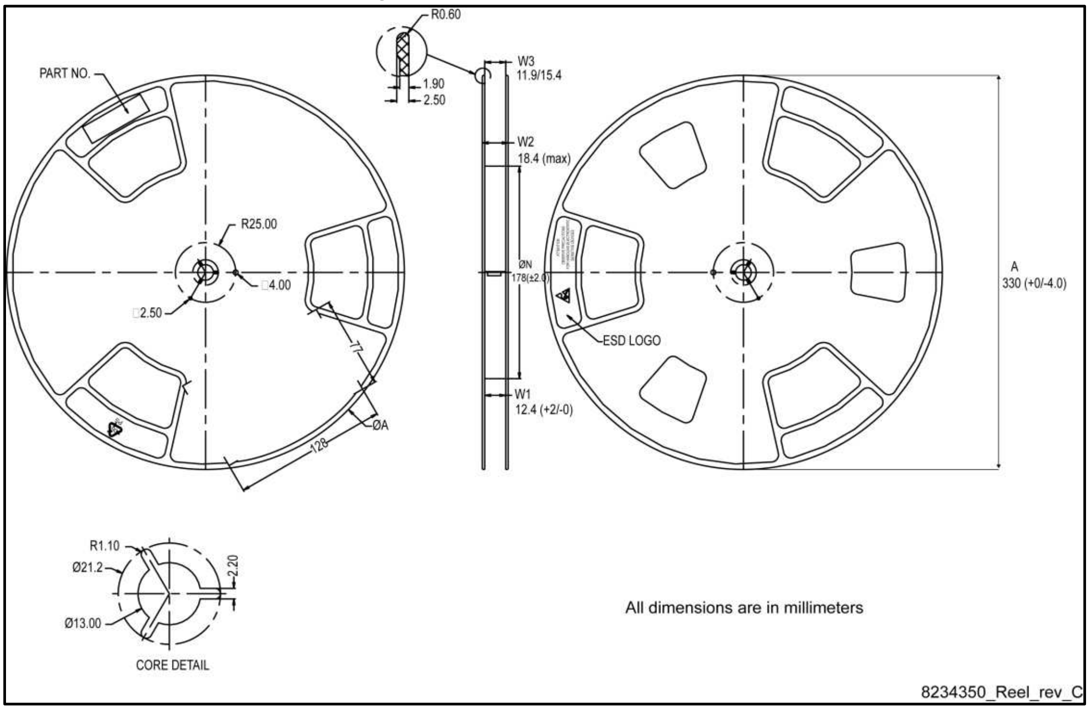


Figure 24: PowerFLAT™ 5x6 reel



5 Revision history

Table 11: Document revision history

Date	Revision	Changes
02-May-2016	1	First release.
07-Dec-2016	2	Document status promoted from preliminary to production data.