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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





# STL20NM20N

## N-CHANNEL 200V - 0.088Ω - 20A PowerFLAT™ ULTRA LOW GATE CHARGE MDmesh™ II MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STL20NM20N	200 V	< 0.105 Ω	20 A

- WORLDWIDE LOWEST GATE CHARGE
- TYPICAL R<sub>DS(on)</sub> = 0.088Ω
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- LOW GATE RESISTANCE
- LOW INPUT CAPACITANCE
- HIGH dv/dt and AVALANCHE CAPABILITIES

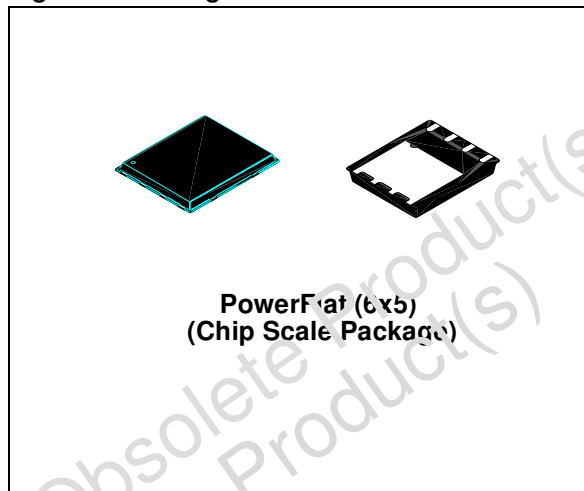
### DESCRIPTION

This 200V MOSFET with a new advanced layout brings all unique advantages of MDmesh technology to lower voltages. The device exhibits worldwide lowest gate charge for any given on-resistance. Its use is therefore ideal as primary switch in isolated DC-DC converters for Telecom and Computer applications. Used in combination with secondary-side low-voltage STRipFET™ products, it contributes to reducing losses and boosting efficiency. The new PowerFLAT™ package allows a significant reduction in board space without compromising performance.

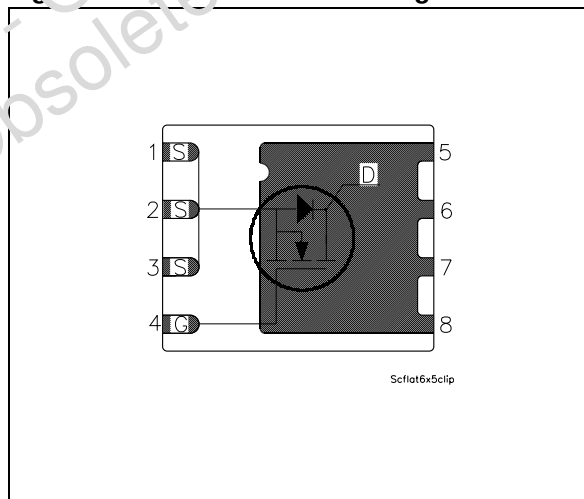
### APPLICATIONS

The MDmesh™ family is very suitable for increasing power density allowing system miniaturization and higher efficiencies.

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STL20NM20N	L20NM20N	PowerFLAT™(6x5)	TAPE & REEL

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	200	V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	200	V
$V_{GS}$	Gate- source Voltage	$\pm 30$	V
$I_D$ (1)	Drain Current (continuous) at $T_C = 25^\circ\text{C}$ (Steady State) Drain Current (continuous) at $T_C = 100^\circ\text{C}$	20 12.3	A A
$I_{DM}$ (3)	Drain Current (pulsed)	80	A
$P_{TOT}$ (2)	Total Dissipation at $T_C = 25^\circ\text{C}$ (Steady State)	2.5	W
$P_{TOT}$ (1)	Total Dissipation at $T_C = 25^\circ\text{C}$ (Steady State)	80	W
	Derating Factor (2)	0.02	W/ $^\circ\text{C}$
$dv/dt$ (4)	Peak Diode Recovery voltage slope	10	V/ns

**Table 4: Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{thj-c}$	Thermal Resistance Junction-case		1.56	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$ (2)	Thermal Resistance Junction-pcb	35	50	$^\circ\text{C}/\text{W}$
$T_j$ $T_{stg}$	Max. Operating Junction Temperature Storage Temperature	-55 to 150		$^\circ\text{C}$

**Table 5: Avalanche Characteristics**

Symbol	Parameter	Max. Value	Unit
$I_{AS}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max)	20	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DL} = 35 \text{ V}$ )	380	mJ

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^\circ\text{C}$  UNLESS OTHERWISE SPECIFIED)**Table 6: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}$ , $V_{GS} = 0$	200			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ , $T_C = 125^\circ\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 30 \text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 10 \text{ A}$		0.088	0.105	$\Omega$

## ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (5)	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		8		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$		800 330 130		pF pF pF
$C_{oss\ eq.}$ (*)	Equivalent Output Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 160\text{ V}$		225		pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 100\text{ V}, I_D = 10\text{ A}$ $R_G = 4.7\Omega, V_{GS} = 10\text{ V}$ (see Figure 16)		40 15 40 11		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 160\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}$ (see Figure 19)		32 6 25	50	nC nC nC

(\*)  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				20	A
$I_{SDM}$ (3)	Source-drain Current (pulsed)				80	A
$V_{SD}$ (5)	Forward On Voltage	$I_{SD} = 20\text{ A}, V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD} = 100\text{ V}, T_j = 25^\circ\text{C}$ (see Figure 17)		160 960 128		ns nC A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD} = 100\text{ V}, T_j = 150^\circ\text{C}$ (see Figure 17)		225 1642 15		ns nC A

- Note: 1. The value is rated according to  $R_{thj-c}$ .  
 2. When Mounted on FR-4 Board of 1inch<sup>2</sup>, 2 oz Cu  
 3. Pulse width limited by safe operating area  
 4.  $I_{SD} \leq 20\text{ A}, di/dt \leq 400\text{ A}/\mu\text{s}, V_{DD} \leq V_{(BR)DSS}$   
 5. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

Figure 3: Safe Operating Area

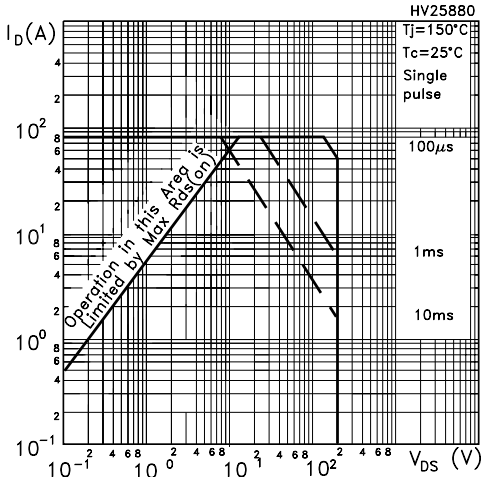


Figure 4: Output Characteristics

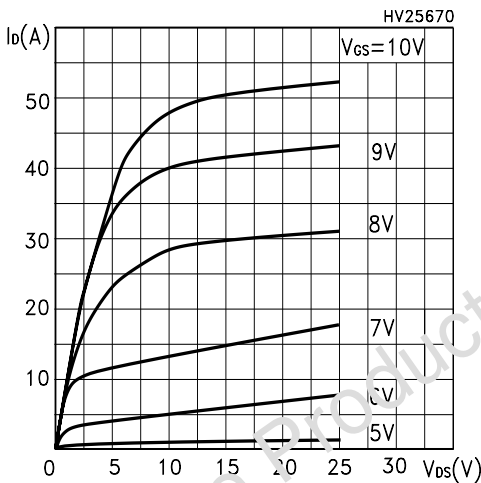


Figure 5: Transconductance

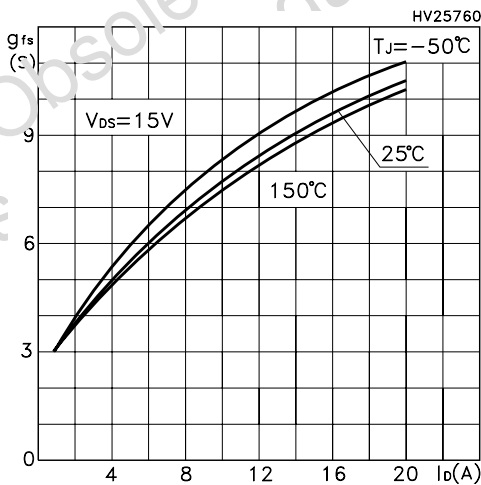


Figure 6: Thermal Impedance

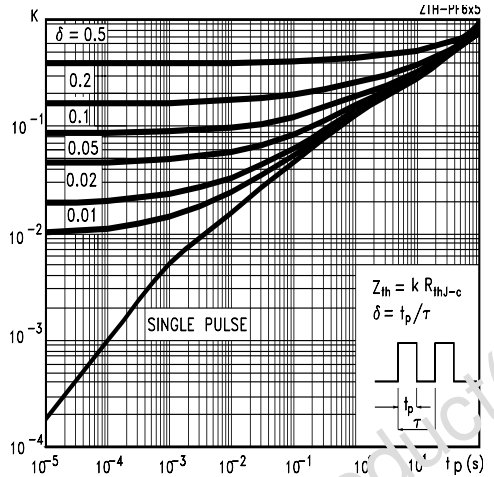


Figure 7: Transfer Characteristics

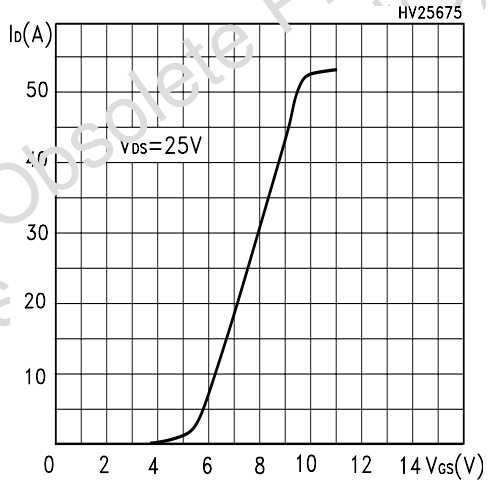


Figure 8: Static Drain-source On Resistance

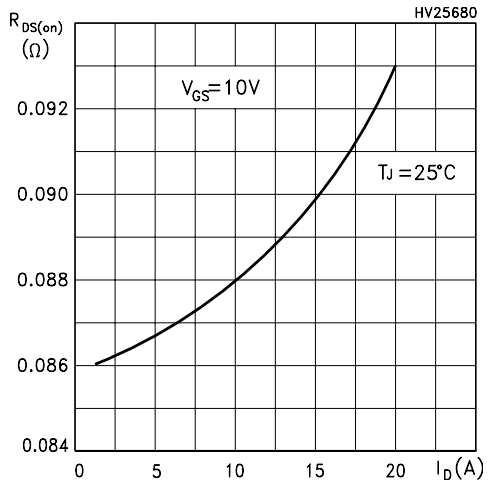


Figure 9: Gate Charge vs Gate-source Voltage

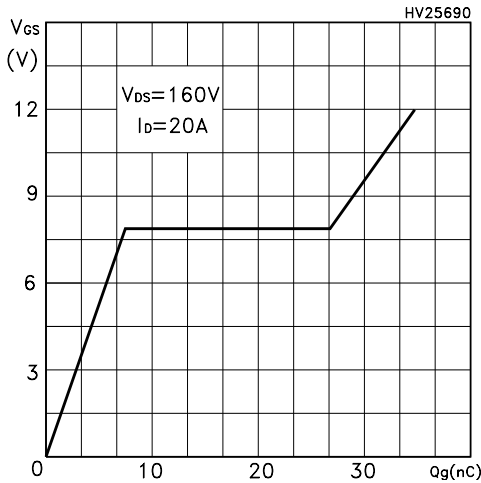


Figure 10: Normalized Gate Threshold Voltage vs Temperature

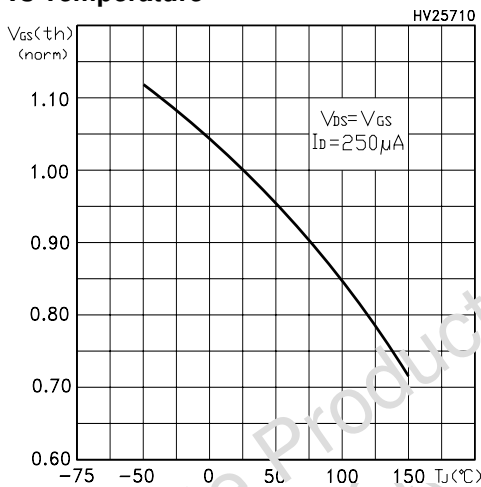


Figure 11: Source-Drain Diode Forward Characteristics

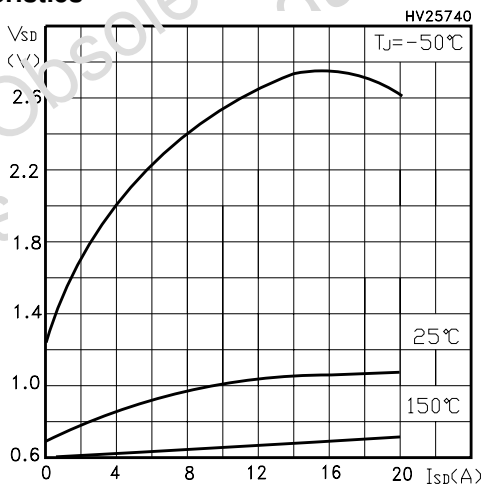


Figure 12: Capacitance Variations

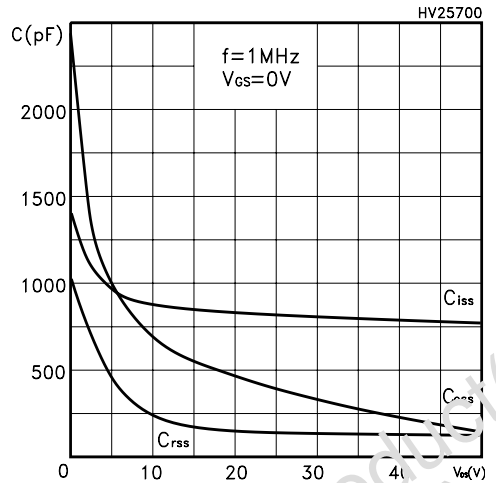


Figure 13: Normalized On Resistance vs Temperature

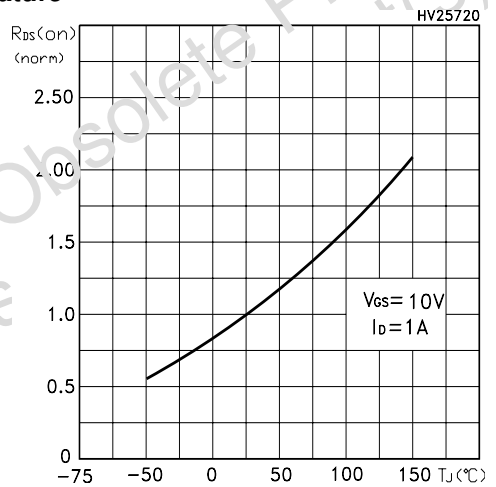


Figure 14: Normalized BVds vs Temperature

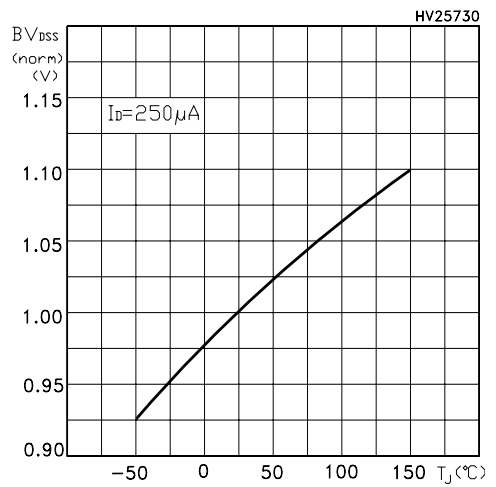


Figure 15: Unclamped Inductive Load Test Circuit

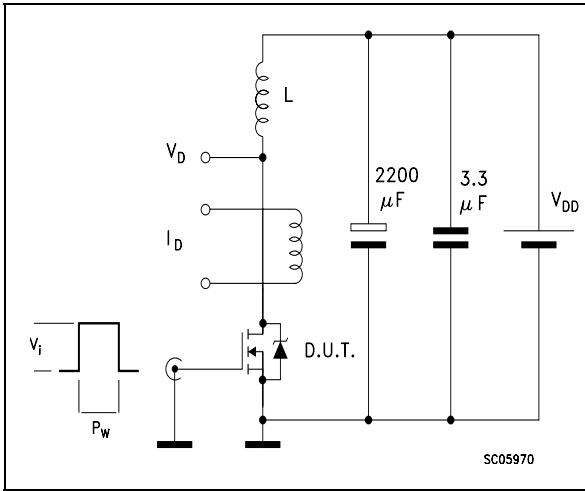


Figure 16: Switching Times Test Circuit For Resistive Load

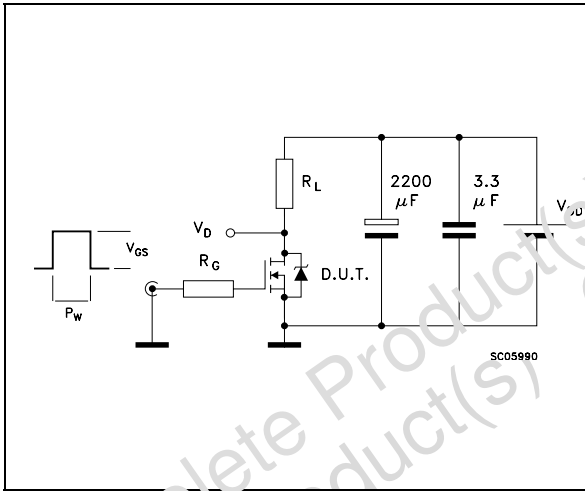


Figure 17: Test Circuit For Inductive Load Switching and Diode Recovery Times

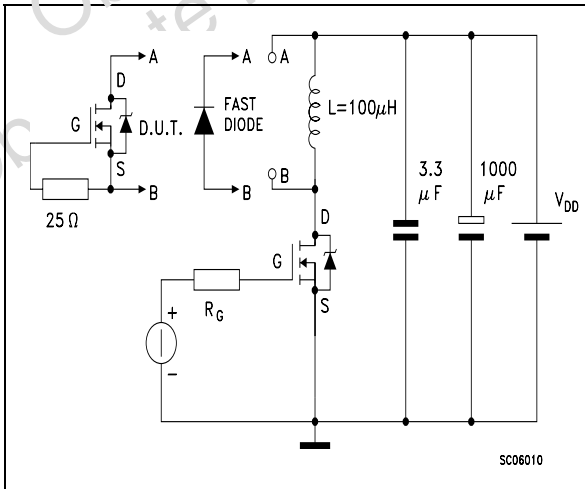


Figure 18: Unclamped Inductive Waferform

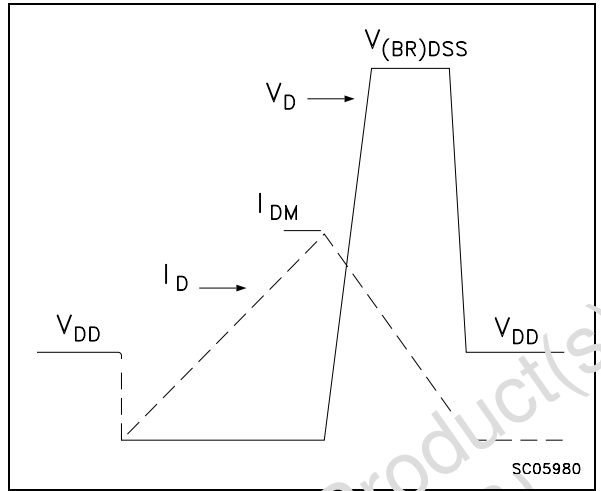
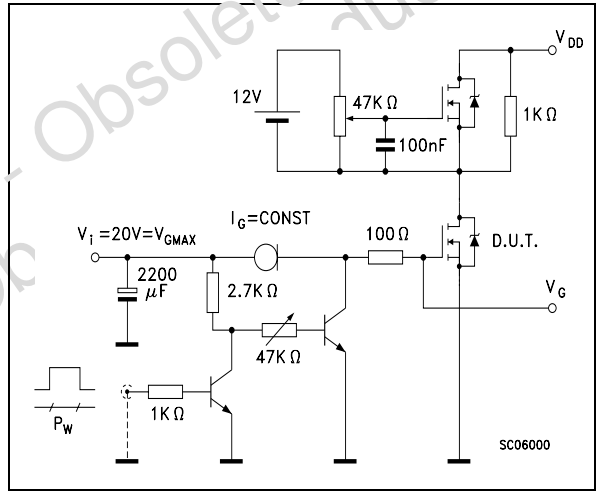


Figure 19: Gate Charge Test Circuit



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

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**PowerFLAT™ (6x5) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035

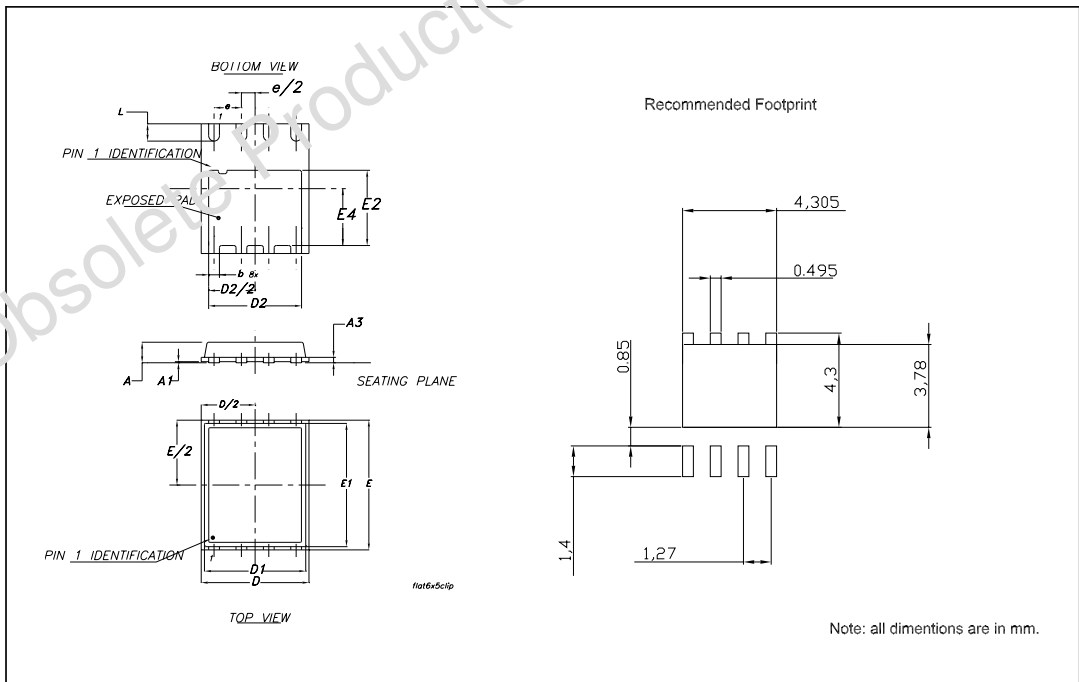


Table 9: Revision History

Date	Revision	Description of Changes
16-Feb-2005	2	New stylesheet Some Values changed on table 6 and 8
09-Jun-2005	3	Inserted curves
20-Jun-2005	4	Updated mechanical data
04-Nov-2005	5	Modified value on table 8, inserted ecopack indication
09-Jan-2006	6	New footprint

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