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STL40DN3LLH5

Dual N-channel 30 V, 0.016 Ω , 11 A
PowerFLAT™ (5x6) double island, STripFET™ V Power MOSFET

Preliminary data

Features

| Type | V _{DSS} | R _{DS(on)} | I _D |
|--------------|------------------|---------------------|---------------------|
| STL40DN3LLH5 | 30 V | < 0.018 Ω | 11 A ⁽¹⁾ |

1. The value is rated according R_{thj-pcb}

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Application

Switching applications

Description

This product utilizes the 5th generation of design rules of ST's proprietary STripFET™ technology. The lowest available R_{DS(on)}*Q_g, in this chip scale package, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

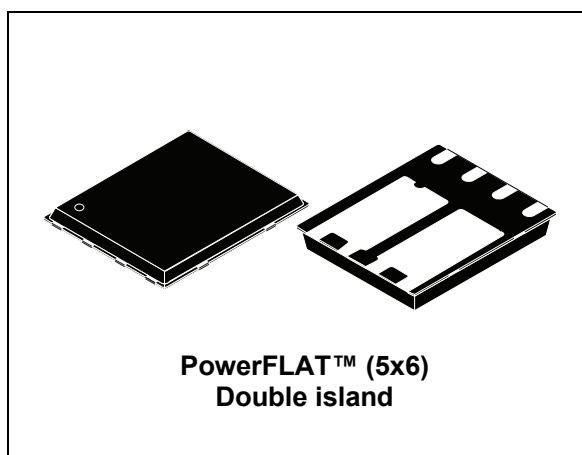


Figure 1. Internal schematic diagram

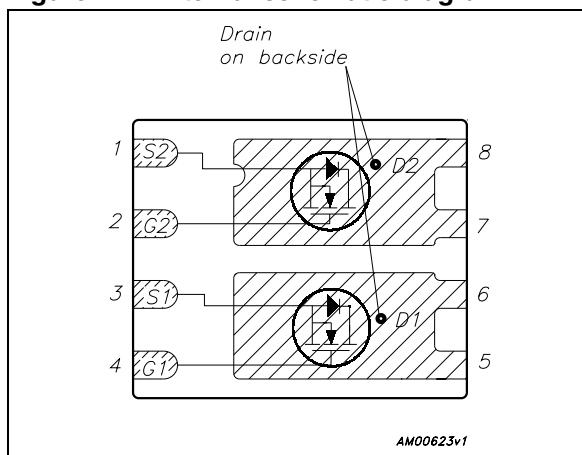


Table 1. Device summary

| Order code | Marking | Package | Packaging |
|--------------|-----------|----------------------------------|---------------|
| STL40DN3LLH5 | 40DN3LLH5 | PowerFLAT™(5x6) Double island | Tape and reel |

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------------|---|------------|---------------------|
| V_{DS} | Drain-source voltage ($V_{GS} = 0$) | 30 | V |
| V_{GS} | Gate-source voltage | ± 22 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25^\circ\text{C}$ | 40 | A |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 100^\circ\text{C}$ | 26 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_C = 25^\circ\text{C}$ | 11 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_C = 100^\circ\text{C}$ | 7 | A |
| $I_{DM}^{(3)}$ | Drain current (pulsed) | 44 | A |
| $P_{TOT}^{(1)}$ | Total dissipation at $T_C = 25^\circ\text{C}$ | 60 | W |
| $P_{TOT}^{(2)}$ | Total dissipation at $T_C = 25^\circ\text{C}$ | 4 | W |
| | Derating factor | 0.03 | W/ $^\circ\text{C}$ |
| T_J | Operating junction temperature | -55 to 150 | $^\circ\text{C}$ |
| T_{stg} | Storage temperature | | |

1. The value is rated according R_{thj-c}
2. The value is rated according $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

| Symbol | Parameter | Value | Unit |
|---------------------|---|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case (drain) (steady state) | 2.08 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-ambient | 32 | $^\circ\text{C}/\text{W}$ |

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10$ sec

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|---|------|---------------|----------------|----------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 250 \mu A, V_{GS} = 0$ | 30 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating @ } 125^{\circ}C$ | | | 1 10 | μA μA |
| I_{GSS} | Gate body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 22 V$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 250 \mu A$ | 1 | 1.5 | | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS} = 10 V, I_D = 5.5 A$ $V_{GS} = 4.5 V, I_D = 5.5 A$ | | 0.016 0.02 | 0.018 0.025 | Ω Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|--|------|------|------|------|
| C_{iss} | Input capacitance | $V_{DS} = 25 V, f = 1 \text{ MHz}, V_{GS} = 0$ | - | 475 | - | pF |
| C_{oss} | Output capacitance | | | 97 | | |
| C_{rss} | Reverse transfer capacitance | | | 19 | | |
| Q_g | Total gate charge | $V_{DD} = 15 V, I_D = 11 A$ | - | 4.5 | - | nC |
| Q_{gs} | Gate-source charge | $V_{GS} = 4.5 V$ | | 1.7 | | |
| Q_{gd} | Gate-drain charge | (see Figure 3) | | 1.9 | | |

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit | |
|--------------|---------------------|---|------|------|------|------|----|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}=15\text{ V}$, $I_D=11\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ (see Figure 2) | | 4 | | ns | |
| t_r | Rise time | | - | 22 | - | ns | |
| $t_{d(off)}$ | Turn-off delay time | | | | 13 | | ns |
| t_f | Fall time | | | | 2.8 | | ns |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|------|------|------|------|
| I_{SD} | Source-drain current | | - | | 11 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 44 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD}=11\text{ A}$, $V_{GS}=0$ | - | | 1.1 | V |
| t_{rr} | Reverse recovery time | $I_{SD}=11\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$, $V_{DD}=25\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ | | 16.2 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 1 | | nC |
| I_{RRM} | Reverse recovery current | | | | 8.1 | |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

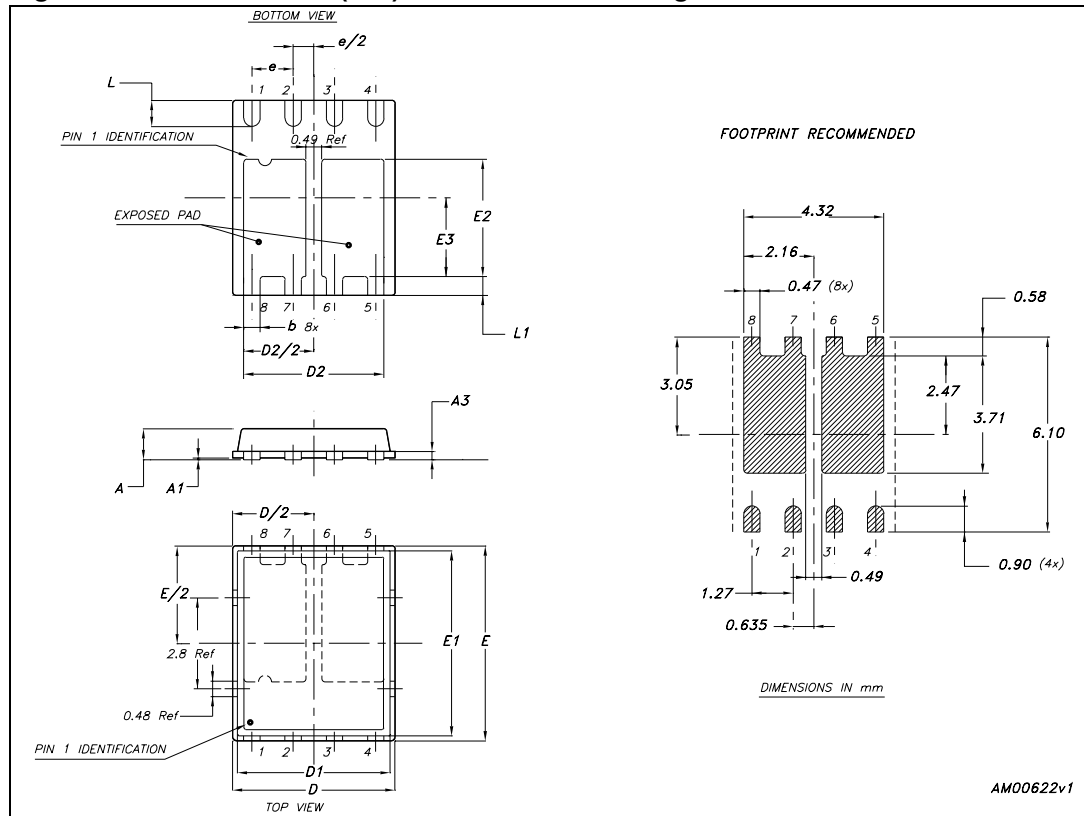
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ (5x6) double island mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.83 | 0.90 |
| A1 | | 0.02 | 0.05 |
| A3 | | 0.20 | |
| b | 0.35 | 0.40 | 0.47 |
| D | | 5.00 | |
| D1 | | 4.75 | |
| D2 | 4.11 | 4.21 | 4.31 |
| E | | 6.00 | |
| E1 | | 5.75 | |
| E2 | 3.51 | 3.61 | 3.71 |
| E3 | 2.32 | 2.42 | 2.52 |
| e | | 1.27 | |
| L | 0.70 | 0.80 | 0.90 |
| L1 | 0.48 | 0.58 | 0.68 |

Figure 8. PowerFLAT™ (5x6) double island drawing



5 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|---------------|
| 24-Jan-2011 | 1 | First release |

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