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STL42P6LLF6

P-channel -60 V, 23 mΩ typ., -42 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

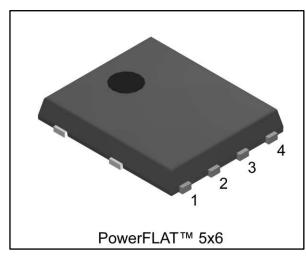
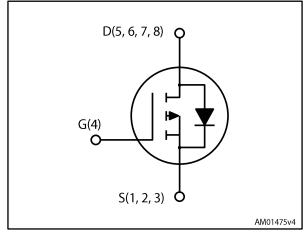


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	ID
STL42P6LLF6	-60 V	26 mΩ	-42 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

• Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET $^{\text{TM}}$ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{\text{DS(on)}}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL42P6LLF6	42P6LLF6	PowerFLAT™ 5x6	Tape and reel

Contents STL42P6LLF6

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STL42P6LLF6 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	-60	٧
V_{GS}	Gate-source voltage	± 20	٧
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	-42	Α
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	-30	Α
I _D ⁽¹⁾⁽³⁾	Drain current (pulsed)	-168	Α
I _D ⁽²⁾	Drain current (continuous) at T _{pcb} = 25 °C	-9	Α
I _D ⁽²⁾	Drain current (continuous) at T _{pcb} = 100 °C	-6.6	Α
I _{DM} ⁽²⁾⁽³⁾	Drain current (pulsed)	-36	Α
P _{TOT} ⁽¹⁾	Total dissipation at T _C = 25 °C 100		W
P _{TOT} ⁽²⁾	Total dissipation at T _{pcb} = 25 °C 4.8		W
T _{stg}	Storage temperature range	55 to 175	٥°
Tj	Operating junction temperature range		10

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	1.5	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max		°C/W

Notes:

 $^{^{(1)}\!} The$ value is rated by $R_{thj\text{-case}}.$

 $^{^{(2)}}$ The value is rated by $R_{thj\text{-pcb}}$.

 $[\]ensuremath{^{(3)}}\mbox{Pulse}$ width is limited by safe operating area.

 $^{^{(1)}\!}When$ mounted on FR-4 board of 1 inch², 2 Oz Cu, t < 10 s.

Electrical characteristics STL42P6LLF6

2 Electrical characteristics

(T_C= 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-60			>
	Zaro gata valtaga Drain	$V_{GS} = 0 \text{ V}, V_{DS} = -60 \text{ V}$			-1	μΑ
IDSS	Zero gate voltage Drain current	$V_{GS} = 0 \text{ V}, V_{DS} = -60 \text{ V},$ $T_{C} = 125 \text{ °C}^{(1)}$			-10	μΑ
I _{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$	-1		-2.5	V
R _{DS(on)} Static drain-source on- resistance		$V_{GS} = -10 \text{ V}, I_{D} = -4.5 \text{ A}$		23	26	mΩ
		V _{GS} = -4.5 V, I _D = -4.5 A		28	34	11122

Notes:

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		1	3780	1	pF
Coss	Output capacitance	V _{DS} = -25 V, f = 1 MHz,	-	262	-	pF
Crss	Reverse transfer capacitance	$V_{GS} = 0 V$	1	170	1	рF
Qg	Total gate charge	$V_{DD} = -30 \text{ V}, I_{D} = -9 \text{ A},$	ı	30	1	nC
Qgs	Gate-source charge	V _{GS} = -4.5 V (see <i>Figure 14: "Gate charge</i>	1	10.8	1	nC
Q_{gd}	Gate-drain charge	test circuit")	1	10.5	1	nC
Rg	Gate input resistance	I _D = 0 A, f = 1 MHz	-	1.7	-	Ω

Table 6: Switching times

Table of Carriering Limits						
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = -30 \text{ V}, I_{D} = -4.5 \text{ A},$	-	51.4	-	ns
tr	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = -10 V$	-	39	-	ns
t _{d(off)}	Turn-off-delay time	(see Figure 13: "Switching times test circuit for resistive	-	171	-	ns
t _f	Fall time	load")	-	21	-	ns

⁽¹⁾Defined by design, not subject to production testing

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-	-42		Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-	-168		Α
V _{SD} (2)	Forward on voltage	$V_{GS} = 0 \text{ V}, I_{SD} = -9 \text{ A}$	-		-1.1	٧
t _{rr}	Reverse recovery time $I_{SD} = -9 \text{ A}$, $di/dt = 100 \text{ A/}\mu\text{s}$,		1	34		ns
Qrr	Reverse recovery charge	$V_{DD} = -4.8 \text{ V}, T_j = 150 \text{ °C}$ (see Figure 15: "Test circuit for		48		nC
I _{RRM}	Reverse recovery current	inductive load switching and diode recovery times")	-	-2.8		Α

Notes:

⁽¹⁾Pulse width limited by safe operating area

 $^{^{(2)}\}text{Pulse}$ test: pulse duration = 300 $\mu\text{s},$ duty cycle 1.5%

2.1 Electrical characteristics (curves)



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

Figure 2: Safe operating area

ID(A)

102

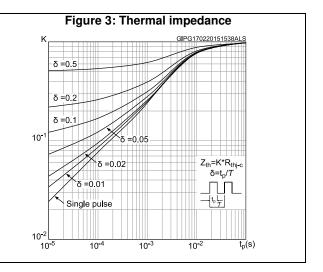
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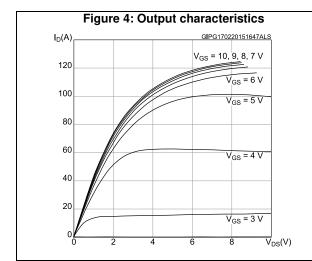
100 µs

1 ms

10 ms

10 ms





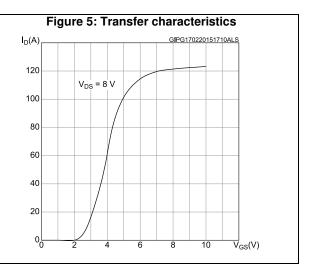


Figure 7: Normalized V_{(BR)DSS} vs temperature
V_{(BR)DSS} (norm.)

1.10

1.00

1.00

0.95

0.90

-75

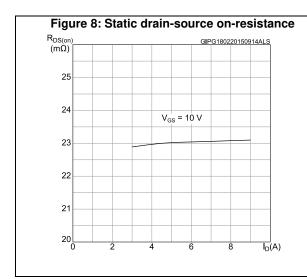
-25

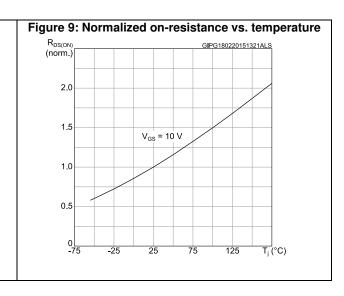
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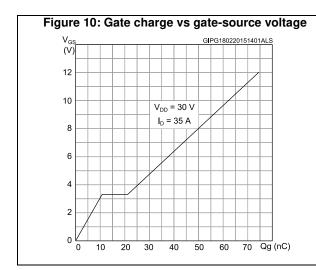
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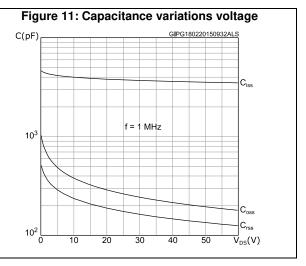
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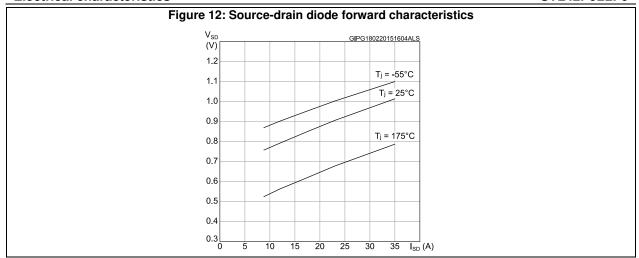
T_J(°C)





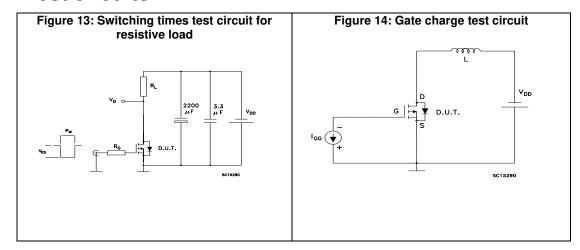


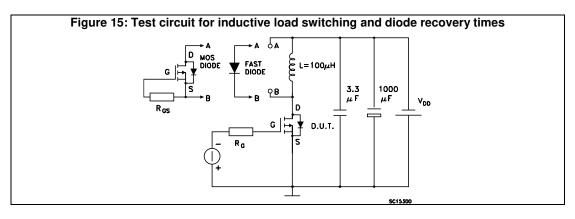




STL42P6LLF6 Test circuits

3 Test circuits





4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

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4.1 PowerFLAT™ 5x6 type R package information

Figure 16: PowerFLAT™ 5x6 type R package outline

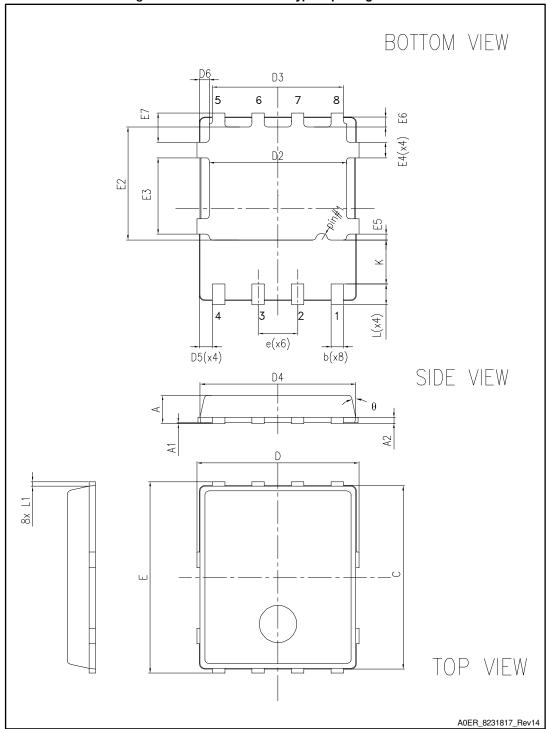
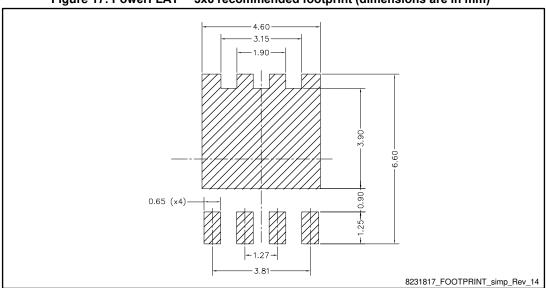


Table 8: PowerFLAT™ 5x6 type R mechanical data

Table 8: PowerFLAT™ 5x6 type R mechanical data				
Dim.		mm		
Dilli.	Min.	Тур.	Max.	
А	0.80		1.00	
A1	0.02		0.05	
A2		0.25		
b	0.30		0.50	
С	5.80	6.00	6.20	
D	5.00	5.20	5.40	
D2	4.15		4.45	
D3	4.05	4.20	4.35	
D4	4.80	5.00	5.20	
D5	0.25	0.40	0.55	
D6	0.15	0.30	0.45	
е		1.27		
Е	5.95	6.15	6.35	
E2	3.50		3.70	
E3	2.35		2.55	
E4	0.40		0.60	
E5	0.08		0.28	
E6	0.20	0.325	0.45	
E7	0.75	0.90	1.05	
K	1.275		1.575	
L	0.60		0.80	
L1	0.05	0.15	0.25	
θ	0°		12°	

Figure 17: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 18: PowerFLAT™ 5x6 tape (dimensions are in mm)

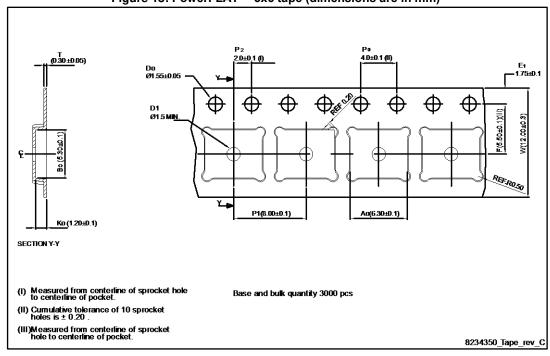
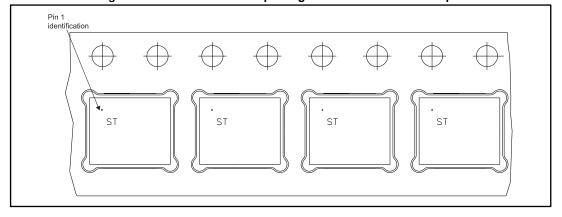


Figure 19: PowerFLAT™ 5x6 package orientation in carrier tape



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8234350_Reel_rev_C

Figure 20: PowerFLAT™ 5x6 reel PART NO. A 330 (+0/-4.0) ESD LOGO All dimensions are in millimeters CORE DETAIL

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STL42P6LLF6 Revision history

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
28-Oct-2013	1	First release.
25-Aug-2014	2	Modified: Figure 1: "Internal schematic diagram" Updated: Section 10: "Package mechanical data" Minor text changes
24-Feb-2015	3	In title description on cover page, changed 0.02Ω to 0.023Ω In features table on cover page, changed 0.028Ω to 0.026Ω Updated <i>Table 2: Absolute maximum ratings</i> Updated <i>Table 4: Static</i> – renamed table and updated Static drainsource on-resistance values Updated <i>Table 5: Dynamic</i> – test conditions and all typical values Updated <i>Table 6: Switching times</i> – test conditions and all typical values Updated <i>Table 7: Source-drain diode</i> – test conditions and all typical values Updated <i>Table 7: Source-drain diode</i> – test conditions and all typical values Added <i>Section 2.2: Electrical characteristics (curves)</i> Updated <i>Section 4: Package mechanical data</i> Minor text changes
15-Nov-2016	4	Updated title, features table and description on cover page Updated <i>Table 2: "Absolute maximum ratings"</i> Updated <i>Table 4: "Static", Table 5: "Dynamic", Table 6: "Switching times"</i> and <i>Table 7: "Source drain diode"</i> Updated <i>Figure 9: "Normalized on-resistance vs. temperature"</i> Updated <i>Section 4.1: "PowerFLAT™ 5x6 type R package information"</i> Minor text changes

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